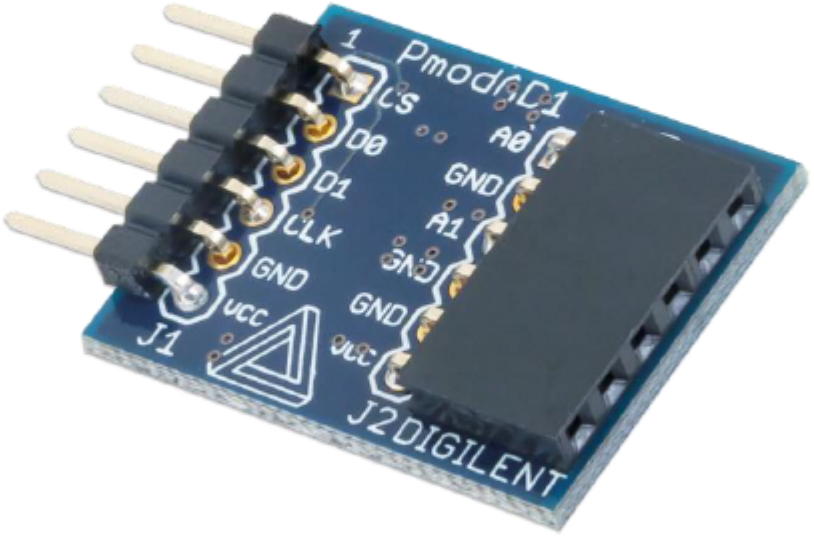
PmodAD1™ Reference Manual

Overview

The Digilent PmodAD1 is a two channel 12-bit analog-to-digital converter that features Analog Devices AD7476A. With a sampling rate of up to 1 million samples per second, this Pmod is capable of excelling in even the most demanding audio applications.



The PmodAD1.

Features include:

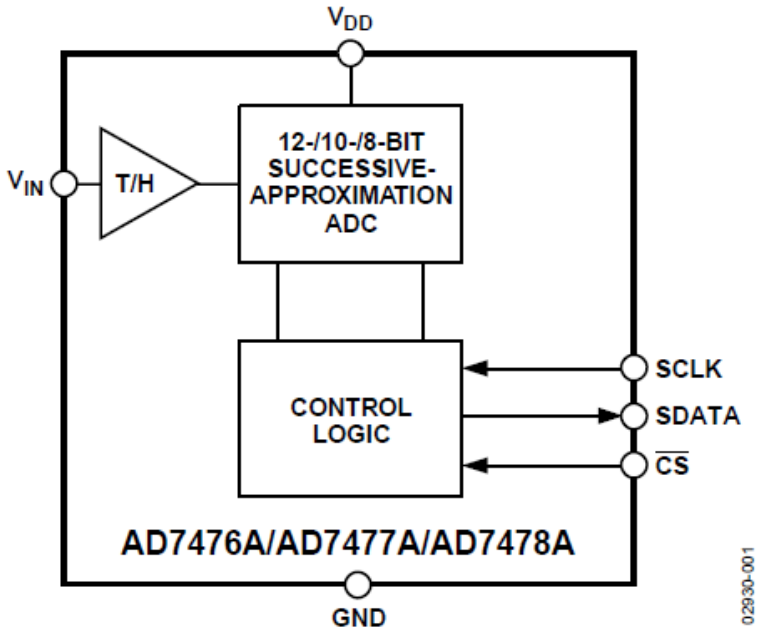
- Two channel 12-bit analog-to-digital converter
- Simultaneous A/D conversion at up to one MSa per channel
- Two 2-pole Sallen-Key anti-alias filters
- Small PCB size for flexible designs 0.95 in × 0.8 in (2.4 cm × 2.0 cm)
- 6-pin Pmod port with GPIO interface
- Library and example code available in resource center

1 Interfacing with the Pmod

The PmodAD1 communicates with the host board via an SPI-like communication protocol. The difference between the standard SPI protocol and this protocol is manifested in the pin arrangement on this Pmod. A typical SPI interface would expect a Chip Select, a Master-Out-Slave-In, a Master-in-Slave-Out, and a Serial Clock signal. However, with the two ADCs on this chip, both of the data lines (MOSI and MISO) are designed to operate only as outputs, making them both Master-In-Slave-Out data lines.

The PmodAD1 will provide its 12 bits of information to the system board through 16 clock cycles with first four bits consisting of four leading zeroes and the remaining 12 bits representing the 12 bits of the data with the MSB first. The first leading zero is clocked out on the falling edge of the CS signal with all of the subsequent bits clocked out on the falling edge of the serial clock signal.

FUNCTIONAL BLOCK DIAGRAM



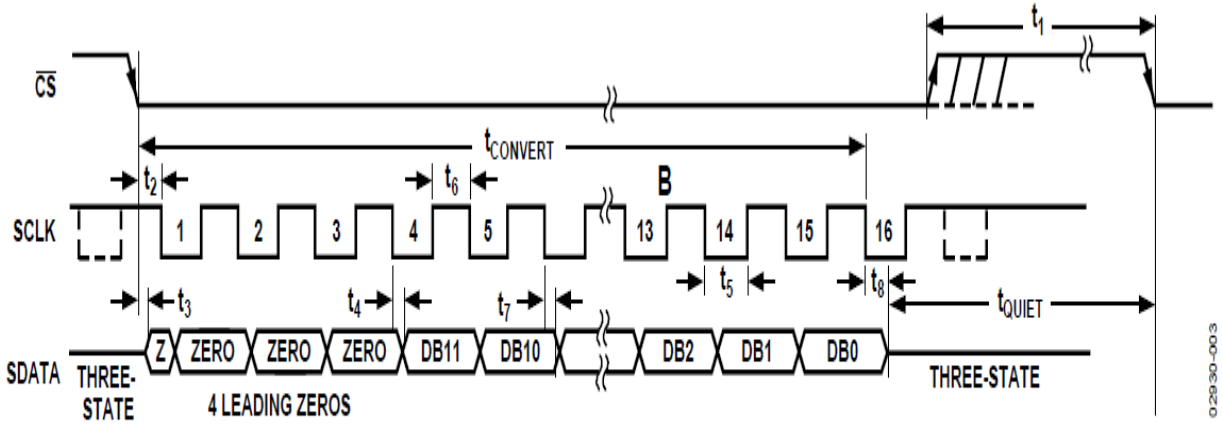


Figure 3. AD7476A Serial Interface Timing Diagram

Header J1		
Pin	**Signal**	**Description**
1	CS	Chip Select
2	D0	Input Data 1
3	D1	Input Data 2
4	SCK	Serial Clock
5	GND	Power Supply Ground
6	VCC	Power Supply (3.3V/5V)

Header J2		
Pin	**Signal**	**Description**
1	A0	Input Data 1
2	GND	Power Supply Ground
3	A1	Input Data 2
4	GND	Power Supply Ground
5	GND	Power Supply Ground
6	VCC	Positive Power Supply

Table 1. Pin descriptions as labeled on the PmodAD1.

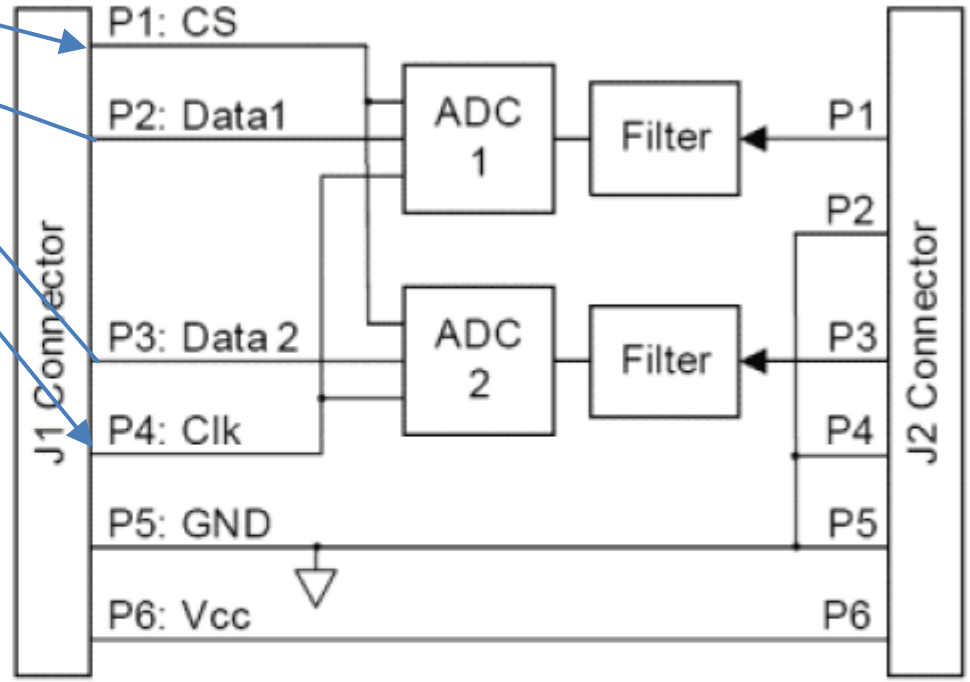
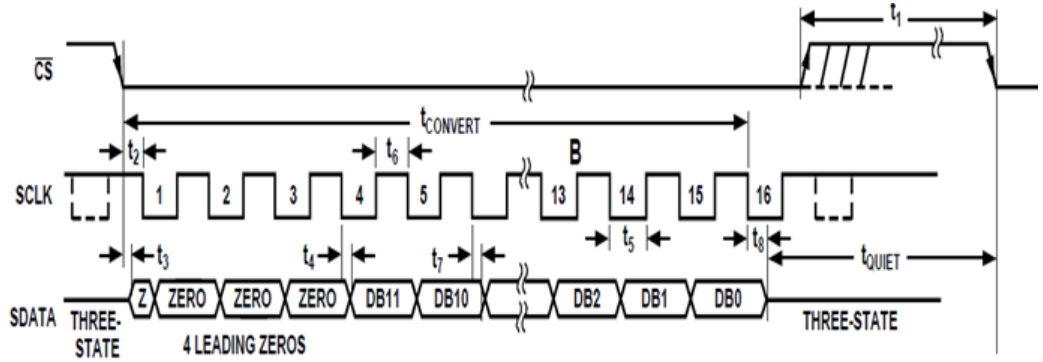


Figure 1. AD1 circuit diagram.

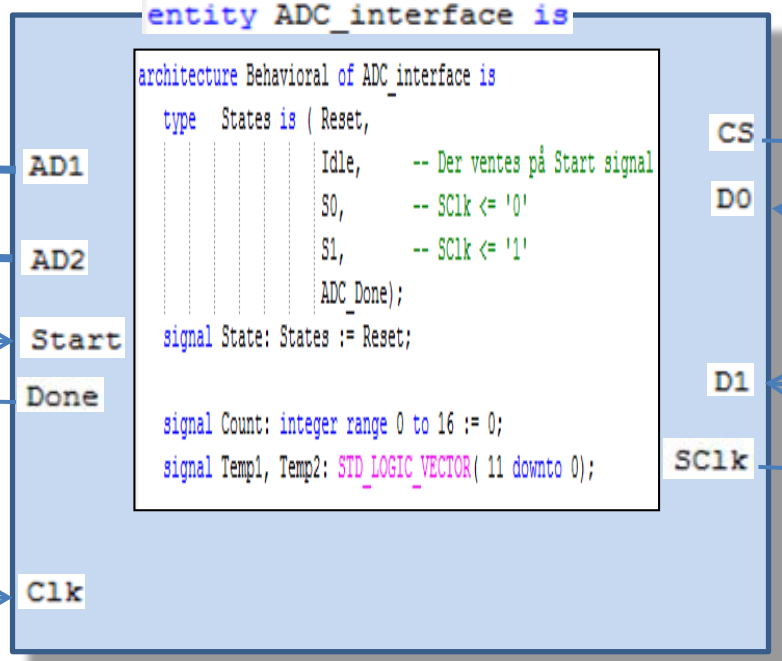


Analoge input signaler

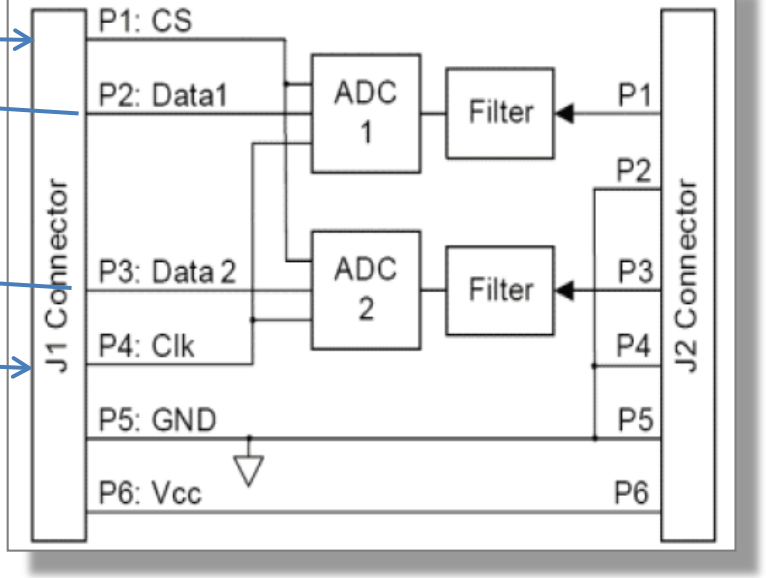
```
entity ADC_interface is
    Port ( Clk :   in  STD_LOGIC;  -- System clock (50 MHz)
           Start : in  STD_LOGIC;  -- Start skift 0->1 starter en konvertering
           Done : out  STD_LOGIC;  -- Done=1 Angiver at konverteringen er færdig
           SClk:  out  STD_LOGIC;  -- Seriel Clock til ADC
           CS:    out  STD_LOGIC;  -- Chip Select til ADC (starter og stopper konverteringen)
           D0:    in   STD_LOGIC;  -- Burde kaldes for D1 - data bit fra ADC0
           D1:    in   STD_LOGIC;  -- Burde kaldes for D2 - data bit fra ADC1
           AD1 :  out  STD_LOGIC_VECTOR (11 downto 0);   -- 12 bit AD data #1
           AD2 :  out  STD_LOGIC_VECTOR (11 downto 0));  -- 12 bit AD data #2
end ADC_interface;
```

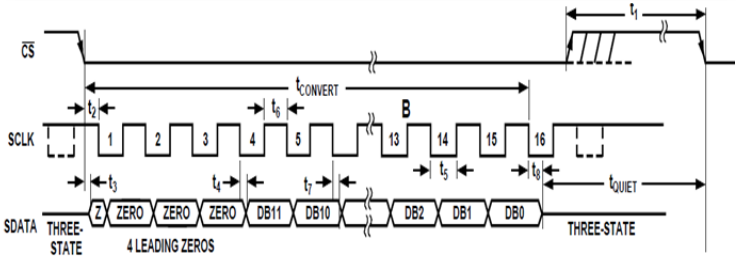
Simulering af den kode som skal bruge det færdige interface.
Faktisk er det kun Start signalet som genereres.

Clock-generator



Simulering af 2 AD konvertere med SPI interface

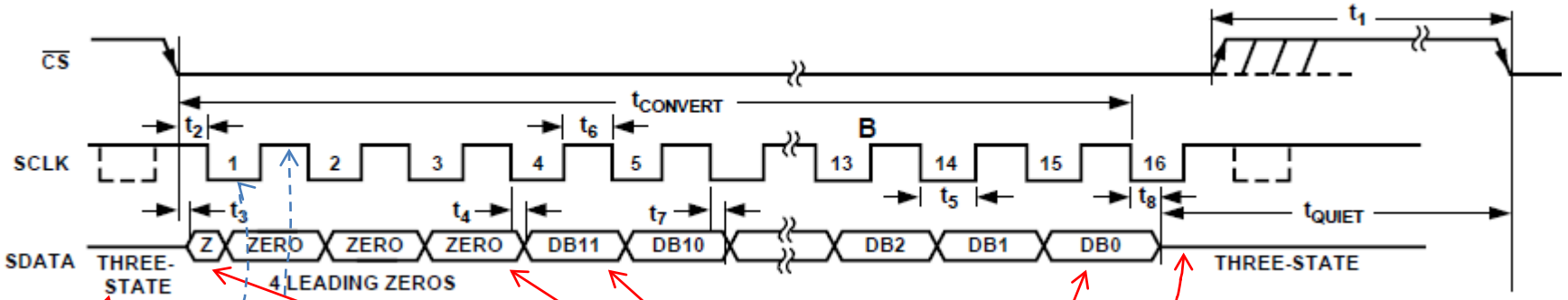




Pseudo kode som eksempel på en ”ADC – DAC” bruger

```
While( true)
{    Start en AD konvertering;
     While (not done ADc);   // Vent på ADC
      Temp = AD_data;
       ”gør et eller andet ved data”
       DA_Data = Temp;
       Overfør data til DA konverter;
       While (not done DAc overførsel);
 }
```

Eksempel på en VHDL process som kan simulere en AD konvertering

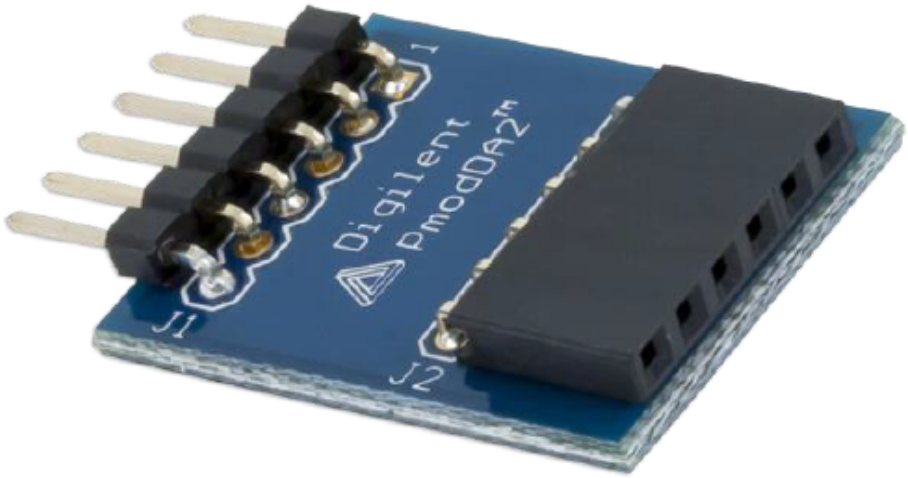



```
AD_Konverter1: process
   variable data: std_logic_vector( 15 downto 0) := "0000HL10ZW-WHL10";
begin
   D0 <= 'Z';
   wait until CS='0';
   D0 <= data(15);
   wait for 2 ns;

   for i in 15 downto 0 loop
      D0 <= data(i);

      wait until SClk='0';

      wait until SClk='1';
   end loop;
   D0 <= '-';
   wait for 15 ns;
   data := X"0123";
end process;
```

PmodDA2™ Reference Manual

Overview

The PmodDA2 is a 12-bit Digital-to-Analog converter powered by the Texas Instruments DAC121S101. As it is able to simultaneously convert two separate channels of digital information provided over an interface similar to SPI, users can easily compare the two reconstructed signals.



The PmodDA2.

Features include:

- 12-bit digital-to-analog converter
- Two simultaneous conversion channels
- Very low power consumption
- Small PCB size for flexible designs 1.0“ × 0.8” (2.5 cm × 2.0 cm)
- 6-pin Pmod connector with GPIO interface
- Library and example code available in resource center

1 Functional Description

The PmodDA2 provides two channels of 12-bit Digital-to-Analog conversion, allowing users to achieve a resolution up to about 1mV.

2 Interfacing with the Pmod

The PmodDA2 communicates with the host board via an SPI-like protocol. By bringing the Chip Select line to a low voltage state, users may send a series of 16 clock pulses on the Serial Clock line (SCLK). The data is sent out with the most significant bit (MSB) first on the last 12 clock pulses. An example data stream of how the data might look is provided from the TI datasheet below:

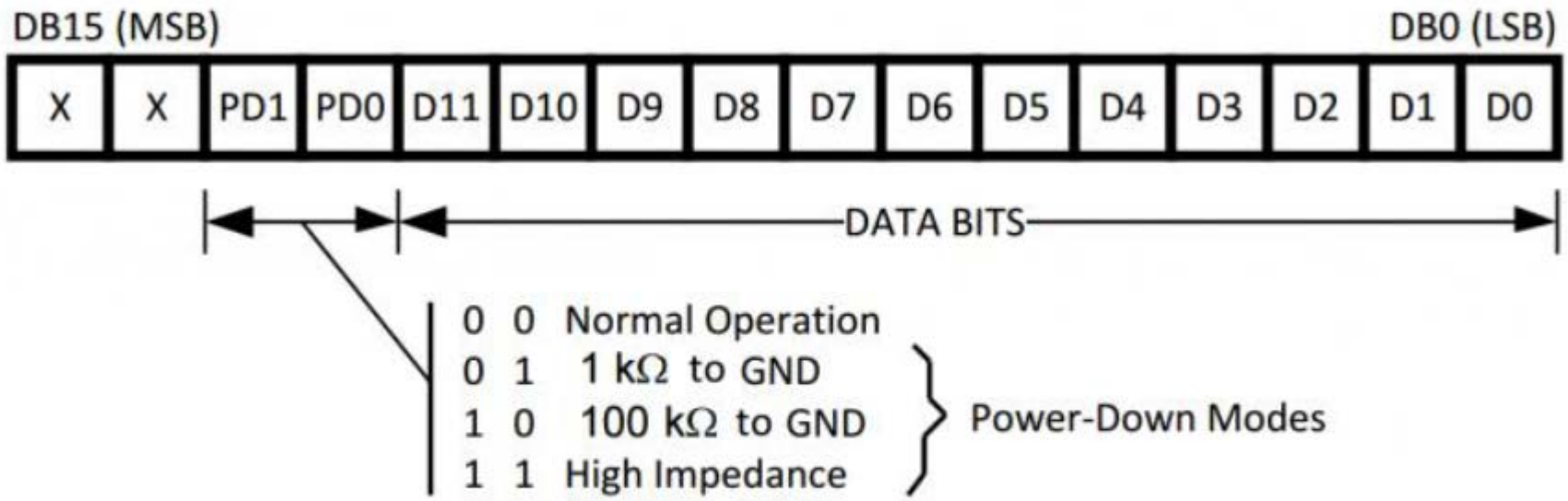


Figure 1. PmodDA2 data stream.

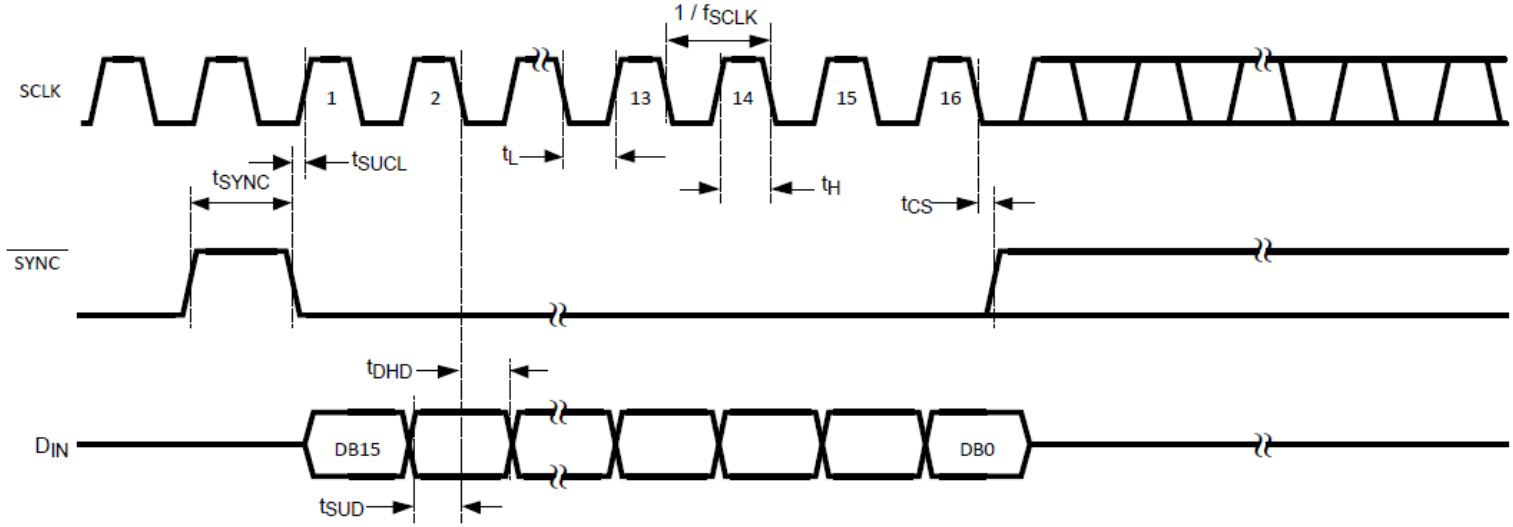


Figure 2. DAC121S101 Timing

Pin	Signal	Description
1	~SYNC	Chip Select
2	DINA	Data In for Channel A
3	DINB	Data In for Channel B
4	SCLK	Serial Clock
5	GND	Power Supply Ground
6	VCC	Power Supply (3.3V/5V)

Table 1. PmodDA2 pinout table.

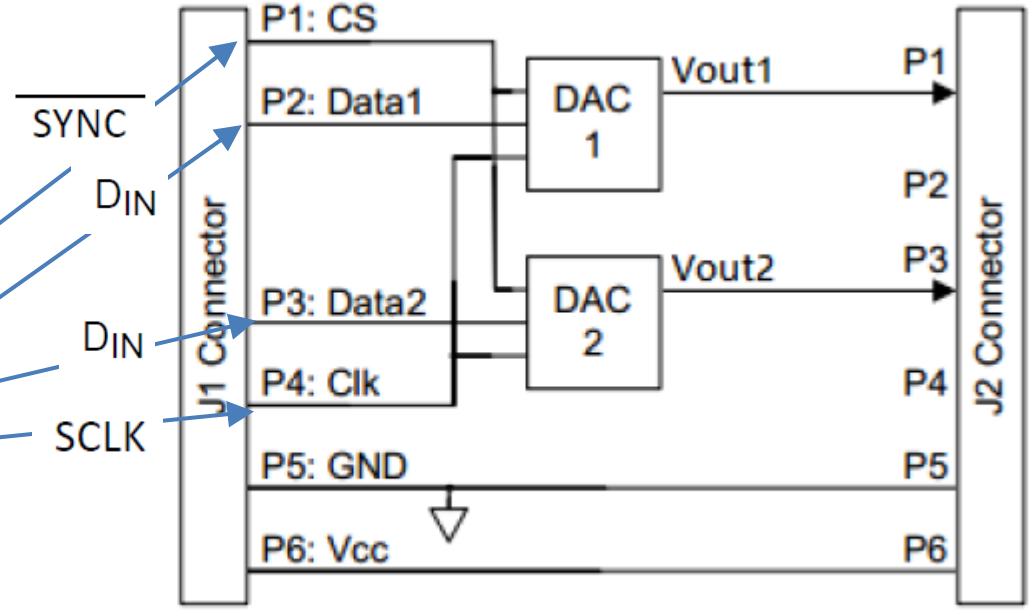


Figure 2. PmodDA2 circuit diagram.

Analoge output signaler