Microprocessor and Computer Architecture (MPCA) Laboratory
UE20CS252 4th Semester,
Academic Year 2021-22

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Week # 2 **Program Number: 1**

Title of the Program

Write a program in ARM7TDMI-ISA to find the sum of N data items at alternate [odd or **even** positions] locations in the memory. Store the result in the memory location.

a. Use Pre-indexing addressing mode
b. Use Post- Indexing addressing mode
c. Use Auto-indexing addressing mode

Program Code

a.

```
; odd alternate pre indexing
.data

        a: .word 10, 20, 30, 40
        sum: .word 0

.text

        mov r2, #0
```

```
        ldr r1, =a
        ldr r3, =sum
        mov r5, #0
        sub r1, r1, #4; initializing r1 for pre indexing

loop:   ldr r4, [r1, #4]
        add r1, r1, #8; increment to skip over even locations
        add r2, r2, r4
        add r5, r5, #2; loop count double increment
        cmp r5, #4
        bne loop

        str r2, [r3]
        swi 0x011

.end
```

b.

```
; even alternate auto indexing
.data

        a: .word 10, 20, 30, 40
        sum: .word 0

.text

        mov r2, #0
        ldr r1, =a
        ldr r3, =sum
        mov r5, #0
        sub r1, r1, #4; initializing r1 for pre indexing, starts at 1 and skips first element

loop:   ldr r4, [r1, #8]!; writeback included
        add r2, r2, r4
        add r5, r5, #2
        cmp r5, #4
        bne loop

        str r2, [r3]
        swi 0x011

.end
```

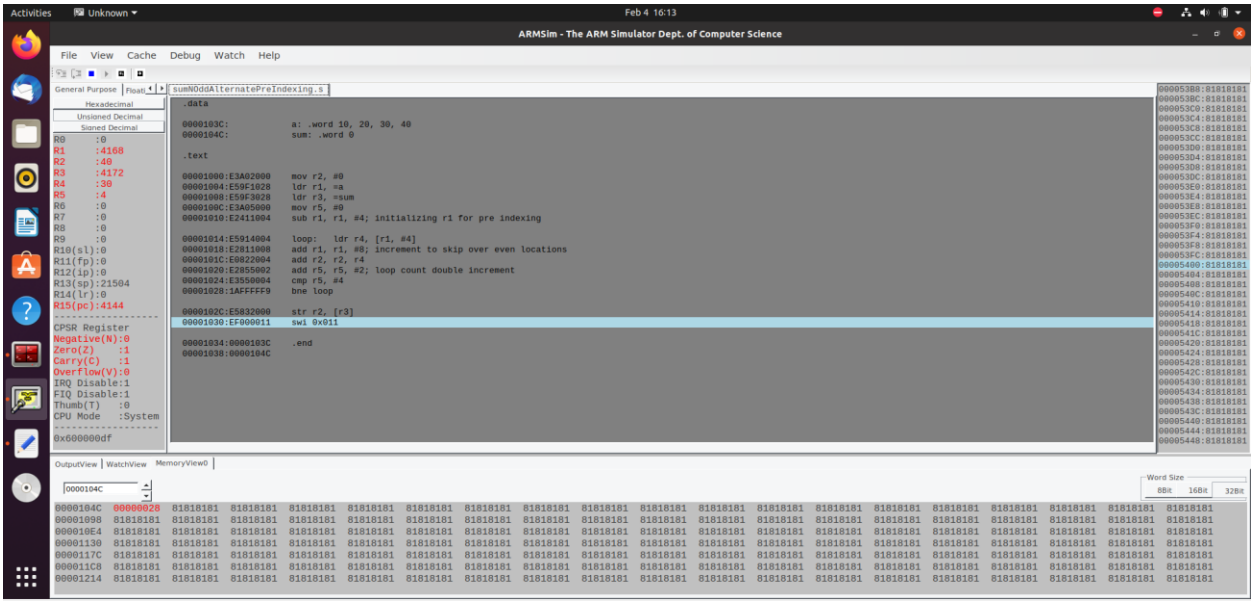
c.

```
; odd alternate post indexing
.data

        a: .word 10, 20, 30, 40
        sum: .word 0

.text

        mov r2, #0
        ldr r1, =a
        ldr r3, =sum
        mov r5, #0

loop:   ldr r4, [r1], #8
        add r2, r2, r4
        add r5, r5, #2
        cmp r5, #4
        bne loop

        str r2, [r3]
        swi 0x011

.end
```

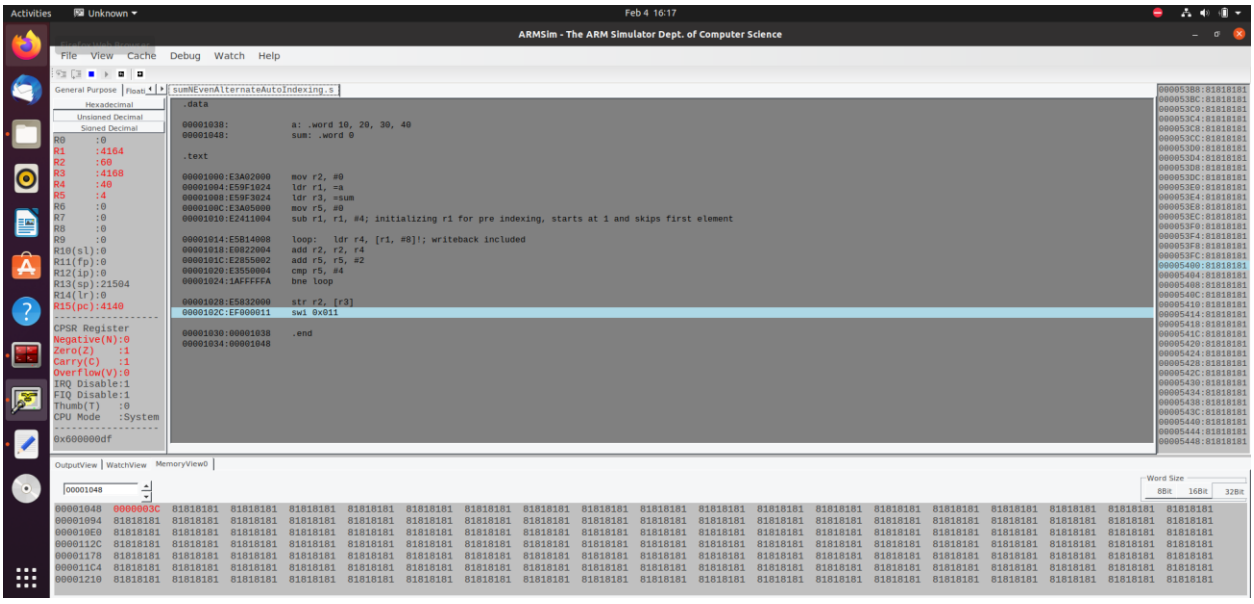
<Screenshots on the next page>

Screenshot of ArmSimulator of the Program Executed

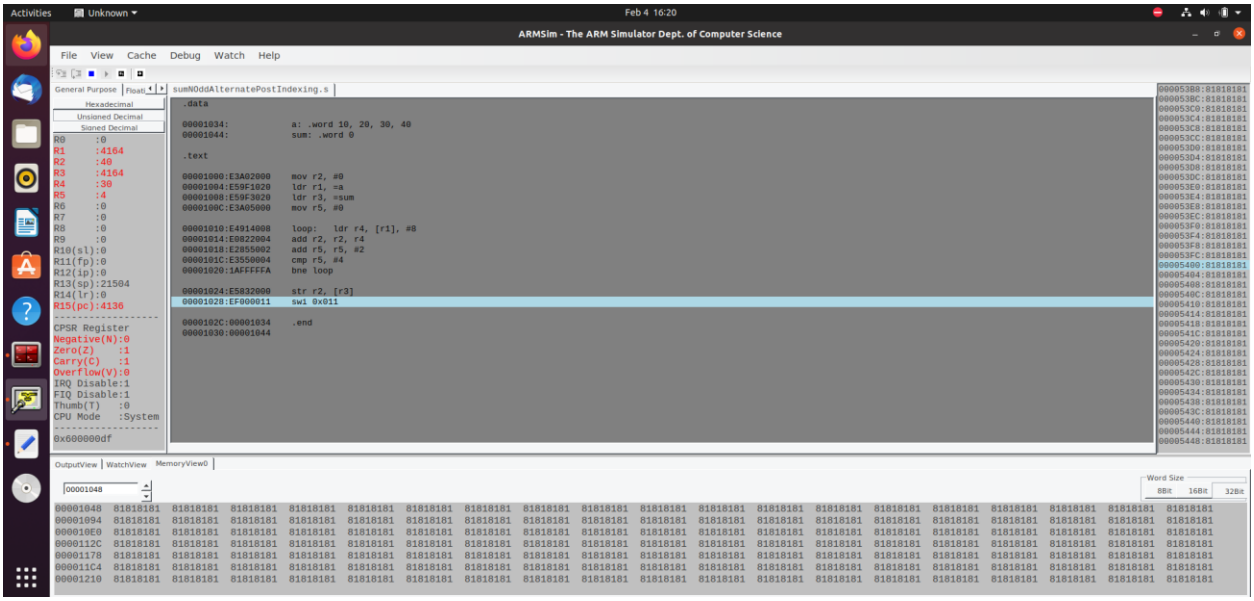
a.



b.



c.


Activities
Unknown
Feb 4 16:20
ARMSim - The ARM Simulator Dept. of Computer Science
File View Cache Debug Watch Help
General Purpose
Float
sumNOddAlternatePostIndexing.s
Hexadecimal
Unsigned Decimal
Signed Decimal
R0 :0
R1 :4164
R2 :40
R3 :4164
R4 :30
R5 :4
R6 :0
R7 :0
R8 :0
R9 :0
R10(sl):0
R11(fp):0
R12(ip):0
R13(sp):21504
R14(lr):0
R15(pc):4136
CPSR Register
Negative(N):0
Zero(Z) :1
Carry(C) :1
Overflow(V):0
IRQ Disable:1
FIQ Disable:1
Thumb(T) :0
CPU Mode :System
0x600000df
.data
00001034: a: .word 10, 20, 30, 40
00001044: sum: .word 0
.text
00001000:E3A02000 mov r2, #0
00001004:E59F1020 ldr r1, =a
00001008:E59F3020 ldr r3, =sum
0000100C:E3A05000 mov r5, #0
00001010:E4914008 loop: ldr r4, [r1], #8
00001014:E0822004 add r2, r2, r4
00001018:E2855002 add r5, r5, #2
0000101C:E3550004 cmp r5, #4
00001020:1AFFFFFA bne loop
00001024:E5832000 str r2, [r3]
00001028:EF000011 swi 0x011
0000102C:00001034 .end
00001030:00001044
OutputView
WatchView
MemoryView0
00001048
Word Size
8Bit
16Bit
32Bit
00001048 81818181
00001094 81818181
000010E0 81818181
0000112C 81818181
00001178 81818181
000011C4 81818181
00001210 81818181