Department of Electrical Engineering, IIT Bombay

EE 204 Analog Electronics
Mid-semester Examination
21:30 to 23:30 hrs.

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22B3936

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Maximum marks: 50

Answer all questions

1. BJT shown in Fig. 1 is used to drive the LED. To operate this transistor at the edge of saturation, the voltage between the base and collector (V_{BC}) >400 mV. Collector current I_c is given by the equation $I_c = I_s e^{V_{BE}/V_T}$, where I_s is the reverse saturation current, V_{BE} is the base-to-emitter voltage and V_T is the thermal voltage. What value should R_B be raised to TURN OFF the LED? [5]
   Given: $I_s = 5 \times 10^{-16} A$, $V_T = 26$ mV, $\beta = 100$

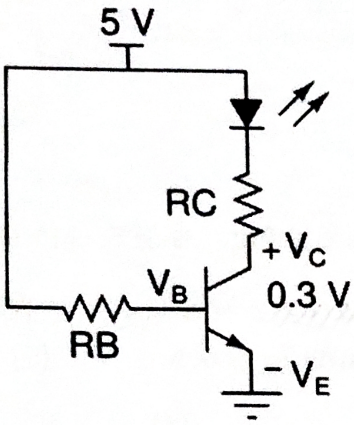


Fig. 1

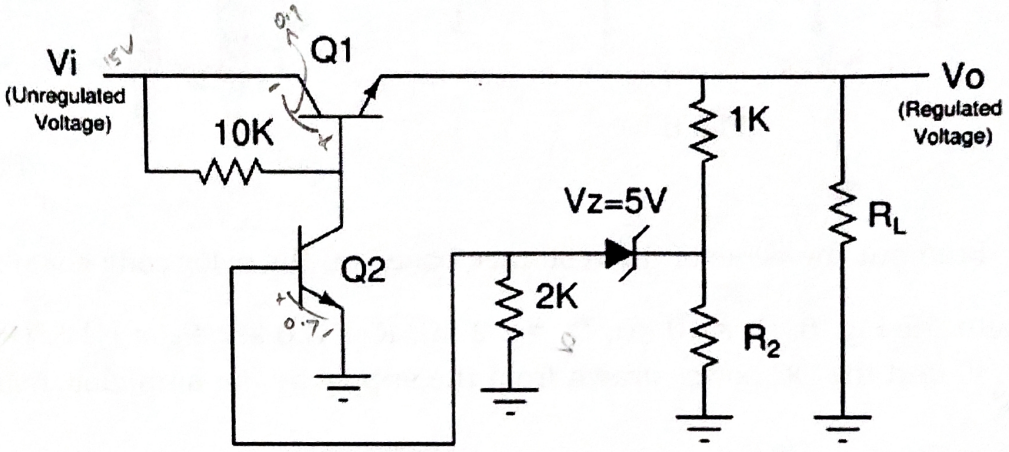


Fig. 2

2. In the voltage regulator shown in the Fig. 2, V_i is the unregulated input voltage of (15V ±20%) and V_o is the regulated output voltage. Assume V_{BE} of each transistor to be 0.7 V and β to be very high ($\simeq \infty$). If the regulated output voltage V_o is 9 V, then find the value of R_2. [5]

3. In the circuits shown in Figs. 3 & 4, Find out the value of C if the time constant is 5 ms. [1+1]

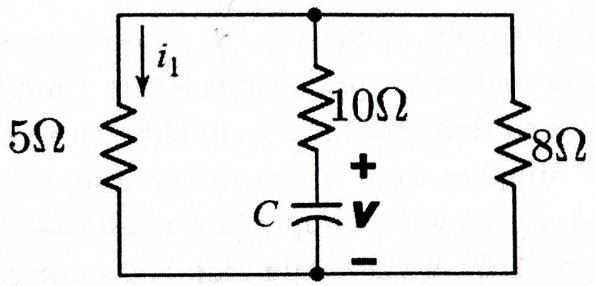


Fig. 3

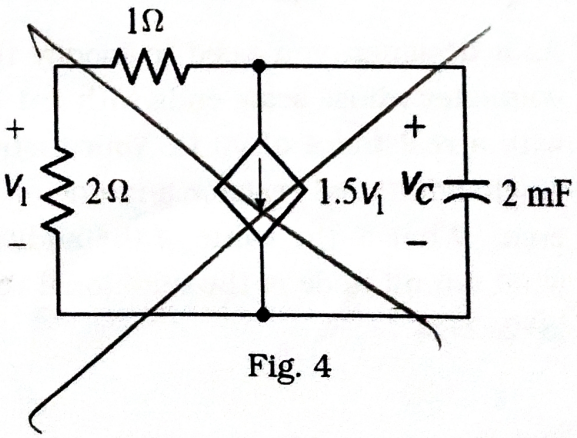


Fig. 4

4. Draw the small signal model of the two-stage CMOS op amp circuit configuration shown in the Fig. 5. [3+3]

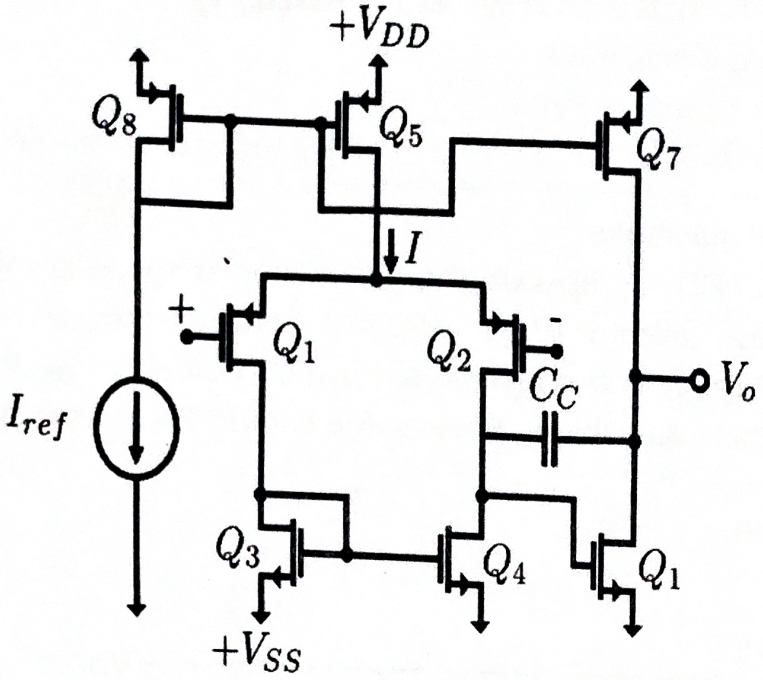


Fig. 5

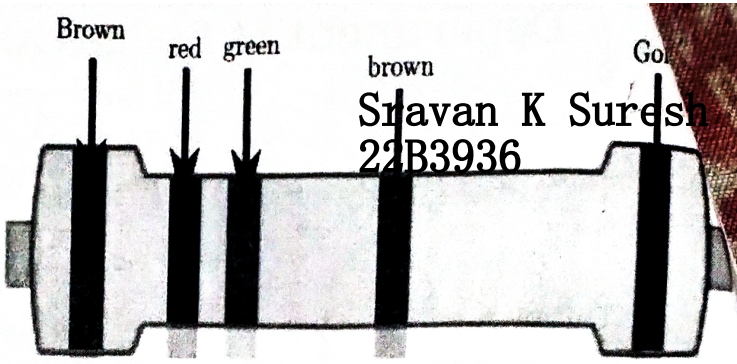


Fig. 6

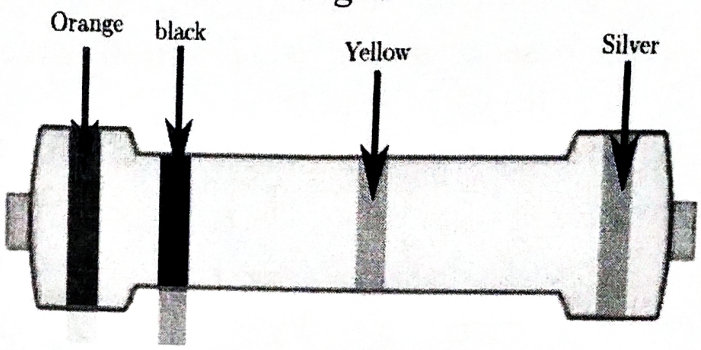


Fig. 7

5. Find out the value of the resitance based on the color code given in the Figs. 6 & 7. [1+1]

6. In the Fig. 8; R_1 = 10 kΩ; R_2 = 2.2 kΩ; R_c = 3.6 kΩ; R_E = 1.1 kΩ ~~= 3.6 kΩ~~; and V_{CC} = ± 10 V, find the DC power drawn from the supply by the amplifier. Assume $I_B \simeq 0$ A. [5]

V_{BE}=0.7V

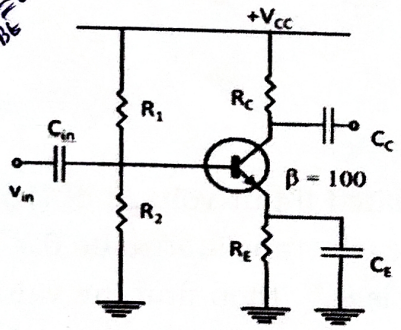


Fig. 8

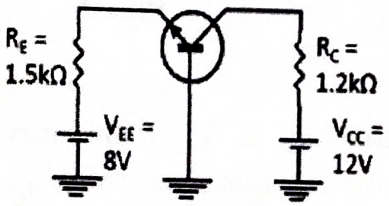
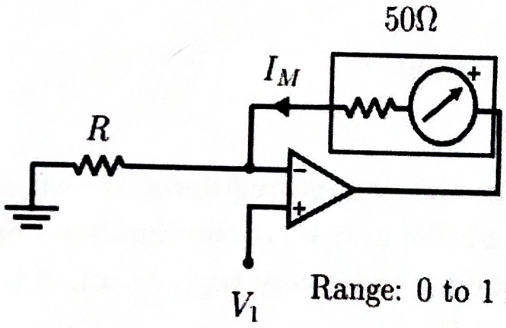


Fig. 9



Range: 0 to 1 mA

Fig. 10

7. For the common base circuit shown in Fig. 9, determine I_C and V_{CB}. Assume V_{BE} = 0.7V, and $I_B \simeq 0A$. $V_{EE} = -8V$. [2.5+2.5]

8. As a designer, you need to modify the circuit as shown in the Fig. 10 as a centre-zero voltmeter whose scale ends with ± 1 V. The meter movement provided is a 0 to 1 mA unit with a resistance of 50 Ω. Your instructor suggests that you have to modify with only a single additional resistor and one of the ±10 V supplies from which the op-amp is powered. What is the value of the additional resistor? To what supply is it connected? To what circuit node is the additional resistor connected? What is the required value of R? [3+2+2+3]

9. The Op amps in the circuit shown in the Fig. 11 are ideal. The input signals are V_{s1} = 3+0.2 sin (300t) V and V_{s2} = -2 + 0.22 sin (300t) V. Find the average value of the voltage in volts. [5]

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Assuming the op amps are ideal shown in the Fig. 12, find out the output voltage V_o. [5]

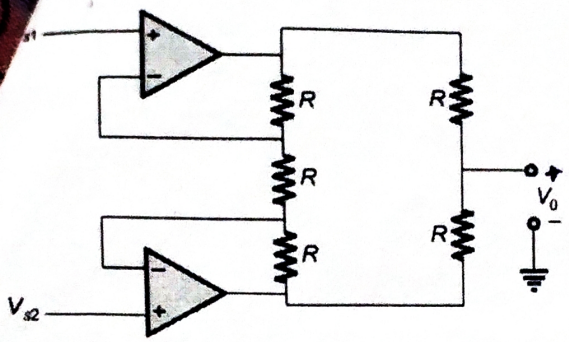

Fig. 11

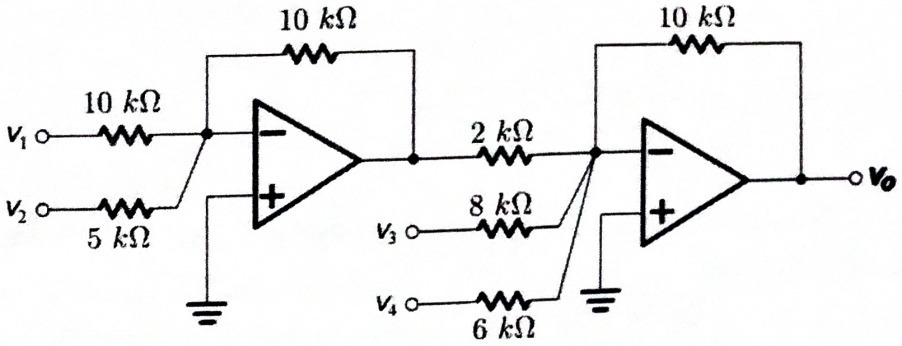

Fig. 12