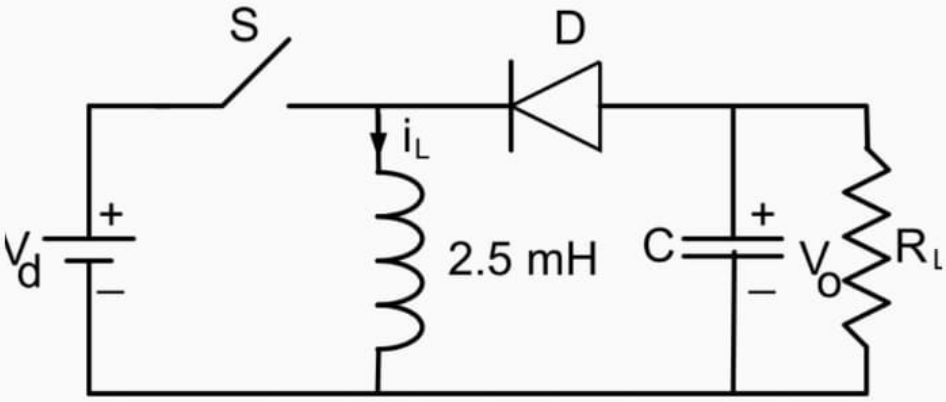
Roll No.: [22b3936] Marks: 5.0

Question 1.

For the dc to dc converter shown in the Figure, the switch, S is operated with a a switching frequency of 5 kHz. The value of the inductor, L is 2.5 mH. Input voltage, $V_d$ of the converter is maintained at 100 V. The output voltage, $V_0$ is maintained at a value of -150 V while a load resistance, $R_L$= 500 Ω is connected to the output terminals of the converter. Determine the duty cycle, δ with which the switch, S is operating. Assume that the output voltage of the regulator is ripple free as the output filter capacitor, C is significantly large.

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CHAT

Roll No.: [22b3936] Marks: 10.0

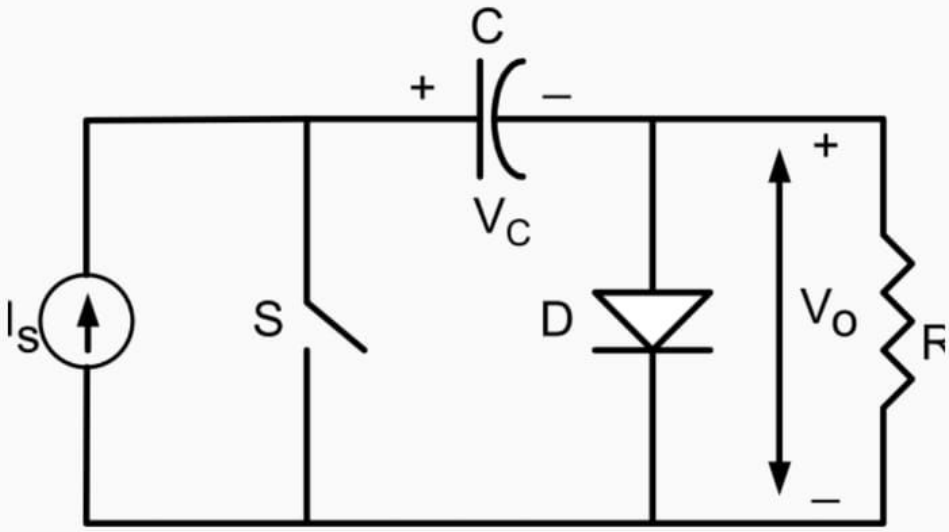
Question 2.

The input to the dc to dc converter circuit shown in the Figure is a current source having a constant magnitude, $I_s$, and the converter is feeding a load, R. The switch, S is operated with a period, T and a duty cycle, δ. You can consider that the capacitor, C is large enough, so that the voltage across it can be assumed to be ripple free. Once the circuit has attained steady state of operation determine the following as a function of $I_s$, δ and R:

1. Average capacitor voltage, $V_C$. (7 marks)

2. Average output voltage, $V_0$. (3 marks)

[Hint: This circuit was not discussed during lecture sessions. Apply the golden rules of steady state circuit analysis, and you will arrive at the expressions asked for]

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Roll No.: [22b3936] Marks: 5.0

Question 3.

Consider the converter circuit shown in the Figure - A. The switches $S_1$ and $S_2$ are turned on and off simultaneously with the switching, frequency $f_s$ ($=\frac{1}{T}$), and with a duty cycle of *d* as shown in Figure - B. Assume that the current through the inductor is continuous. 1) Derive the expression of the output voltage, $V_0$ in terms of the given parameters when the circuit is operating at steady state. 2) Comment on the functionality of the circuit. (4+0.5+0.5 marks)

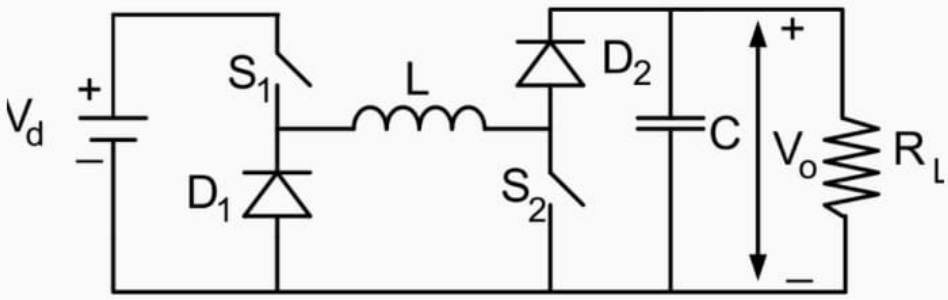


Figure A

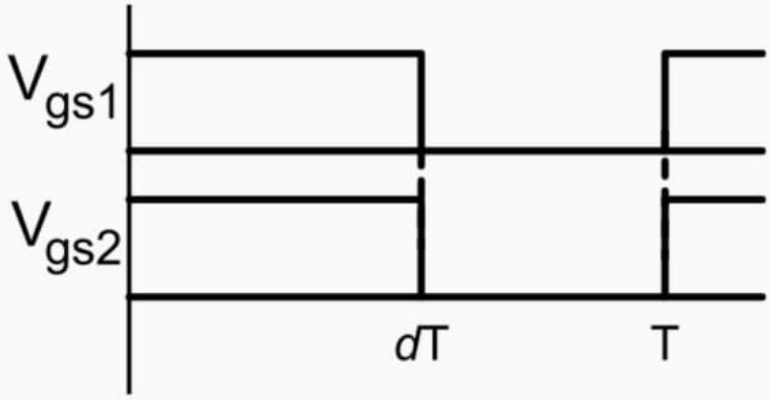


Figure B

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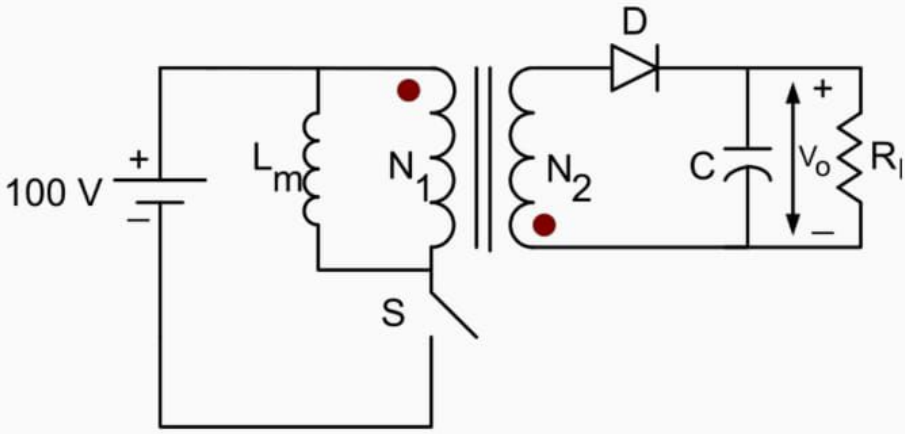
Roll No.: [22b3936] Marks: 10.0

Question 4.

Consider the flyback converter circuit shown in the figure. The switching frequency is maintained at 50 kHz, and the switch, S is operated with a duty cycle, δ = 0.25. The magnetizing inductance of the transformer, $L_m$ = 250 μH if seen from the side of the transformer which has $N_1$ turns. The turns ratio of the transformer ($N_1/N_2$) is 2. The output voltage of the converter is found to be 80 V. Find the load resistance, $R_L$. Assume the value of the capacitor, C is large, and hence ripple in the output voltage can be neglected.

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CHAT

Roll No.: [22b3936] Marks: 10.0

Question 5.

**Part A:** A single phase full bridge inverter circuit shown in Figure A is to be operated to produce a square wave output voltage, $v_o$ at a frequency of 1/T Hz. Considering the load to be **capacitive** (i.e. when the load is fed by a sinusoidal source having a frequency of 1/T Hz, the load current leads the sinusoidal source voltage by a certain angle once steady state is reached). Plot the following waveforms for a period, T, when the circuit has attained steady state (i.e. once the dc component of the load current has become zero):

i) Gating pulses for the switches S1 to S4. (1 mark)

ii) Output voltage vo across the load indicating its magnitude in terms of $V_d$. (1 mark)

iii) Approximate waveform of the output current, $i_o$. (1 mark)

iv) Mark on $i_o$ that you have drawn in iii), the devices that are conducting at every instant over the period, T. (2 marks)

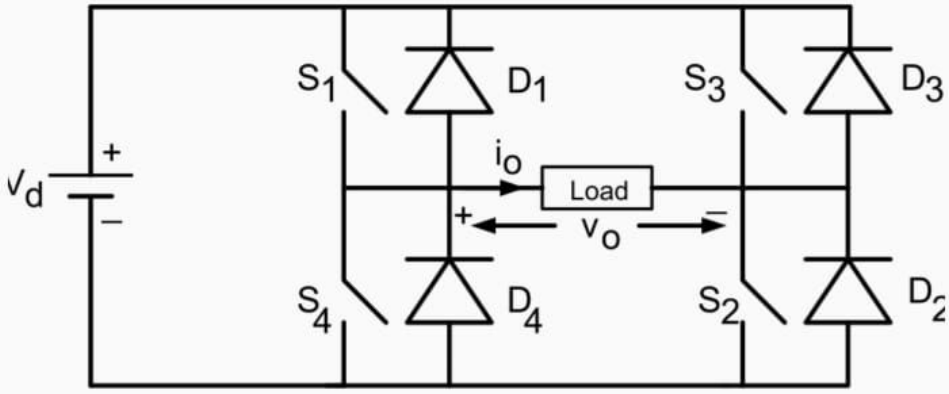


Figure A

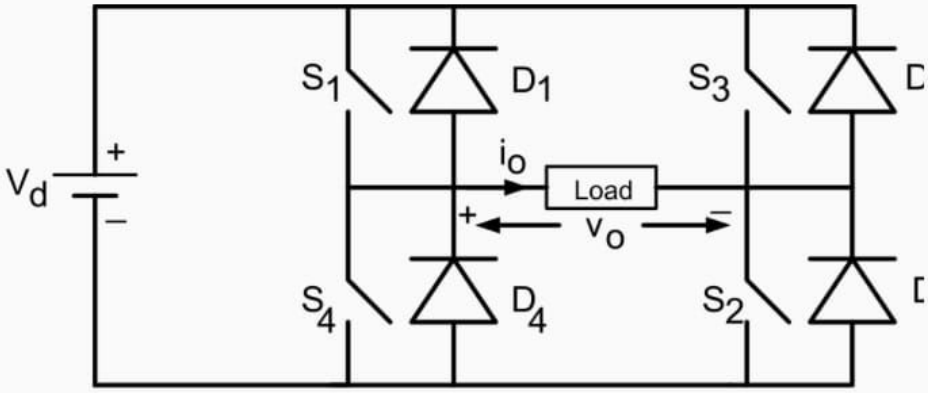


Figure A

**Part B:** Now consider that the inverter of Figure B is feeding an R-L load. Plot **(along with the given waveforms of $v_o$)** the gating pulses for the switches $S_1$ to $S_4$ of the inverter (Figure A) if the output voltage waveform, $v_o$, to be obtained is:

i) as shown in Figure B. (3 marks)

ii) as shown in Figure C. (2 marks)

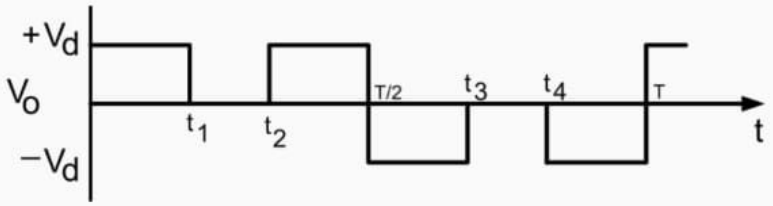


Figure B

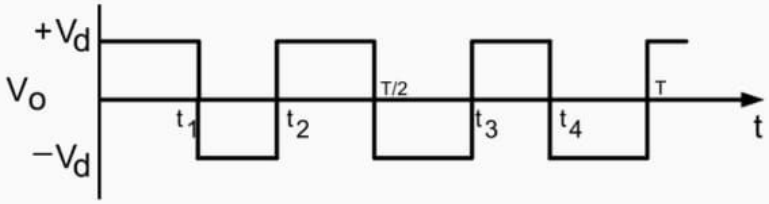


Figure C

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The three phase inverter shown in the Figure is to be operated as a square wave inverter such that the fundamental component of $v_{BC}$ lags that of $v_{AB}$ by $120^\circ$ and fundamental component of $v_{CA}$ lags that of $v_{BC}$ by $120^\circ$ while gating pulse for each device is provided for $180^\circ$. The input dc voltage for the inverter, $V_d$ is 600 V (two dc voltage sources of magnitude 300 V each are connected in series having their connecting point at 'O').

a) Plot the gating pulses for the six switches, $S_1$ to $S_6$ along with $v_{Ao}, v_{Bo}, v_{AB}, v_{An}$ when $\mathbf{Z_a}$ = (10 + j0) Ω, $\mathbf{Z_b}$ = (20 + j0) Ω, $\mathbf{Z_c}$ = (20 + j0) Ω and the switch, **MS is closed**. Comment on the presence/absence of third harmonic component in $v_{AB}$ and $v_{An}$ giving proper justification. (3 marks)

b) Plot the gating pulses for the six switches, S1 to S6 along with $v_{Ao}, v_{Bo}, v_{AB}, v_{An}$ when $\mathbf{Z_a}$ = (10 + j0) Ω, $\mathbf{Z_b}$ = (20 + j0) Ω, $\mathbf{Z_c}$ = (20 + j0) Ω and the switch, **MS is open**. Comment on the presence/absence of third harmonic component in vAB and vAn giving proper justification. (7 marks)