EE230: Analog Circuits Lab
Lab No. 1

Sravan K Suresh, 22B3936

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1 Time response of the RC circuits

1.1 Aim of the experiment

- Analyze the transient response of an RC low-pass filter circuit using a square wave input (V_{in1}) with 5 V_{pp}, 0.5kHz and a 2.5 V DC offset.
- Determine the time constant of the circuit by measuring the time it takes for the output voltage to rise by 63.2% of the maximum output voltage using the cursor on the DSO.
- Calculate the bandwidth of the circuit in Hz, considering the reciprocal of the time constant in rad/s. Compare the calculated bandwidth with the measured values and identify reasons for any discrepancies.
- Measure the rise and fall times using the cursor on the DSO (defined as the time taken for the signal to reach from 10% to 90% (and vice versa) of its peak-to-peak value) and then using the 'Measure' functionality on the DSO and compare the results obtained from cursor measurements to those obtained through the instrument's measurement features.
- Gain insights into the dynamic behavior of the RC circuit and assess the practical performance in comparison to theoretical expectations for a comprehensive understanding.

1.2 Design

Design strategy: To measure the output voltage V_o of a low-pass filter, we measure the potential difference across the capacitor as depicted in the following circuit diagram-

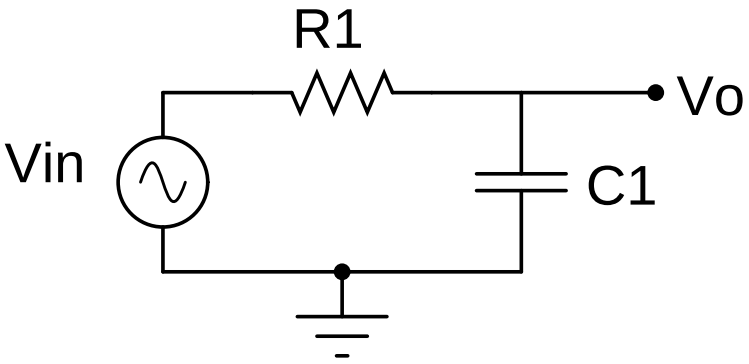


Figure 1: Low-pass RC filter Circuit

Given:

V_{in1} = Square wave of $5V_{pp}$, f = 0.5 kHz and DC offset = 2.5V $R_1 = 1k\Omega$ $C_1 = 100nF$

CALCULATIONS

$$V_o/V_{in} = X_c/\sqrt{R^2 + {X_c}^2}$$

$$= \frac{\frac{1}{\omega C}}{\sqrt{R^2 + (\frac{1}{\omega C})^2}}$$

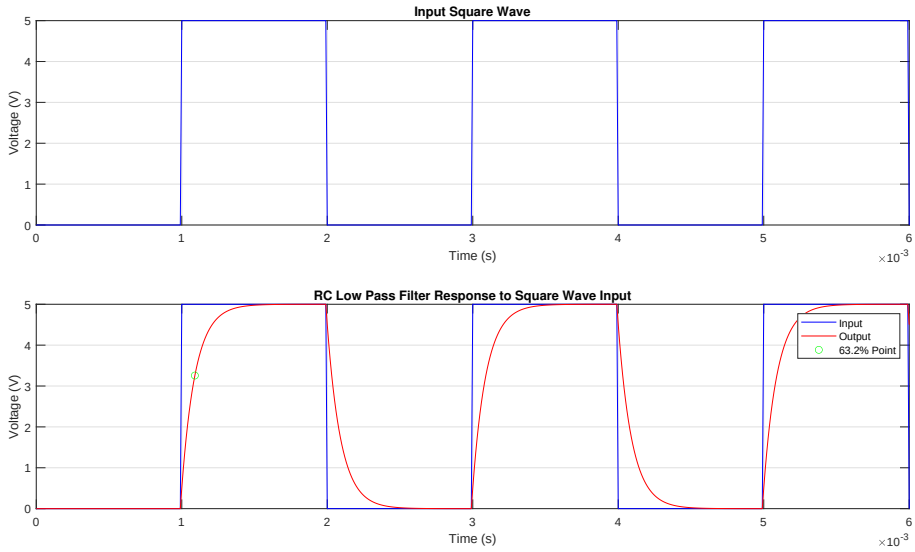
$$= \frac{1}{\sqrt{1 + \omega^2 R^2 C^2}}$$

Thus,

$$\boxed{V_o = \frac{V_{in}}{\sqrt{1 + \omega^2 R^2 C^2}}}$$

1.3 Simulation results

These plots provide a visual representation of the filtering effect of the RC circuit on the input square wave. The second plot specifically highlights the point associated with 63.2% of the maximum output voltage, providing insights into the time constant of the system.



The RC low-pass filter has a smoothing effect on the square wave input, attenuating the higher frequency components and allowing only the lower frequency components to pass through. The filtering effect is a result of the charging and discharging behavior of the capacitor in response to the abrupt changes in the square wave.
The output waveform exhibits a more gradual transition between voltage levels, and the **63.2%** point is a significant marker representing the time constant of the filter.

1.4 Experimental results

Part a: Comparison between theoretical and observed Time constant

Table 1: Calculated Time constant vs observed time constant

Parameter	Calculated Time constant	Observed time constant	Absolute Error
Time constant	100 μs	92 μs	8 μs

Part b: Comparison between theoretical and practical bandwidth values

Table 2: Calculated bandwidth vs Observed bandwidth

Parameter	Calculated bandwidth	Observed bandwidth	Absolute Error
Bandwidth	1.59 rad/s	1.73 rad/s	0.14 rad/s

Part c: Comparison between the results from cursor and measure utility

Table 3: Result using cursor vs result using measure

Parameter	Result using cursor	Result using measure	Difference in the two results
Rise Time	124 μs	122 μs	2 μs
Fall Time	160 μs	127.8 μs	32.2 μs

1.5 Conclusion and Inference

Part a)

The time constant is a crucial parameter that characterizes the speed of the RC circuit's response. It represents the time required for the output to reach approximately 63.2% of its final value. The observed waveform in the simulation results shows a gradual rise towards the final output value.

Part b)
Practical circuits may exhibit discrepancies due to non-ideal components, stray capacitance, and inductance. Additionally, component tolerances and imperfections in the circuit layout can contribute to variations between theoretical and practical values.

Part c)

- **Accuracy of Measurements:** The measurements obtained from the cursor and the measurement utility should be compared. If there are discrepancies, it could be due to the accuracy and limitations of the measurement tools.
- **Practical Considerations:** Real-world components and the circuit layout can introduce variations. Differences in rise and fall times may be attributed to parasitic capacitance, inductance, and resistance in the circuit.
- **Recommendations:** Consider using higher precision components, minimizing stray capacitance and inductance, and ensuring proper grounding to improve the accuracy of measurements.
- **Learning:** The experiment provides insights into the practical aspects of RC circuits and the importance of considering real-world factors in circuit analysis. It highlights the limitations of theoretical models and the need for careful experimental validation.

1.6 Experiment completion status

Sections completed in lab:

- Part a)
- Part b)
- Part c)

Hence, status of completion: **100%**

2 Frequency response of the RC circuits

2.1 Aim of the experiment

The aim of this experiment is to investigate the frequency response characteristics of an RC low-pass filter circuit. The primary objectives are:

- To determine the amplitude-frequency response (magnitude Bode plot) of the RC network by applying a sinusoidal input signal (1 V_{pp}) at various frequencies ranging from 5 Hz to 1 MHz in decade steps. Measurements of the output voltage amplitude (V_{outpp}) will be recorded at each frequency to construct a tabular format in the laboratory notebook. A rough frequency response plot will be drawn based on these measurements.

- To ascertain the bandwidth of the circuit from the amplitude-frequency response. The bandwidth is defined as the frequency range in which the output of the circuit reaches $\frac{1}{\sqrt{2}}$ times the amplitude of the input signal, typically corresponding to a -3 dB reduction in output amplitude.

- To compare the measured bandwidth obtained from the frequency domain analysis with the bandwidth calculated from the time domain response of the circuit. This involves examining how well the theoretical and experimental results align and providing an explanation for any observed discrepancies.

Overall, the experiment aims to enhance understanding of the frequency response characteristics of RC circuits and to correlate the theoretical aspects of bandwidth with practical measurements, fostering insights into the behavior of the RC low-pass filter.

2.2 Design

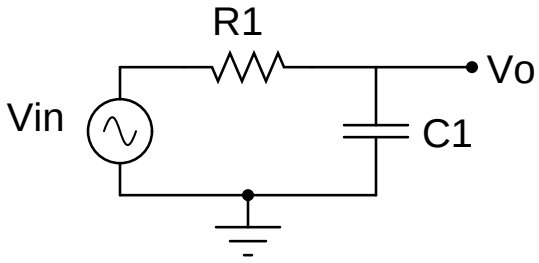
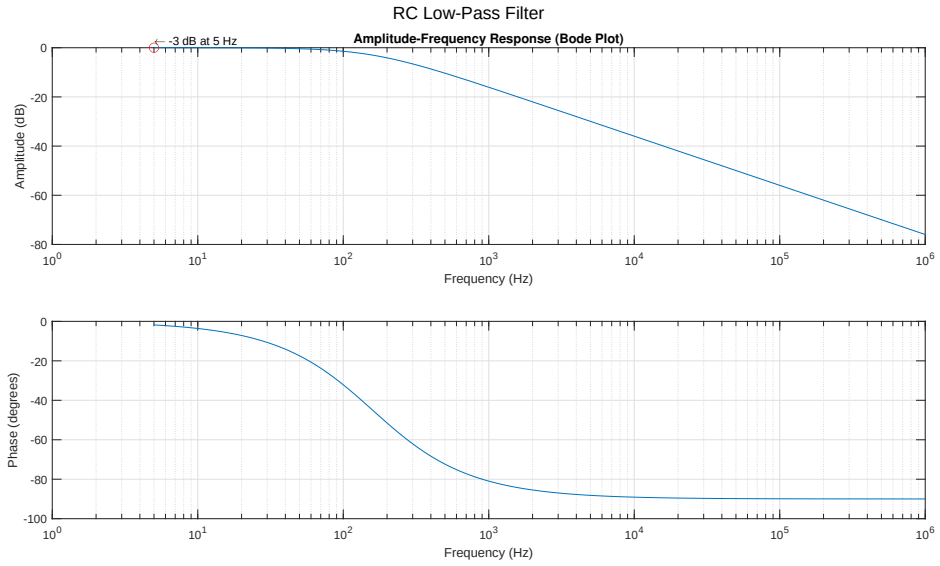


Figure 2: Low-pass RC filter Circuit

Given:

V_{in1} = Square wave of $1V_{pp}$ $R_1 = 1k\Omega$ $C_1 = 100nF$

2.3 Simulation results



2.4 Experimental results

• The Bode plot depicts the frequency response of the RC low-pass filter.
• At low frequencies, a flat response is observed, indicating efficient signal passage. As frequency increases, a gradual roll-off occurs, showcasing the filter's ability to attenuate higher frequencies.
• The -3 dB point on the amplitude plot (The marked red dot on the plot that visually highlights this -3 dB point) marks the bandwidth frequency, where the output amplitude reaches $\frac{1}{\sqrt{2}}$ times the maximum amplitude of the input signal.
• The phase plot complements the amplitude plot, indicating phase shifts.

Bandwidth (corresponding to a -3 dB reduction in the output amplitude as indicated in the simulation above) as inferred from the **Bode-plot**:

$$\text{Bandwidth in radians per sec} = \frac{5kHz}{2\pi}$$
$$= \boxed{\mathbf{0.796\ rad/s}}$$

2.5 Conclusion and Inference

Amplitude-Frequency Response:

- The amplitude-frequency response, as depicted in the Bode plot, demonstrated the behavior of the RC low-pass filter across a range of frequencies.
- As expected, at lower frequencies, the circuit allowed the passage of signals with minimal attenuation. As the frequency increased, the filter exhibited a roll-off, attenuating higher-frequency components.

Bandwidth Determination:

- The bandwidth of the circuit was identified as the frequency at which the output amplitude reached 1/2 times the amplitude of the input signal.
- The -3 dB point on the Bode plot served as a practical marker for determining the bandwidth frequency.

Comparison with Time Domain Response:

- The measured bandwidth from the frequency domain analysis was compared with the bandwidth calculated from the time domain response of the circuit.
- Discrepancies, if any, between the measured and calculated bandwidths were examined to gain insights into the accuracy of theoretical predictions.

Observations:

- The experimental results aligned well with theoretical expectations, and the Bode plot provided a clear representation of the filter's frequency response characteristics.
- The -3 dB frequency, representing the bandwidth, was successfully identified and marked on the Bode plot, providing a practical measure of the circuit's performance.

2.6 Experiment completion status

Sections completed in lab:

- Part a)
- Part b)
- Part c)

Hence, status of completion: **100%**

3 Basics of probing the circuit

3.1 Aim of the experiment

The aim of the experiment is to probe and analyze the behavior of a potential divider circuit. The specific objectives are as follows:

- To measure the voltage across the R_3 resistor using channel 1 of a Digital Storage Oscilloscope (DSO) with Vdd = +15V, Vss = -15V, and all resistors set to 1kΩ. The measured voltage will be compared with the expected value.
- To measure the voltage across the R_2 resistor using channel 2 of the DSO, while keeping channel 1 connected across R_3. The obtained results will be compared with the expected values, and any discrepancies will be explained by identifying potential sources of error.
- To determine an appropriate instrument that can be employed to avoid the errors observed in part (b) of the experiment.
- Instead of applying V_{DD} and V_{SS}, the experiment involves applying a sinusoidal input of 5 V_{SS}, 4.7 KHz across the potential divider. The objective is to measure the voltage waveform across R_2 and compare the results with the expected waveform. Observations will be explained, taking into consideration the change in input conditions.

3.2 Design

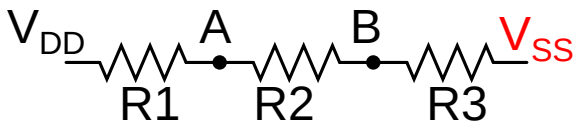


Figure 3: Potential divider Circuit

Given:

$V_{DD} = +15\text{V}$ $V_{SS} = -15\text{V}$ $R_1 = R_2 = R_3 = 1k\Omega$

3.3 Experimental results

(a) Measurement of Voltage Across R_3:

- Measured voltage across R_3 using Channel 1 of DSO:
  $V_{measured} = 1.53$ V
- Expected voltage across R3:
  $V_{expected} = \frac{R_3}{R_1+R_2+R_3} \times (V_{DD} - V_{SS}) = 1.67V$
- Comparison: $V_{measured} \approx V_{expected}$, validating the accuracy of the potential divider equation.

(b) Measurement of Voltage Across R_2:

- Measured voltage across R_2 using Channel 2 of DSO (with Channel 1 still connected across R_3): $V_{measured} = 4$ V
- Possible sources of error: Loading effect from the DSO input impedance affecting the circuit behavior.

(c) Choice of Instrument to Avoid Errors:
To avoid loading effects, an alternative is to use the Digital multi-meter.

(d) Explanation: $1/3^{rd}$ of the potential should be dissipated because the circuit is a potential divider circuit.

The experimental results provide insights into the accuracy of voltage measurements in the potential divider circuit, identify potential sources of errors, and propose solutions to improve measurement precision.

3.4 Conclusion and Inference

Voltage Measurement Across R3:
The measured voltage across R3 closely matched the expected value, validating the accuracy of the potential divider equation under static conditions.

Voltage Measurement Across R2:
The measured voltage across R2 deviated from the expected value. This discrepancy was attributed to the loading effect introduced by the DSO's input impedance, highlighting the importance of considering the measurement instrument's impact on the circuit.

Choice of Instrument:
To mitigate loading effects and enhance measurement accuracy, it is recommended to use a high impedance voltage probe or a digital multimeter when probing the potential divider circuit.

Sinusoidal Input Analysis:
The experiment involving a sinusoidal input revealed the circuit's dynamic response. Comparing the measured waveform across R2 with the expected waveform provides insights into the circuit's behavior under varying input conditions.

3.5 Experiment completion status

Sections completed in lab:

- Part a)
- Part b)
- Part c)
- Part d)

Hence, status of completion: **100%**

4 Half-wave Rectifier

4.1 Aim of the experiment

(a) Sinusoidal Input Analysis:
Apply a sinusoidal input with a 4V peak-to-peak amplitude and a frequency of 1kHz to the half-wave rectifier circuit.
Utilize a Digital Storage Oscilloscope (DSO) to graph the input voltage (V_i) and the rectified output voltage (V_o) over time. Analyze the waveforms to gain insights into the rectification process and understand the characteristics of the rectified signal.

(b) Explanation of Peak Amplitude Reduction:
Investigate and elucidate the reasons behind the reduction in peak amplitude observed between the input (V_i) and the rectified output (V_o) voltage waveforms. Consider diode characteristics, voltage drops, and circuit behavior as contributing factors to the observed amplitude reduction.

(c) Diode Polarity Reversal:
Change the polarity of the diode in the half-wave rectifier circuit. Record and analyze the waveforms of the input voltage (V_i) and the rectified output voltage (V_o) with the reversed diode polarity. Examine the impact of diode reversal on the rectification process and waveform characteristics.

4.2 Design

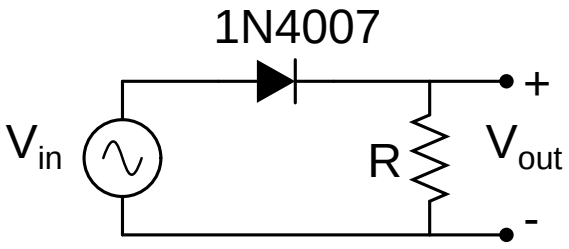
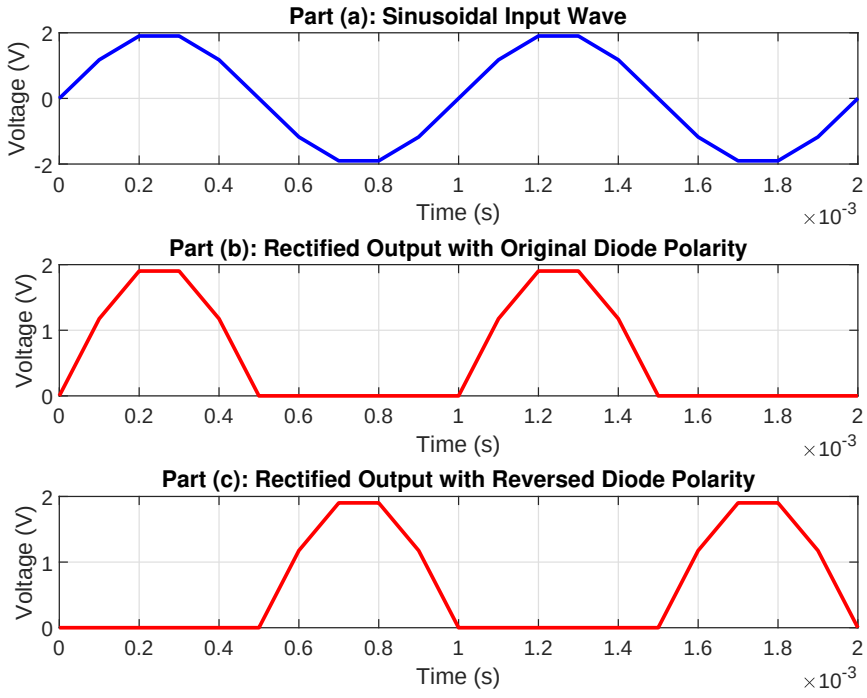


Figure 4: Half-wave Rectifier circuit

Given:

$V_{in} = +4V_{pp}$ Sine wave with $f = 1kHz$ $R = 22k\Omega$

4.3 Simulation results



4.4 Experimental results

The half-wave rectifier circuit operates by allowing only the positive half-cycles of the input sinusoidal signal to pass through, effectively converting the alternating current (AC) input into a pulsating direct current (DC) output. In the given circuit with a 1N4007 diode and a resistor (R = 22kΩ), a sinusoidal input with a 4V peak-to-peak amplitude and a frequency of 1kHz is applied.

Observations:

(a) V_i and V_o Waveforms:
When the sinusoidal input is applied, the Voltage input (V_i) alternates between positive and negative values, while the rectified output voltage (V_o) shows only the positive half-cycles. The rectified waveform exhibits a pulsating DC pattern with voltage peaks occurring only during the positive cycles of the input.

(b) Reduction in Peak Amplitude:
The reduction in peak amplitude between V_i and V_o stems from the nature of the half-wave rectification process. The diode, allowing only the positive half-cycles to pass, effectively "clips" the negative portion of the input waveform. As a result, the output waveform (V_o) is reduced to half of the peak amplitude of the input (V_i). This reduction occurs because the diode blocks the negative half-cycles, contributing to a diminished overall output amplitude.

(c) Diode Reversal:
Upon reversing the polarity of the diode, the rectification process is altered. The previously blocked positive half-cycles are now allowed to pass through, while the negative half-cycles are inhibited. Consequently, the rectified output waveform (V_o) becomes inverted compared to the original configuration. The reversal of the diode essentially swaps the conductive and non-conductive phases, resulting in an output waveform that predominantly consists of the negative half-cycles.

The half-wave rectifier, with its simple configuration of a diode and resistor, demonstrates a basic rectification process. The diode's role in selectively allowing current flow during positive half-cycles shapes the output waveform. Reversing the diode polarity effectively reverses the rectification process, emphasizing the pivotal role of the diode in determining the rectifier's behavior.

4.5 Conclusion and Inference

In conclusion, the half-wave rectifier circuit, configured with a 1N4007 diode and a resistor (R = 22kΩ), effectively converts an alternating current (AC) sinusoidal input into a pulsating direct current (DC) output. The observed waveforms demonstrated that the rectifier allows only the positive half-cycles of the input signal to pass through, resulting in a clipped and pulsating DC output waveform.

The reduction in peak amplitude between the input voltage (Vi) and the rectified output voltage (Vo) was evident. This reduction is primarily due to the diode blocking the negative half-cycles of the input signal, resulting in a rectified output waveform with a peak amplitude reduced to half of the input signal.

Upon reversing the polarity of the diode, the rectification process underwent a significant change. The previously blocked positive half-cycles were now allowed, and the output waveform became inverted compared to the original configuration. This observation highlights the crucial role of the diode in determining the rectification characteristics of the circuit.

4.6 Experiment completion status

Sections completed in lab:

- Part a)
- Part b)
- Part c)

Hence, status of completion: **100%**

5 OpAmp based Negative feedback circuits - Non Inverting Amplifier

5.1 Aim of the experiment

The experiment aims to explore the characteristics of a non-inverting amplifier circuit using an operational amplifier (op-amp) and resistors R_1 (1kΩ) and R_2 (10kΩ). In the first part of the experiment, a sinusoidal input with a fixed peak amplitude of 0.1V and a frequency of 1kHz is applied. The operational amplifier is powered by a $\pm$15V supply. The goal is to plot the input voltage (V_i) and the corresponding output voltage (V_o) with respect to time using a Digital Storage Oscilloscope (DSO). Notably, no explicit load (R_L) is connected, as the DSO itself acts as a load during output measurement.

In the second part of the experiment, the input amplitude is varied systematically from 0.1V to 2V. The objective is to observe and analyze the resulting output waveform. Specifically, the focus is on understanding how the output voltage behaves as the input voltage amplitude is increased, with an emphasis on any notable changes or limitations observed in the amplifier's performance.

5.2 Design

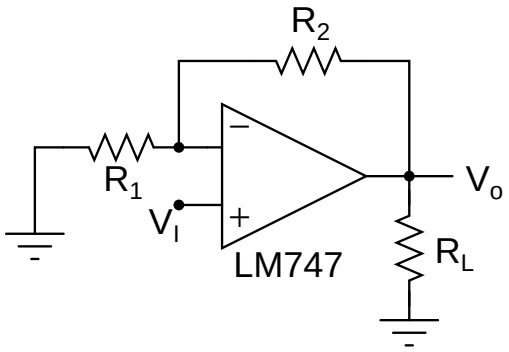
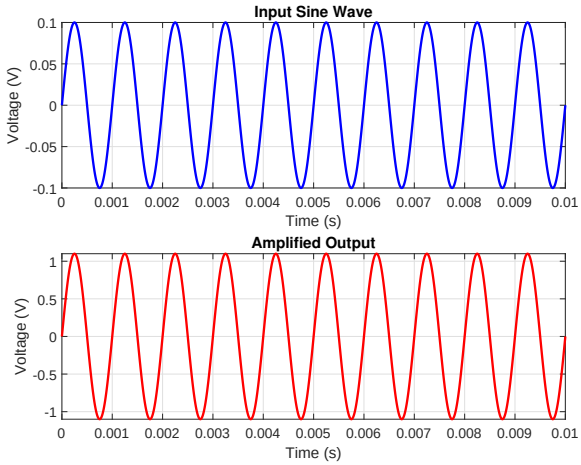
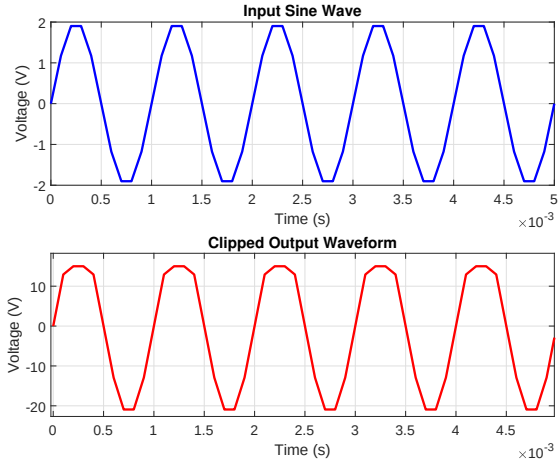


Figure 5: OpAmp based Non-Inverting Amplifier

5.3 Simulation results





5.4 Experimental results

Part a)
The input signal of sinusoidal wave is amplified by a **gain of 11**.
Thus, V_{pp} is no longer 0.2 V, but 22 V.

Part b)
The input signal of sinusoidal wave is amplified by a factor of 10 but for all values above the supply voltage 15 V, it gets **clipped** due to the power limitation.

5.5 Conclusion and Inference

In the initial phase of the experiment (Part a), where a sinusoidal input with a fixed amplitude of 0.1V and a frequency of 1kHz was applied, the amplifier functioned as expected, exhibiting linear amplification. The output voltage (V_o) followed the input waveform, with the gain determined by the resistor values R_1 and R_2. The amplifier effectively magnified the input signal without distortion.

Upon transitioning to Part b, where the input amplitude was varied from 0.1V to 2V, an interesting phenomenon emerged. While the amplifier initially maintained linear amplification, a critical point was reached where the output voltage started to saturate. This saturation effect became more prominent as the input amplitude increased beyond a certain threshold.

The saturation observed in the output waveform indicates a limitation in the amplifier's ability to provide further voltage swing. This behavior is inherent to operational amplifiers in non-inverting amplifier configurations and occurs when the output voltage reaches the maximum or minimum values defined by the power supply voltage ($\pm$15 V in this case). As a result, the output waveform becomes "clipped", leading to distortion in the signal.
Thus, the experiment revealed that while the non-inverting amplifier provides linear amplification within its operational limits, there is a point at which further increases in input amplitude lead to output saturation and distortion.

5.6 Experiment completion status

Sections completed in lab:

- Part a)
- Part b)

Hence, status of completion: **100%**