EE214 Digital Circuits Laboratory

Quiz-1

Department of Electrical Engineering, IIT Bombay

Name: Duration: 60 minutes

Roll No.: September 5, 2023 Maximum marks: 20 + 5 bonus

Instructions:

1. Use structural modelling i.e., instantiate components and use port mapping to connect them.
2. All responses must be written in this sheet and returned at end of exam.
3. Perform RTL simulation using the given testbench and tracefile.
4. **Download tracefiles from Moodle in first five minutes.**

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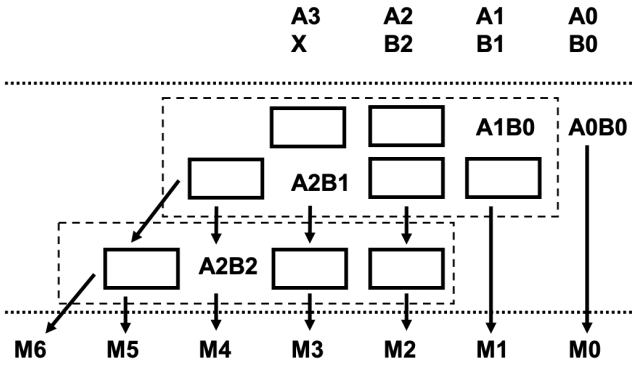
1. **Design of unsigned multiplier circuit [2 marks]**

   Design an unsigned multiplier circuit that multiples a 4-bit binary number (A3 A2 A1 A0) and a 3-bit binary number (B2 B1 B0). **Fill in the boxes in the left-panel** in Figure 1 below. Recall how multiplication is performed, using the example for decimal numbers (base-10) shown in right-panel below.




```
   3214
 × 4561
 -------
   3214
 19284X
 16070X
+12856X
 -------
 14659054
```

Figure 1: (Left) Fill in the blanks for bit-wise operations on the two binary numbers. (Right) Example of multiplication of two base-10 decimal numbers.

2. **VHDL description [12 marks]**

   i. Draw pen-paper design of the circuit on back side of this paper, using legible labels for each wire and same labels for the VHDL code. **(4 marks)**

   ii. Write VHDL description of the circuit that you have designed for the multiplier. Ensure that the input and output bit names match the notations in left-panel of Figure 1. **(8 marks)**

3. **Simulation [6 marks]**

   Simulate your design using the generic testbench. Use the tracefile and modify the testbench appropriately.

   Tracefile format: (<A3 A2 A1 A0 B2 B1 B0> <M6 M5 M4 M3 M2 M1 M0> 1111111)

   Download tracefile for multiplier from Moodle.

4. **BONUS [5 marks]**

   Note: No bonus marks if you do not adequately attempt all questions above. No partial marking in bonus question!!

   Design a 4-bit comparator to compare first 4 MSBs (i.e., M6 M5 M4 M3) with last 4 LSBs (i.e., M3 M2 M1 M0), that produces output Y0 = '1' if (M6 M5 M4 M3) > (M3 M2 M1 M0) else Y0 = '0'.

   Draw pen-paper design and describe your circuit design in VHDL.

   Simulate your design using the generic testbench to confirm the correctness of your description, using the tracefile provided to you. Modify the testbench given to you appropriately.

   Tracefile format: (<M6 M5 M4 M3 M2 M1 M0> <Y0> 1)

   Download tracefile for bonus question from Moodle.