Indian Institute of Technology Bombay

EE214 - Digital Circuits Lab

End Semester Exam(LA)

Timing: 3:30 PM - 6:30 PM **Date: October 29, 2022**

Exam Instructions:

1. Download the **Question Paper** and **Tracefile** containing **zip folder** from **Moodle** by **3:25 PM**.
2. Turn off your internet and keep your laptop in airplane mode after the download and switch off the mobile phone.
3. If anyone is caught using internet between the duration of exam **3:30 PM to 6:30 PM** action will be taken as per Institute policy.
4. **Password for the zip folder will be provided at 3:30 PM**.
5. You can switch on your internet at 6:30 PM only for uploading the files.
6. The **Final Design (VHDL Design files, qpf file and simulation results)** in a zip format only (file format: **Rollnumber_Name.zip**) should be uploaded in **Moodle** between **6:30 PM to 6:40 PM (sharp)**.
7. **Hard copy of the handwritten design** will be collected by your **respective TA** at **6:40 PM (sharp)**.
8. Demonstrate your **VHDL description** downloaded from moodle and **Working on board** to your **respective TA** for the overall design from 6.30 PM to 7 PM.
9. Create the Quartus project according to your assigned board model(10M25SAE144C8G/10M08SAE144C8G).

May the force be with you!

1 Feedback [2 Marks]

- List the topics and concepts you enjoyed learning during the lab sessions.
- What are the things you want to be changed or improved?

2 Problem Statement: Sequence Generator

- Generate the sequence **1 1 1 0**.
- Reset is asynchronous in nature i.e. reset effects the output sequence irrespective of the input clock arrival.
- On Reset, current sequence is interrupted and new sequence should start from the first '1'. Unused states should be mapped to one of the known state which is reset state.

2.1 VHDL Description and RTL Simulation [15 Marks]

- Write VHDL description in **Behavioral modeling** to generate the sequence **1 1 1 0**.
- **Structural modelling VHDL description will fetch 0 marks**.
- Verify the results with the given Tracefile.
- Tracefile format: ($< reset\ clock >$ $< output >$ $< Maskbit >$)

3 Problem Statement: FSM

- WEL internet server receives access request from 4 users (Admin, Professor, Researcher, Student). Server can be accessed by only one user at a time. But access can be requested by the multiple user at the same time. Now the users have certain priority assigned to them. Admin has highest priority. Priority order is Admin > Professor > Researcher > Student.
- Take initial state as idle. From idle state access will go to the requesting user. If no one is requesting access or the present user finishes using the server, it will simply come back to the idle state. No LED glows in idle state.
- When Admin is accessing the server **four LEDs** will glow. When Professor is accessing the server **three LEDs** will glow. Likewise for Researcher **two LEDs** and for Student **one LED** will glow. If the present user finishes using the server, it will simply go to the idle state.
- If a user is already using the server and a higher priority user requests access, control of the server will directly go to higher priority user from the lower priority user. Whenever access of the server go from lower priority user to higher priority user, **five LEDs** will glow for **3 sec** as a warning to the lower priority user and the access will automatically go to the higher priority user. If the higher priority user finishes using the server, it will go to the idle state before serving other requests. **Only use 50 MHz clock.**
- You can take four bits (b3 b2 b1 b0) to represent users requesting access. b3, b2, b1, b0 map to Admin, Professor, Researcher and Student respectively. b3 set to '1' means Admin is requesting access. Similarly b2 set to '1' means Professor is requesting access. b1 set to '1' means Researcher is requesting access. b0 set to '1' means Student is requesting access. For example:

b3 b2 b1 b0	Requesting User
0 0 0 0	ideal state
1 0 0 0	Admin
0 1 0 0	Professor
0 0 1 0	Researcher
0 0 0 1	Student
1 1 0 0	Admin and Professor
0 1 1 1	Professor, Researcher and Student

Likewise consider all the combinations.

3.1 Pen and Paper Design [13 Marks]

- Draw State Diagram.
- Input will be of 4 bits, representing who is requesting access. Properly define all the states, input and output as stated above.

3.2 VHDL Description and On Board Implementation[20 Marks]

- Describe your designed state diagram in VHDL using **Behavioural modelling only**. **Only use 50 MHz clock.**
- No tracefile needed. You will implement it on Xen10 Board.

- FPGA Pin No. for **50 MHz CLK** is **Pin 26**.

Switch	FPGA Pin no.	LED	FPGA Pin no.
SW 8	47	LED 8	60
SW 7	46	LED 7	59
SW 6	45	LED 6	58
SW 5	44	LED 5	57
SW 4	43	LED 4	56
SW 3	41	LED 3	54
SW 2	39	LED 2	52
SW 1	38	LED 1	50

Figure 1: Pin-mapping for on-board Switches and LED's