Lab Session 4: `BCD Adder` using pre-designed `components`

Sravan K Suresh
Roll Number: `22B3936`

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Overview of the Report

This report contains:

- Circuit Diagram of *BCD Adder*
- RTL Waveform Simulation of the function
- RTL Gates Map of the function
- OUTPUT verifying all tests successful

Problem Statement

Design a circuit to add two 4-bit BCD numbers. Input numbers are only in BCD (0 to 9) format. Follow the given steps to design the BCD adder -

- Design a 4-bit binary adder for initial addition.
- Design a logic circuit to detect if the initial sum greater is than 9.
- Design another 4-bit adder to add (0110) to the initial sum if it is greater than 9 or the carry is 1.

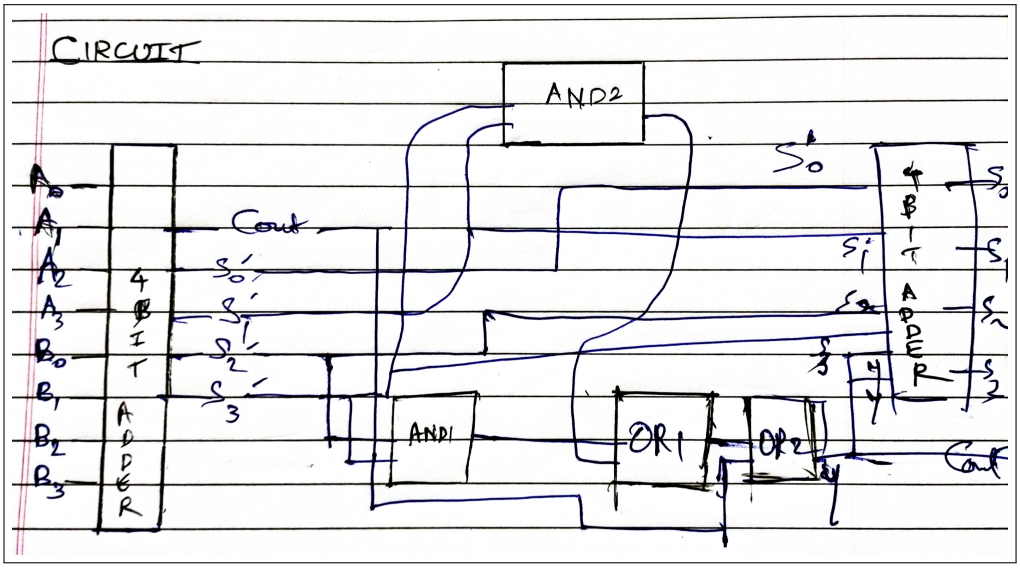
VHDL Description

VHDL description for the given problem statement:
Input (8-bit): $A_3A_2A_1A_0B_3B_2B_1B_0$
Output (5-bit): $Y_4Y_3Y_2Y_1Y_0$
Tracefile format: $< A_3A_2A_1A_0B_3B_2B_1B_0 >< Y_4Y_3Y_2Y_1Y_0 >< 11111 >$

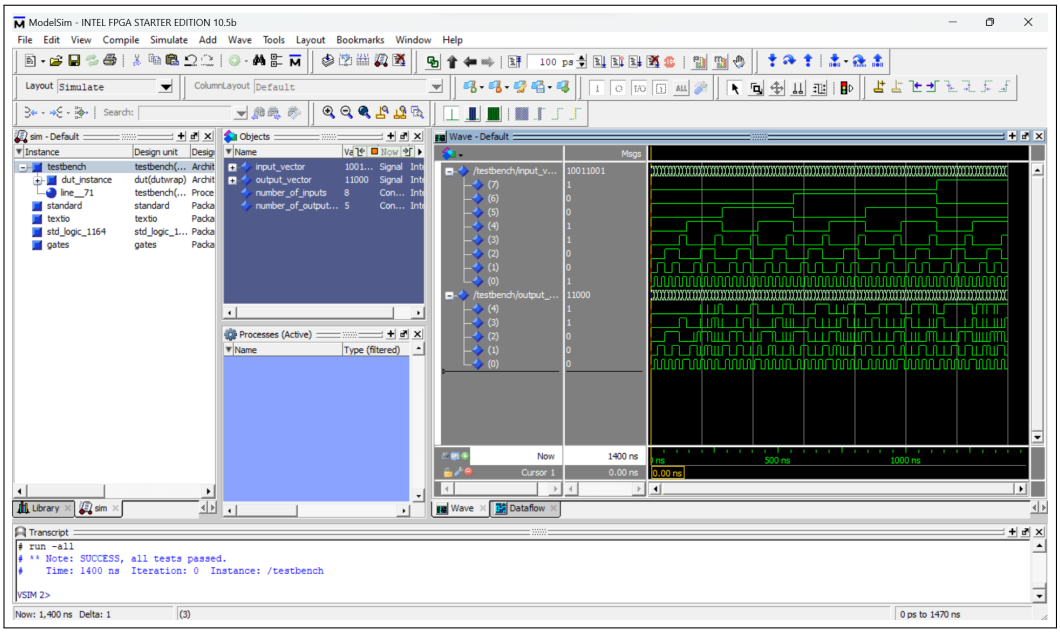
Concept

- If four-bit sum is equal to or less than 9, no correction is needed. The sum is in proper BCD form.
- If the four-bit sum is greater than 9 or if a carry is generated from the four-bit sum, the sum is invalid.
- To correct the invalid sum, add 0110_2 to the four-bit sum. If a carry results from this addition, add it to the next higher-order BCD digit.

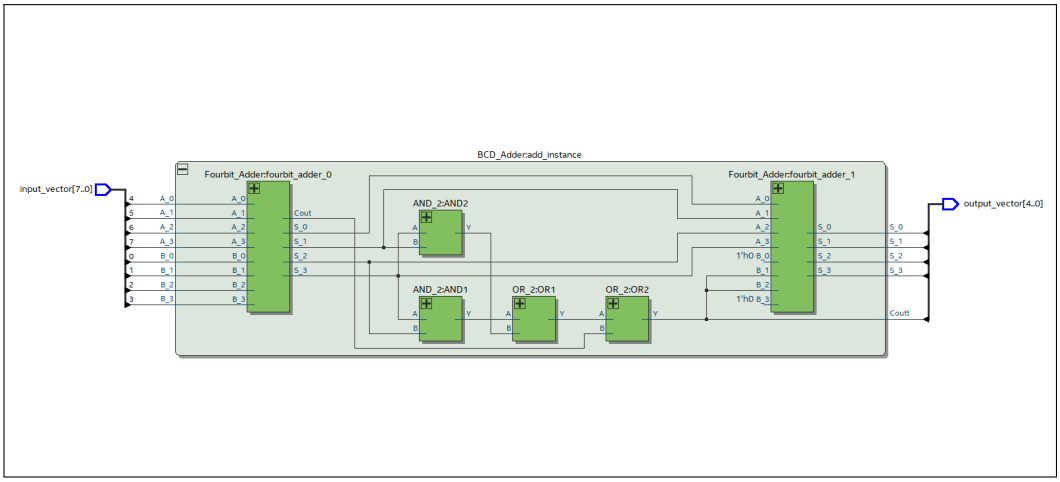
1 Pen-paper Design of the Circuit



2 RTL Waveform Simulation



3 RTL Gates Map



4 All Success OUTPUT