

Lab Session 6: Sequence Generator

using *Structural Dataflow Modelling*

Sravan K Suresh
Roll Number: 22B3936

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Overview of the Report

This report contains:

- [State Table](#)
- [RTL Waveform Simulation of the function](#)
- [RTL Gates Map of the function](#)
- [OUTPUT verifying all tests successful](#)

Problem Statement

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- Write VHDL description in Structural-Dataflow modeling to generate the sequence 1 1 0 0 1 1.
- Use structural-dataflow modeling only.
- Reset is asynchronous in nature i.e. reset effects the output sequence irrespective of the input clock arrival.
- On Reset, sequence should start from the first '1'.
- Unused states should be mapped to one of the known state which is reset state.

0.1 Dataflow Equations

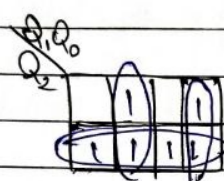
Code Documentation

```
1  entity Sequence_generator_stru_dataflow is
2  port (reset, clock: in std_logic;
3  y:out std_logic);
4  end entity Sequence_generator_stru_dataflow;
5  architecture struct of Sequence_generator_stru_dataflow is
6  signal D:std_logic_vector(2 downto 0);
7  signal Q:std_logic_vector(2 downto 0);
8
9  begin
10     — equations for D(2), D(1), and D(0)
11  D(2) <= (Q(2) and (not Q(1)) AND Q(0)) or ((not Q(0)) and
        Q(1)AND (NOT Q(2)));
12  D(1) <= (Q(0) and (not Q(1))) or ((not Q(2)) AND (not Q(1))
        );
13  D(0) <= Q(2) or (Q(0) xor Q(1));
14
15  DFF2 : dff_reset port map (D => D(2), clock => clock, reset
        => reset, Q => Q(2));
16  DFF1 : dff_reset port map (D => D(1), clock => clock, reset
        => reset, Q => Q(1));
17  DFF0 : dff_set port map (D => D(0), clock => clock, set =>
        reset, Q => Q(0));
18
19  y <= Q(0);
```

Observations

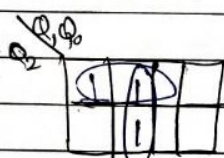
1 State Table

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Present State	Next State	DFF inputs
001	011	011
011	000	000
000	010	010
010	101	101
101	111	111
111	001	001
100	001	001
110	001	001

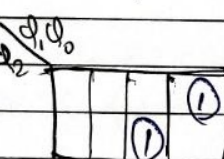
D_0 : 

$$D_0 = Q_2 + Q_0Q_1 + Q_0\bar{Q}_1$$

$$D_0 = Q_2 + (Q_1 \oplus Q_0)$$

D_1 : 

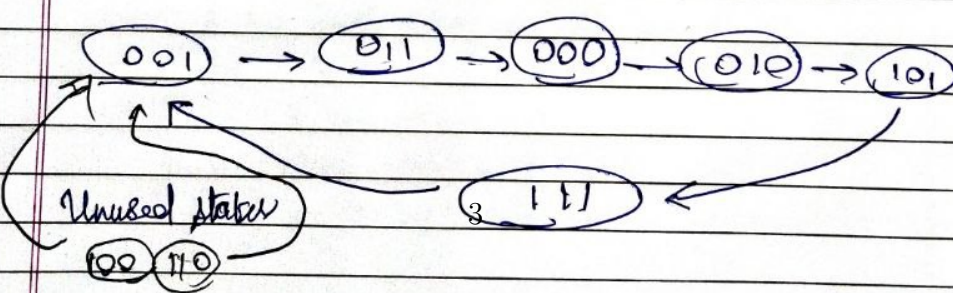
$$D_1 = Q_0\bar{Q}_1 + \bar{Q}_1\bar{Q}_2$$

D_2 : 

$$D_2 = \bar{Q}_1Q_0Q_2 + \bar{Q}_0Q_1\bar{Q}_2$$

$$= Q_1 \oplus (Q_0Q_2)$$

Reset State



2 Transcript

```
Transcript
File Edit View Bookmarks Window Help

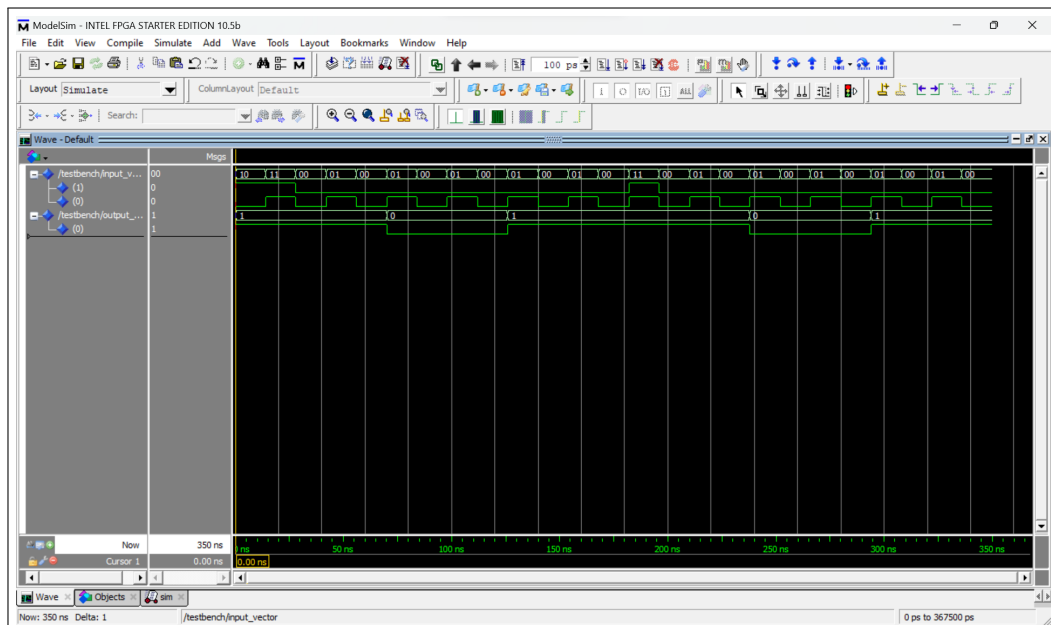
-- Loading package ieee
-- Loading package Gates
-- Compiling entity Sequence_generator_stru_dataflow
-- Compiling architecture struct of Sequence_generator_stru_dataflow
End time: 16:03:17 on Sep 15, 2023, Elapsed time: 0:00:00
Errors: 0, Warnings: 0

# vcom -93 -work work (C:/Users/ASUS/OneDrive - Indian Institute of Technology Bombay/ACADS/SEMESTER-3/EE-214/Lab6_22B3936/Testbench.vhdl)
# Model Technology ModelSim - Intel FPGA Edition vcom 10.5b Compiler 2016.10 Oct 5 2016
# Start time: 16:03:17 on Sep 15, 2023
# vcom -reportsprogress 300 -s3 -work work C:/Users/ASUS/OneDrive - Indian Institute of Technology Bombay/ACADS/SEMESTER-3/EE-214/Lab6_22B3936/Testbench.vhdl
-- Loading package STANDARD
-- Loading package TEXTIO
-- Loading package std_logic_1164
-- Compiling entity Testbench
-- Compiling architecture Behave of Testbench
End time: 16:03:17 on Sep 15, 2023, Elapsed time: 0:00:00
Errors: 0, Warnings: 0

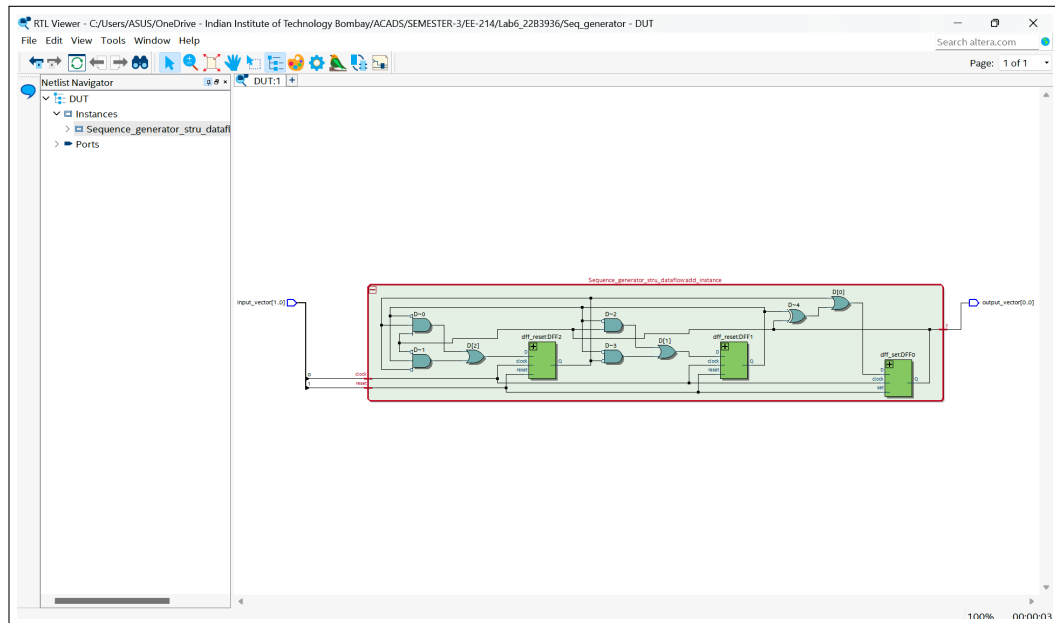
# vsim -t lps -L altera -L lpm -L sgate -L altera_mf -L altera_lnsim -L fiftyfivenm -L rtl_work -L work -voptargs="+acc" testbench
# vsim -t lps -L altera -L lpm -L sgate -L altera_mf -L altera_lnsim -L fiftyfivenm -L rtl_work -L work -voptargs="+acc" testbench
# Start time: 16:03:17 on Sep 15, 2023
# Loading std.standard
# Loading std.textio(body)
# Loading ieee.std_logic_1164(body)
# Loading work.testbench(behave)
# Loading work.dat(dutwrap)
# Loading work.flipflops
# Loading work.gates
# Loading work.sequence_generator_stru_dataflow(struct)
# Loading work.diff_reset(behav)
# Loading work.diff_set(behav)
#
# add wave *
# view structure
# .main_pane.structure.interior.cs.body.struct
# view signals
# .main_pane.objects.interior.cs.body.tree
# run -all
# ** Note: SUCCESS, all tests passed.
# Time: 350 ns Iteration: 0 Instance: /testbench

VSM 2>
```

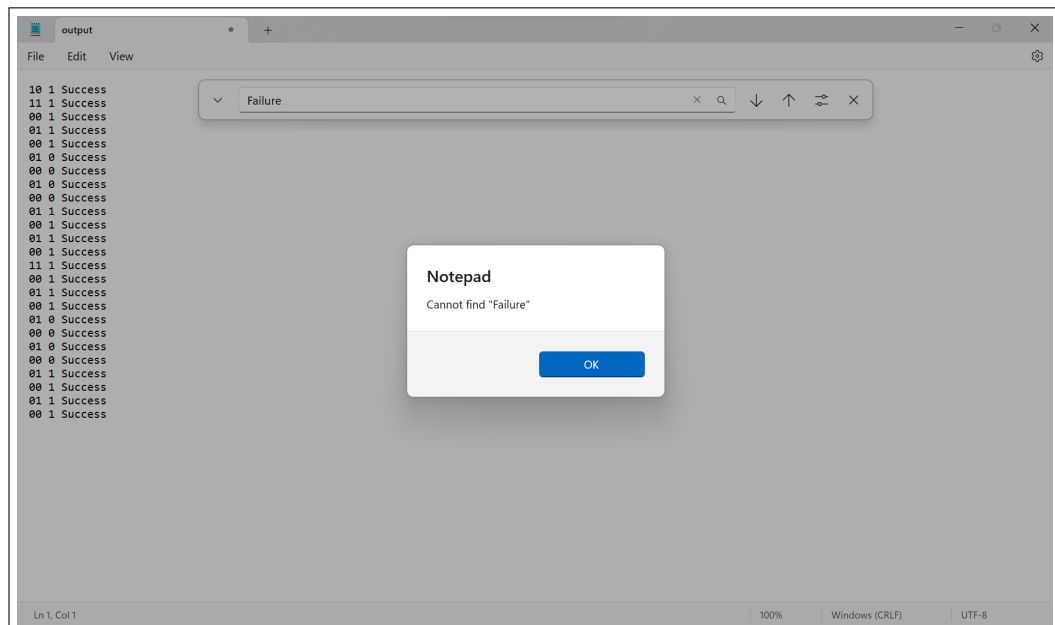
3 RTL Waveform Simulation



4 RTL Gates Map



5 All Success OUTPUT



References

- [1] EE214 Github Page: <https://ee214.github.io/>