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Xen 10 FPGA Board kit Demo

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In this demo:

- Introduction to Xen 10 FPGA board
- Selecting proper FPGA board
- Pin Planning
- Generating .svf file after compilation
- UrJTAG Installation and commands used
- load .svf file into the FPGA using UrJTAG
- Loading your design.svf file into the fpga and verify it by using the switches and LEDs

Xen-10 board

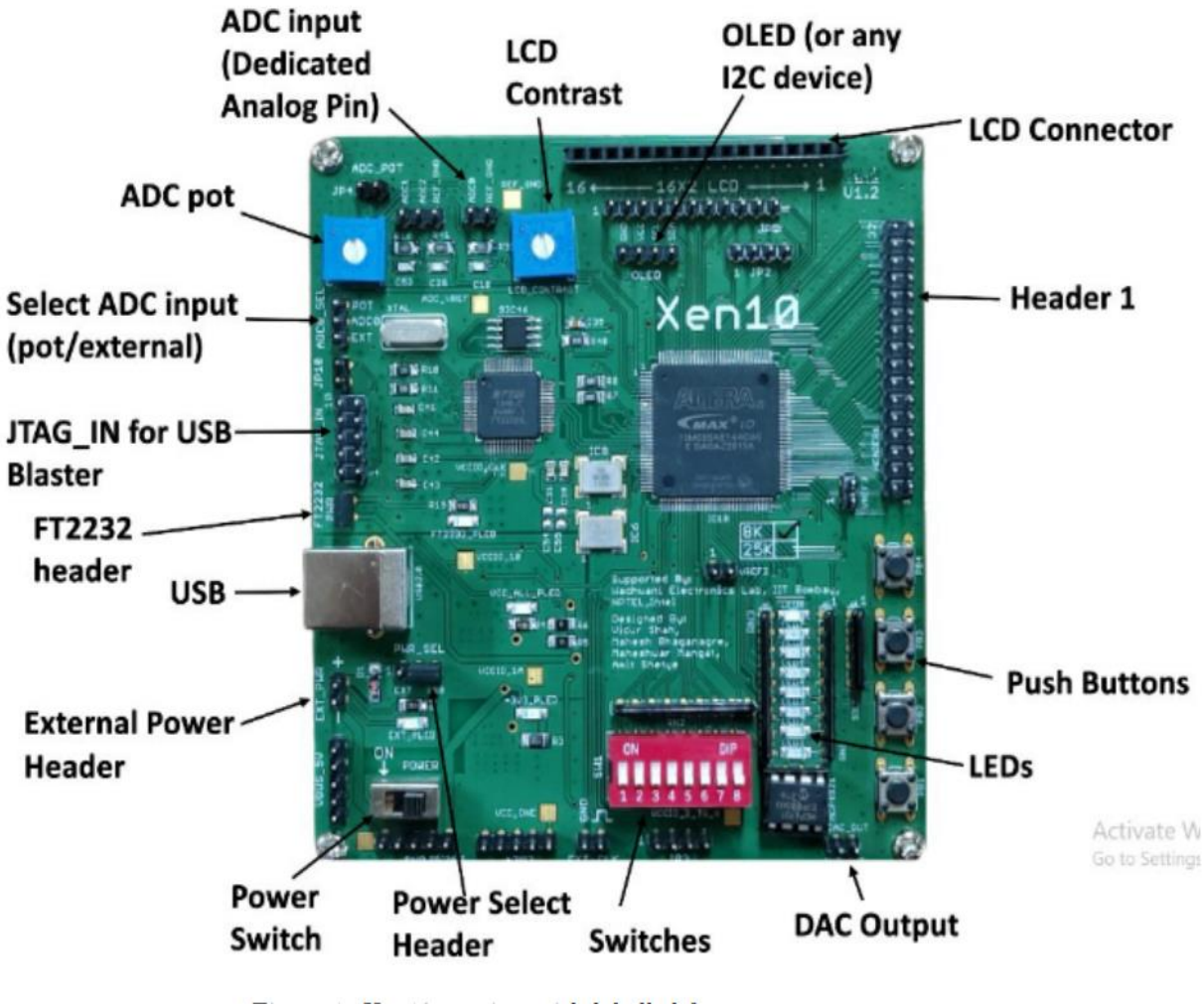
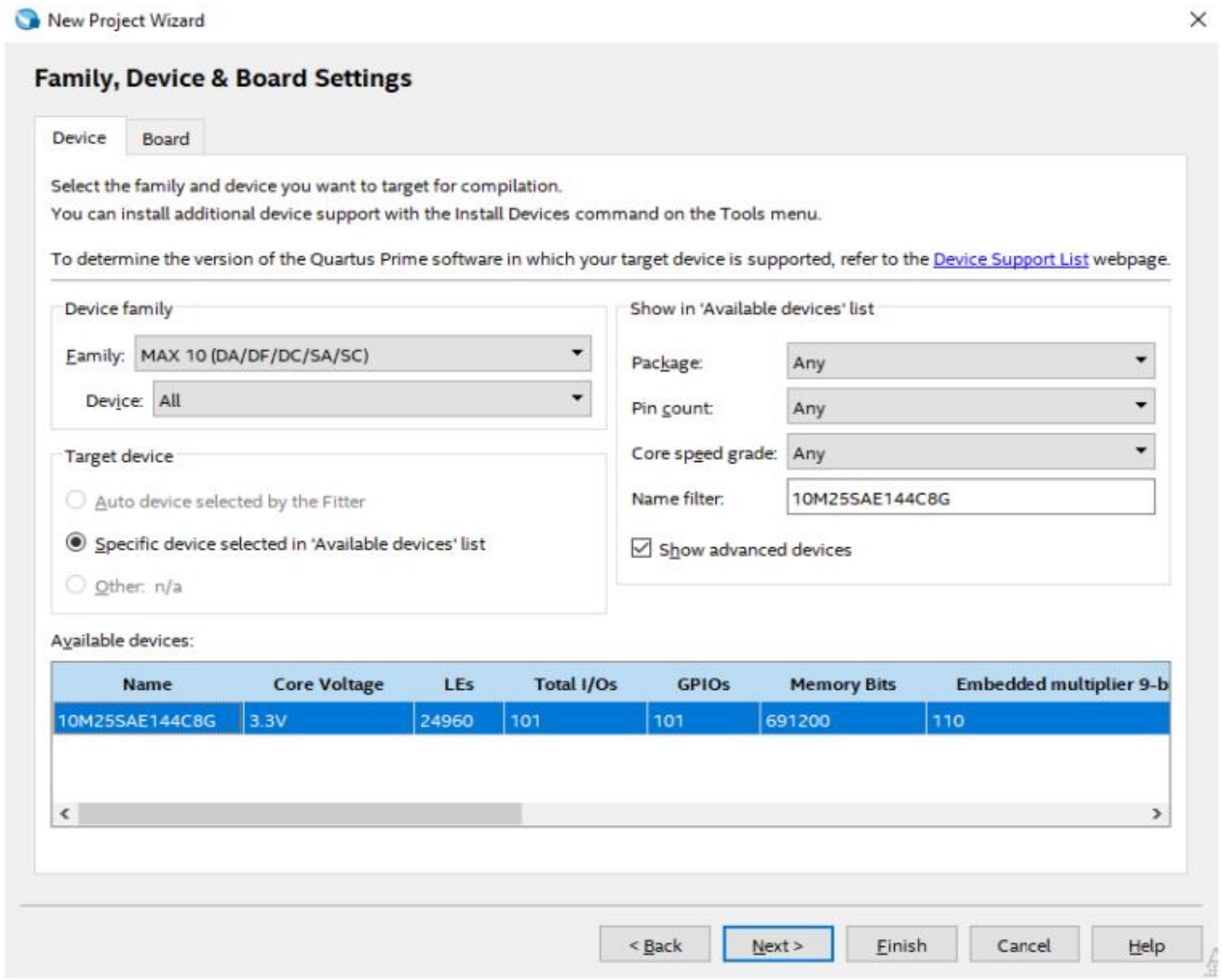


Fig: Top View of Xen 10 Board

- FPGA of Altera's MAX 10 family (**MAX 10 - 10M25SAE144C8G / 10M08SAE144C8G**)
- USB connector.
- 8 on-board switches.
- 8 on-board LEDs.
- 4 push-buttons.
- HEADER to connect to external devices.
- HEADER-1 : pin-31 is tied to VDD and 32 is tied to VSS. Never short and connect other signals to these pins.
- 16-pin connector for LCD panel and OLED or any other device with I2c interface.
- On-board 12-bit single channel MCP4921 DAC.
- On-board clock of 1Hz ,10MHz,50MHz and provision for external clock source connection through EXT CLK header.

DEVICE SELECTION

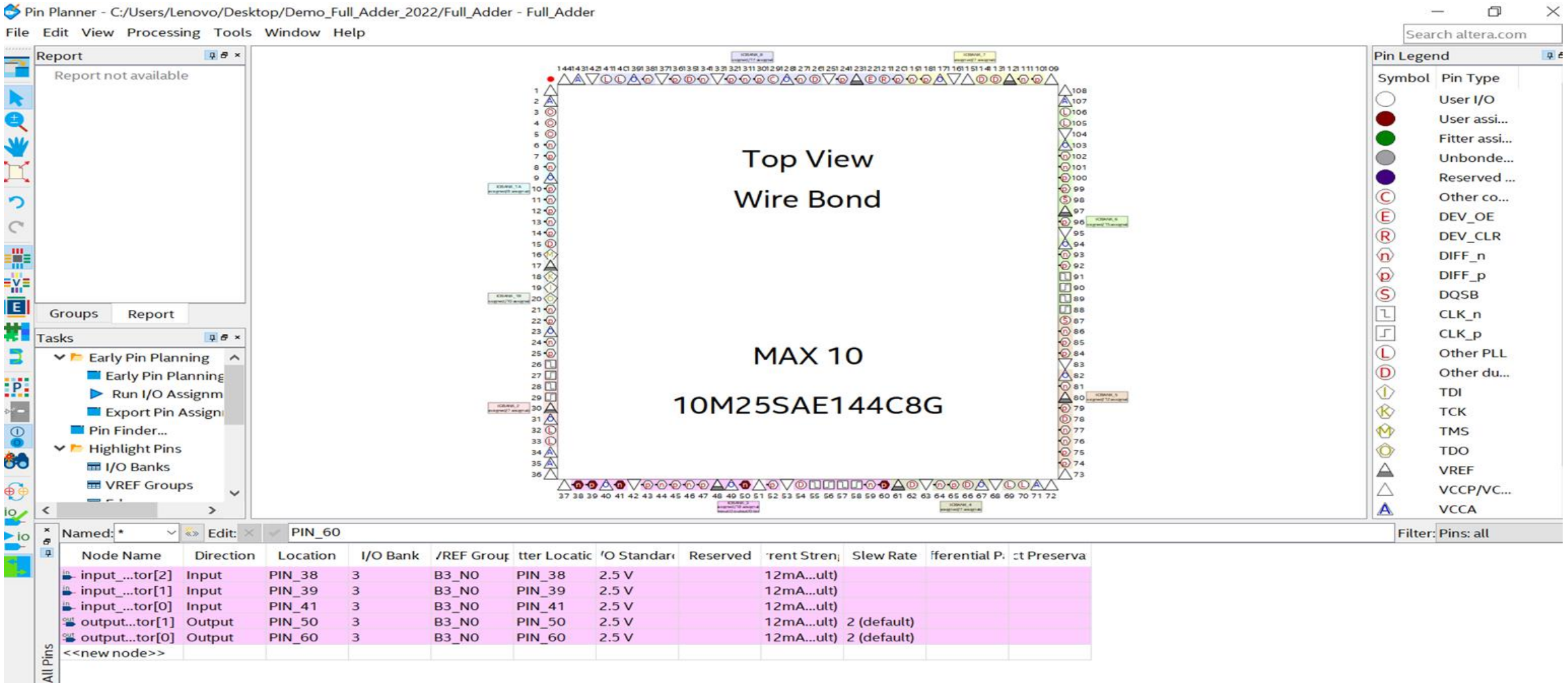
- In this family ,device and board settings ,we need to select the board properly.



Pin planning

In Pin Planning align the I/O ports of DUT with FPGA pins

Go to Assignments -> Pin Planner. Following window will open and will be able to see all the signals of DUT .



- Write Pin number in location column for assigning Input and output pins to the signals .
- Once done close the window and compile your design again.

Named: * Edit: PIN_60

Node Name	Direction	Location	I/O Bank
input_vector[2]	Input	PIN_38	3
input_vector[1]	Input	PIN_39	3
input_vector[0]	Input	PIN_41	3
output_vector[1]	Output	PIN_50	3
output_vector[0]	Output	PIN_60	3
<<new node>>			

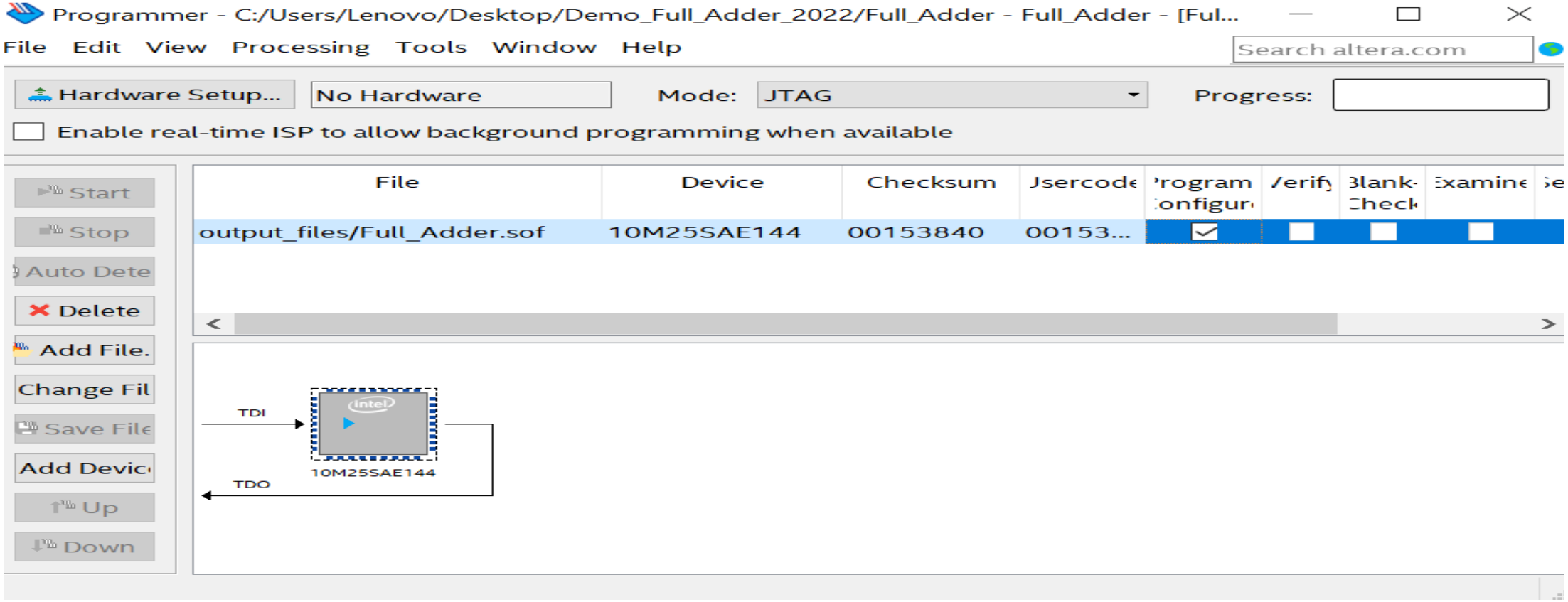
Assignment of Input /Output Pins

Switch	FPGA Pin no.	LED	FPGA Pin no.
SW 8	47	LED 8	60
SW 7	46	LED 7	59
SW 6	45	LED 6	58
SW 5	44	LED 5	57
SW 4	43	LED 4	56
SW 3	41	LED 3	54
SW 2	39	LED 2	52
SW 1	38	LED 1	50

Pin Mapping for On-board switches and leds

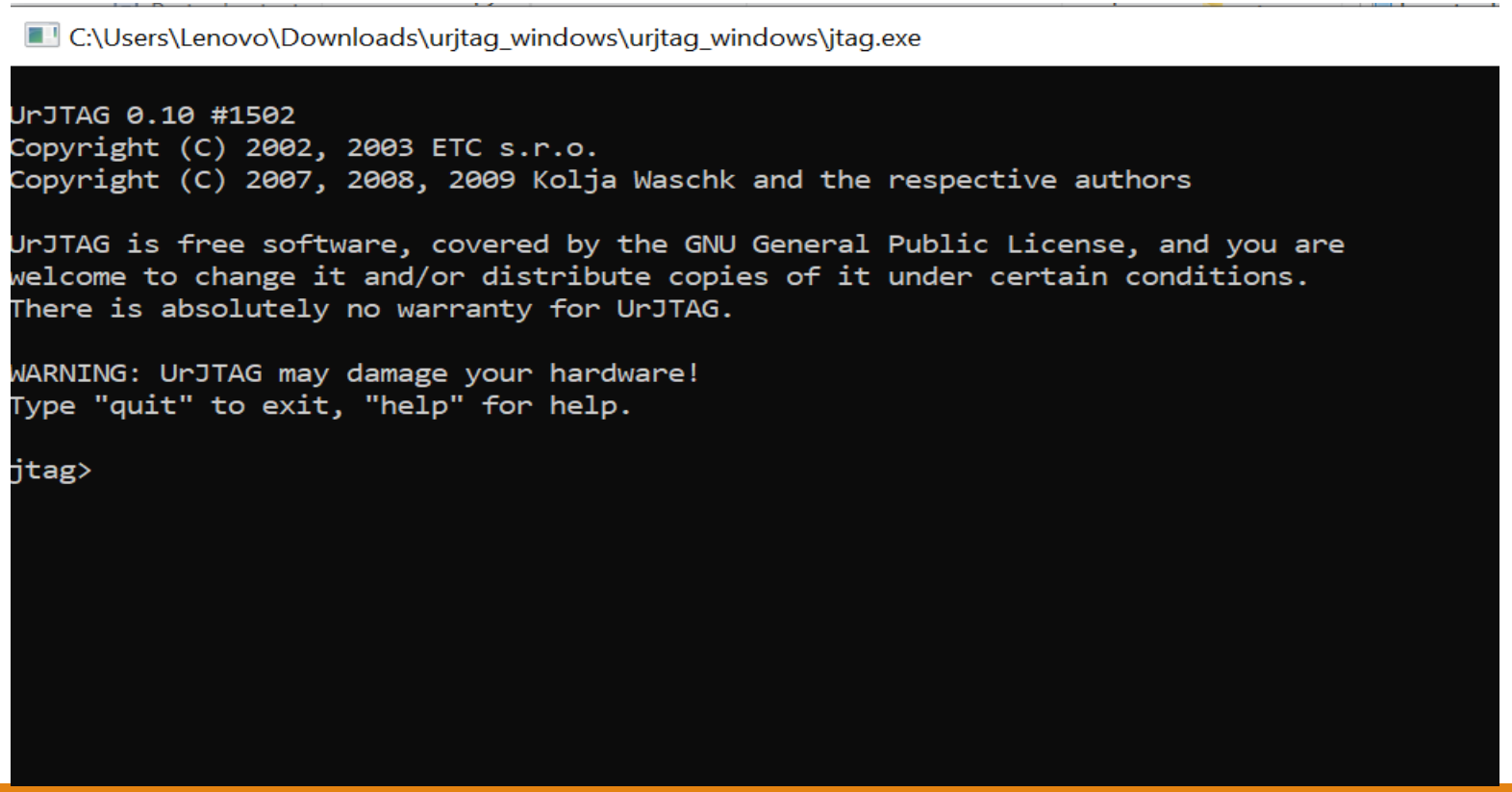
Generating svf file

- Go to Tools -> Programmer (Following Window will appear)
- Check we have .sof file if not add from output files
- Go to File -> Click on Create JAM,JBC,SVF or ISC file
- Change the File format to .svf then Click OK(Can change the file name also)
- .svf file will be generated in your project folder.



UrJTAG Installation

- JTAG : Joint Test action Group
- Download the UrJTAG_Max10 Zip folder and extract it.
- Inside UrJTAG open jtag.exe file , below jtag window will open.
- Connect your Xen10 Board to your device.



UrJTAG Commands

- Type: **cable ft2232**
  Establish the connection between FPGA board and usb(PC/LAPTOP).
- Now type: **detect**
  which displays the detected CPLD device (Details like IRChain length, Manufacturer, Device ID, Stepping etc.)
- Load the svf file into the CPLD device by typing
  svf <path> /<Name_of_File.svf> progress
  Either drag the file to the jtag window for path or Copy the .svf file to UrJTAG folder.

UrJTAG Possible errors

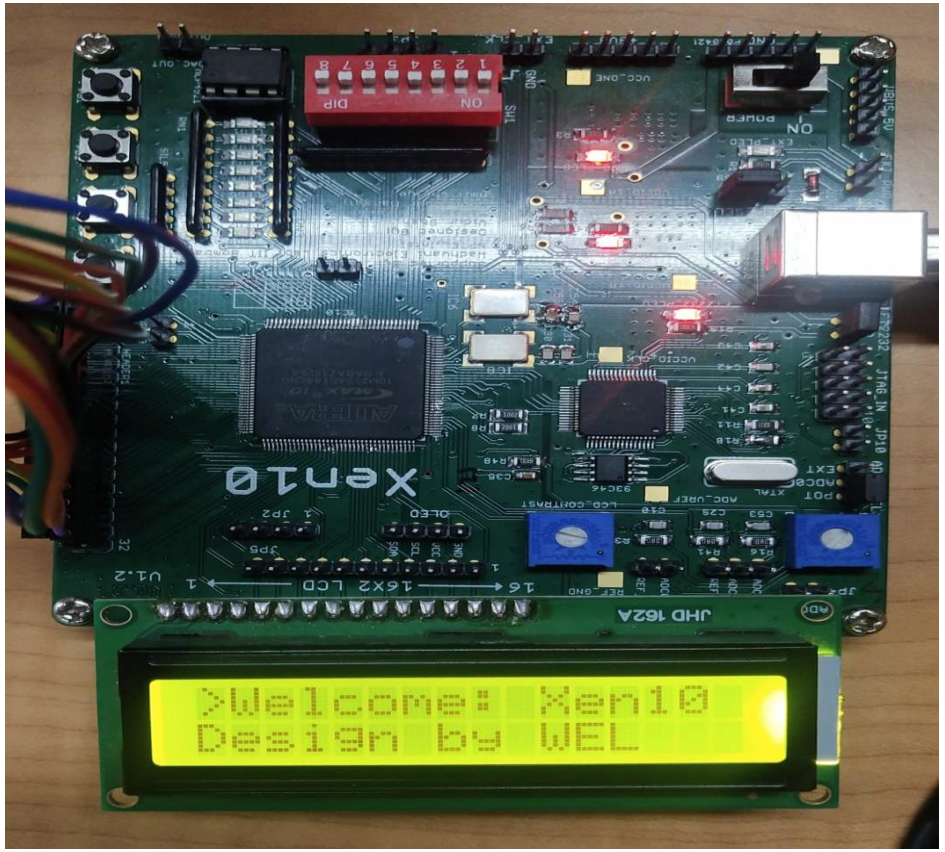
- TDO mismatch
  - Selected wrong device name
- Hardware Detect, TDI/TDO stuck at 0/1.
  - Reconnect the board
  - Use different USB port
  - Restart your computer/Laptop.
- Part not found/ Unknown Manufacturer.
  - Reinstall using the script for Ubuntu.
- Segmentation Fault
  - Reinstall using the script for Ubuntu.
- Strange error : SIR Instruction Length Inconsistent.
  - Create new project.

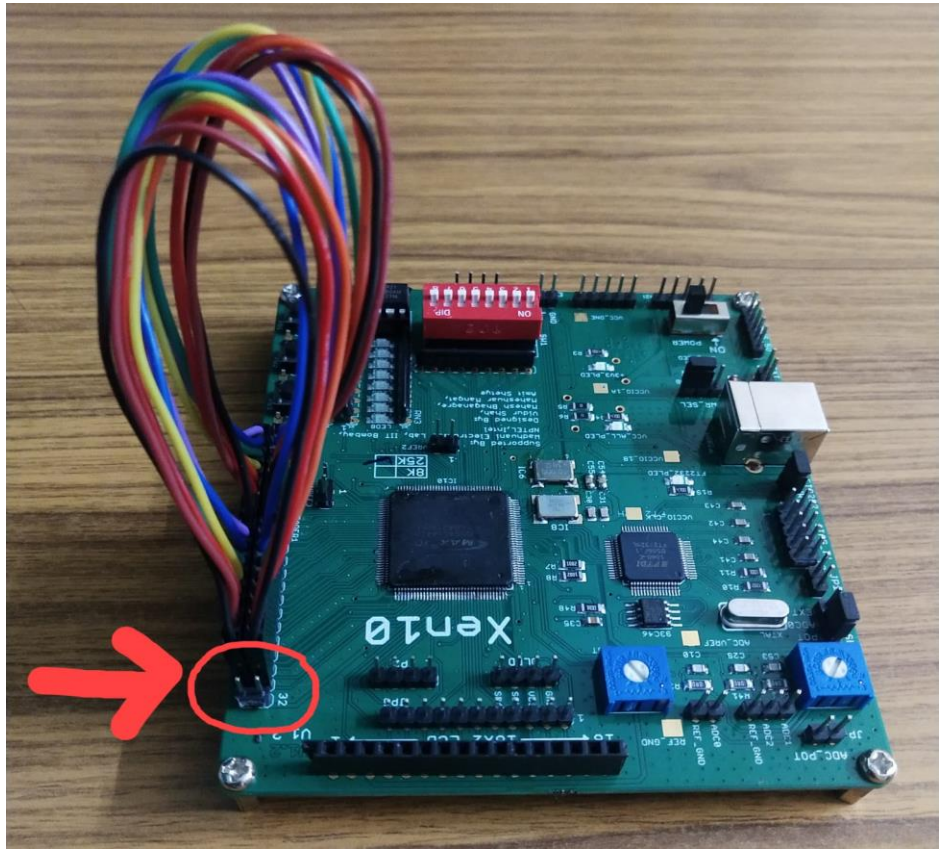
Testing the Xen10 board

Required Connection:

- Connect LCD to LCD header , ensuring pin-1 of LCD is connected to the corresponding pin-1 of the LCD header.
- Connect pins of Header-1 using strip cables. Pin-1 should be connected to pin-2, similarly pin-3 to pin -4 and so on until pin-29 to pin-30 .
  Make sure that pin-31 (i.e. VDD) should not be connected to pin-32(i.e. GND) of the header .

Header connections





Testing the Xen10 board: On board peripheral and IO header

Svf file to be loaded according to your device , initially all switches are to be kept off.

- Make SW8 on to reset the system and make it off after resetting. On successful reset LCD will display "***Welcome: Xen10 Design by WEL***" this implies SW8 is working properly.
- After that LCD will displayed "***Push PB1 for start testing***". Press PB1 to start Xen 10 board testing.
- Testing will start with Clock frequencies testing : **50 MHz, 10 MHz and 1 Hz** clock generators are tested sequentially. Clock pulses are counted and displayed on LED's in binary encoded format, once a threshold count is reached, LCD will display "***Done***" message.
- "***Test SW and LED***" will appear on LCD .
  Turn on SW1. Notice one led will blink at a time and shift through all the LEDs. Similarly when SW2 is turned on keeping the SW1 on, two LEDs will blink and shift and so on until SW7 is turned on where seven LEDs will blink and shift. Once all switches till SW7 are on, LCD will display "***Done***".
- **Push Button Testing**: After completing switch and LED test, LCD will display "***Test: Push Button***". Press each push button at least once to pass the test.
- **Bidirectional Pin Header Testing**: Switch on SW4 and press PB2 after the LCD displays "***SW on SW4, Press PB2: test Header***". Result of Header-1 testing will be displayed on LCD within few seconds.

Thank you