Lab Session 6: `Sequence Generator` using *Structural Dataflow Modelling*

Sravan K Suresh
Roll Number: `22B3936`

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Overview of the Report

This report contains:

- State Table
- RTL Waveform Simulation of the function
- RTL Gates Map of the function
- OUTPUT verifying all tests successful

Problem Statement

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• Write VHDL description in Structural-Dataflow modeling to generate the sequence 1 1 0 0 1 1.
• Use structural-dataflow modeling only.
• Reset is asynchronous in nature i.e. reset effects the output sequence irrespective of the input clock arrival.
• On Reset, sequence should start from the first '1'.
• Unused states should be mapped to one of the known state which is reset state.

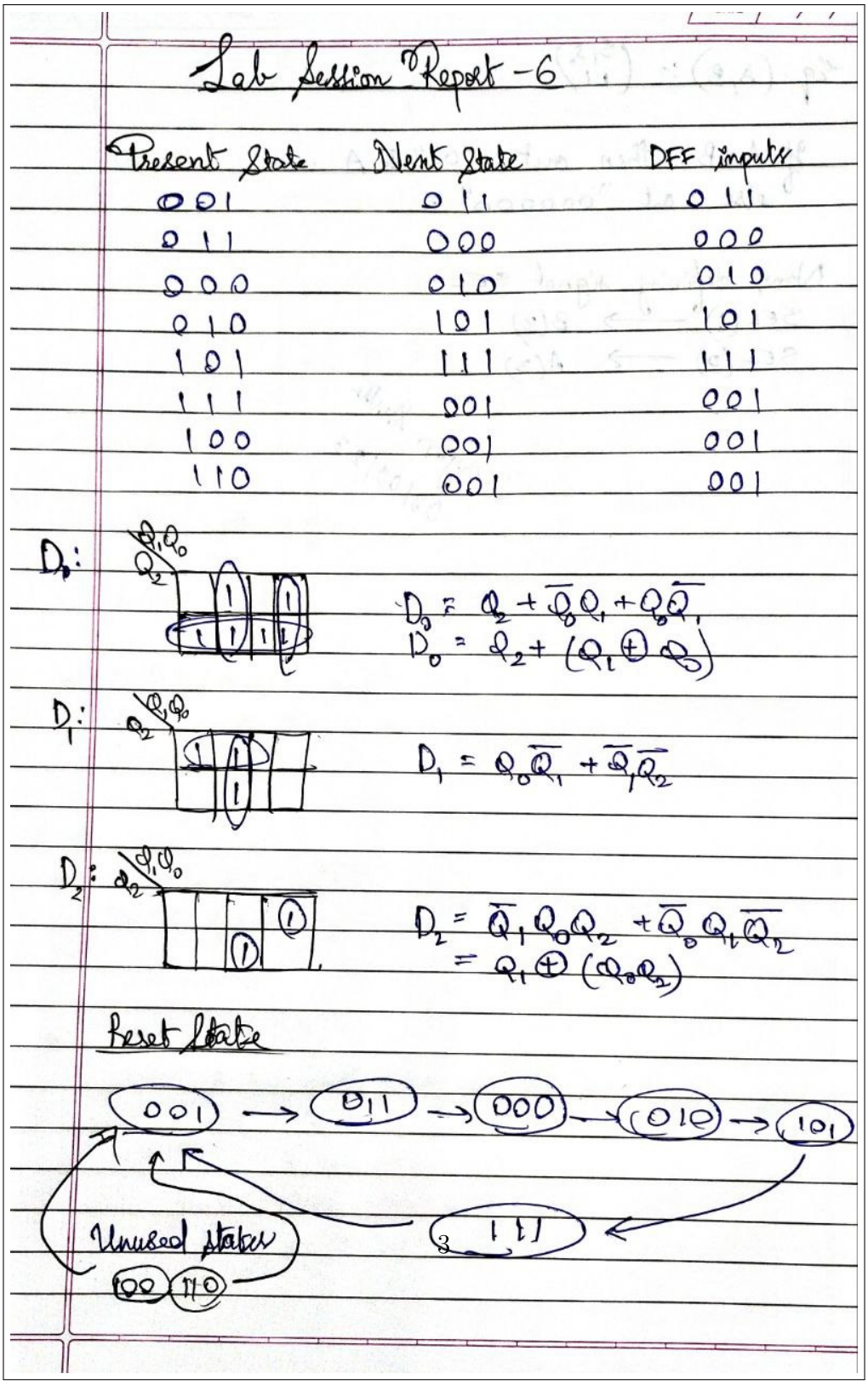
0.1 Dataflow Equations

Code Documentation

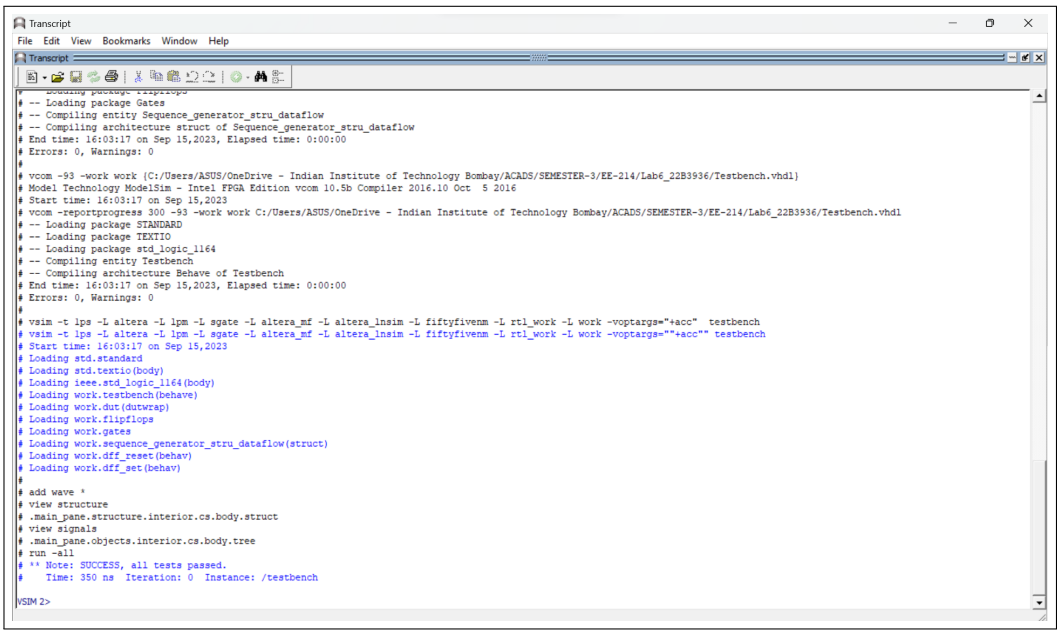
```
entity Sequence_generator_stru_dataflow is
port (reset,clock: in std_logic;
y:out std_logic);
end entity Sequence_generator_stru_dataflow;
architecture struct of Sequence_generator_stru_dataflow is
signal D:std_logic_vector(2 downto 0);
signal Q:std_logic_vector(2 downto 0);

begin
    -- equations for D(2), D(1), and D(0)
D(2) <= (Q(2) and (not Q(1)) AND Q(0)) or ((not Q(0)) and
   Q(1)AND (NOT Q(2)));
D(1) <= (Q(0) and (not Q(1))) or ((not Q(2)) AND (not Q(1))
    );
D(0) <= Q(2) or (Q(0) xor Q(1));

DFF2 : dff_reset port map (D => D(2), clock => clock, reset
    => reset, Q => Q(2));
DFF1 : dff_reset port map (D => D(1), clock => clock, reset
    => reset, Q => Q(1));
DFF0 : dff_set port map (D => D(0), clock => clock, set =>
   reset, Q => Q(0));

y <= Q(0);
```

Observations

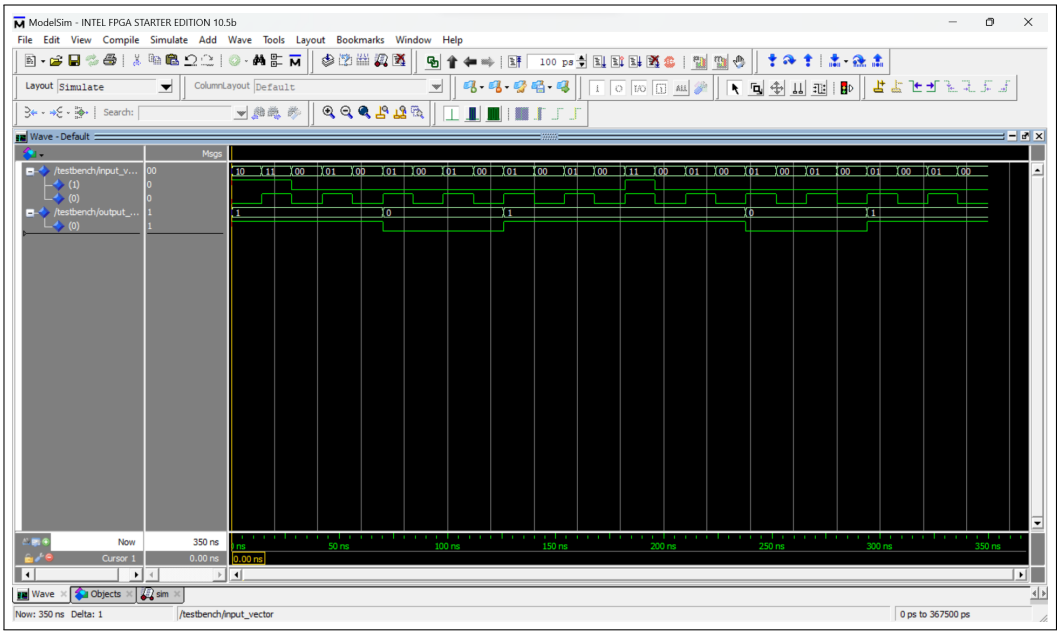
1 State Table



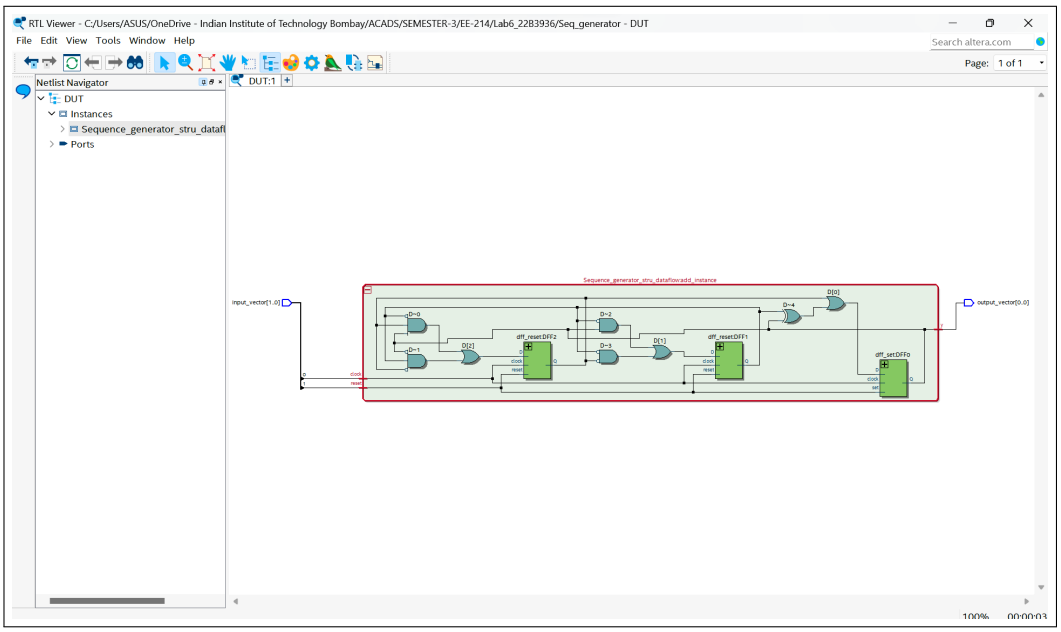
2 Transcript



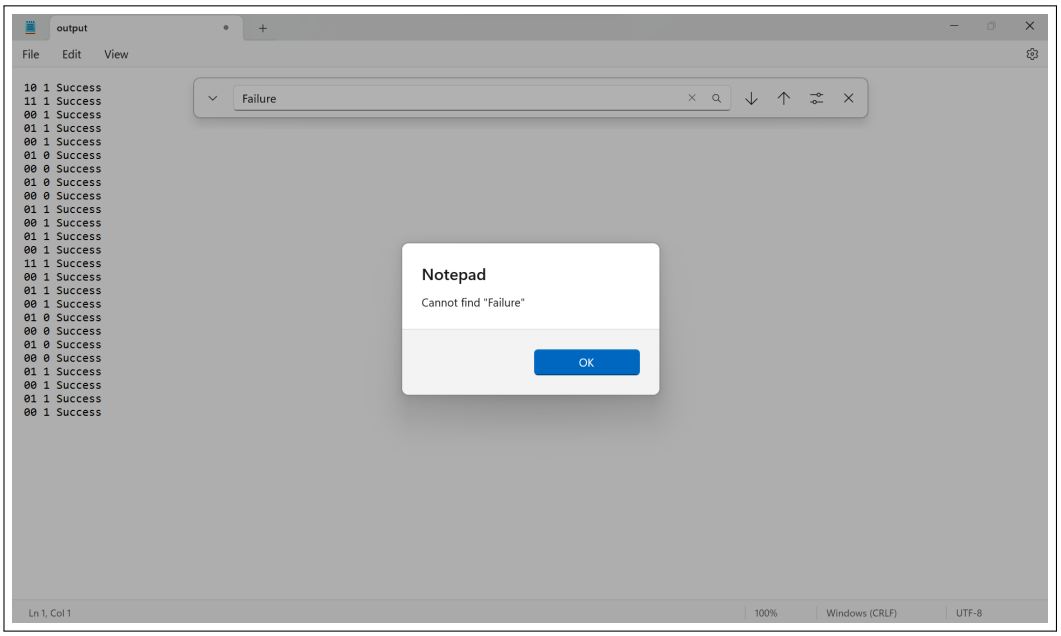
3 RTL Waveform Simulation



4 RTL Gates Map



5 All Success OUTPUT



References

[1] EE214 Github Page: https://ee214.github.io/