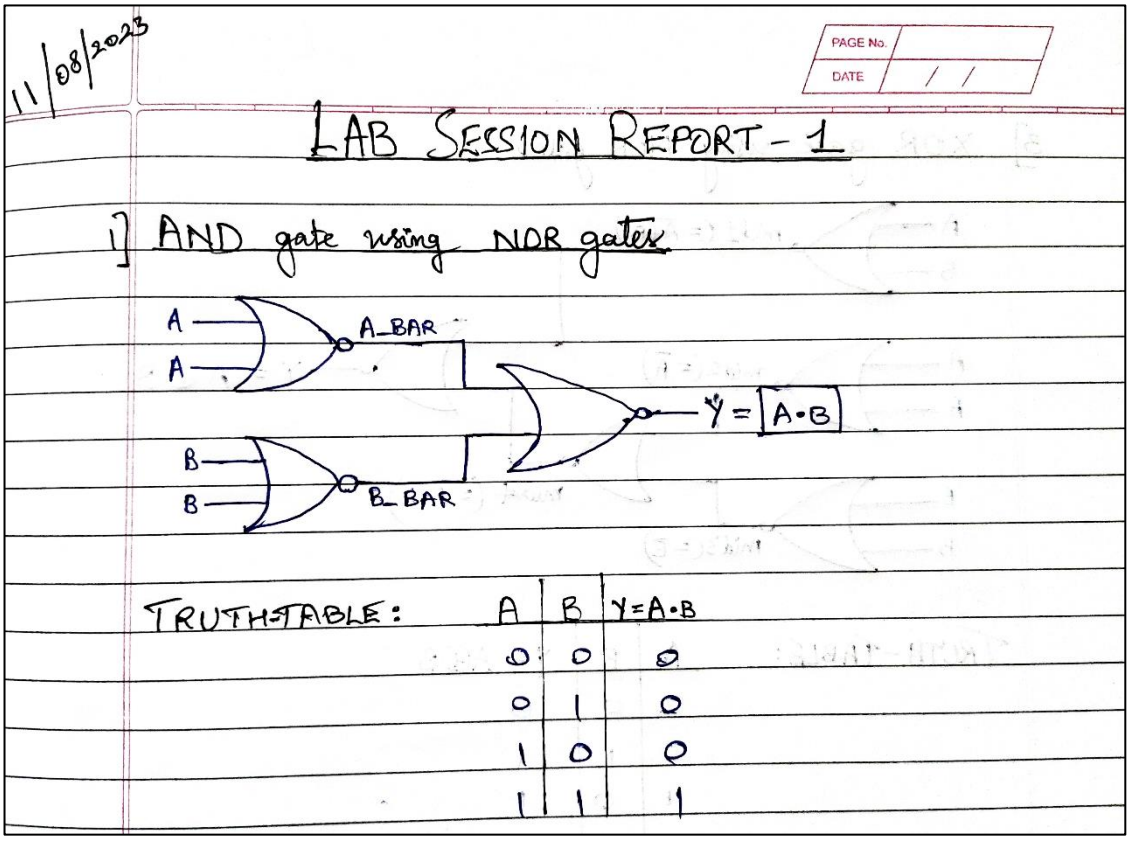
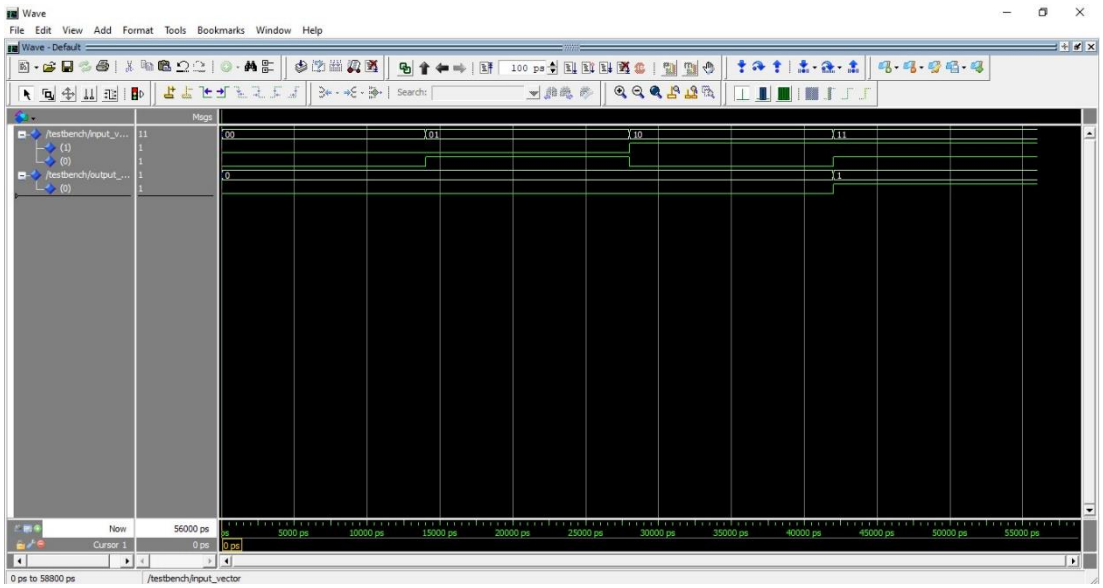
EE214 (Digital Circuits Lab)
Lab Report (Expt. 1)

❖ AND gate using NOR

- Pen-paper design



- ModelSim Waveforms



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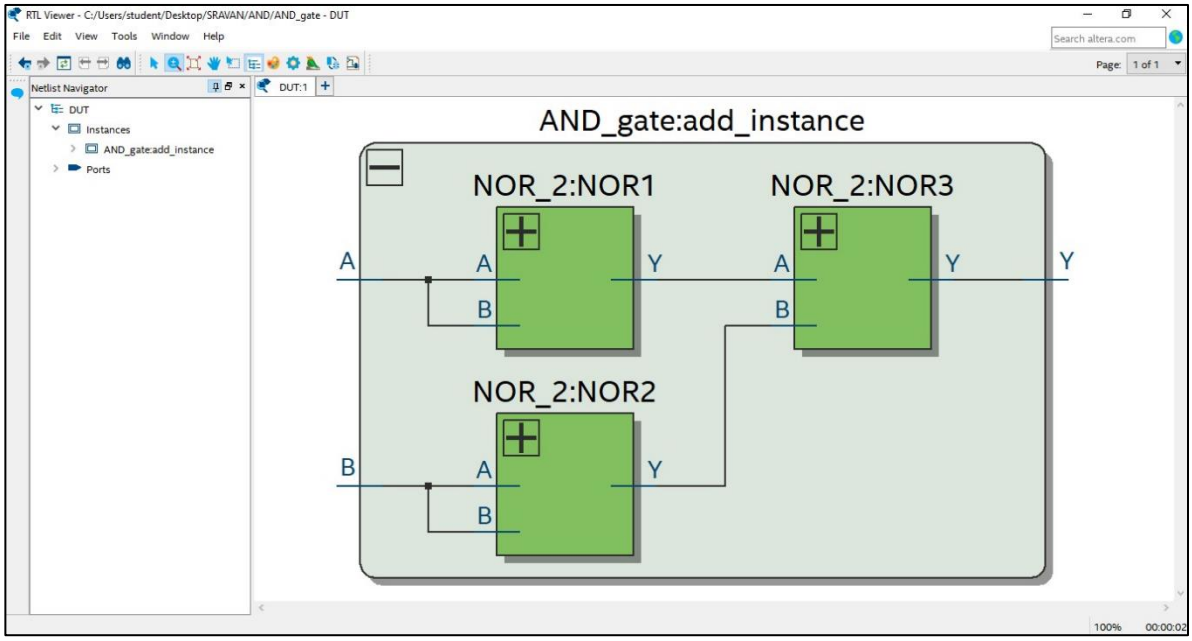
EE214 (Digital Circuits Lab)

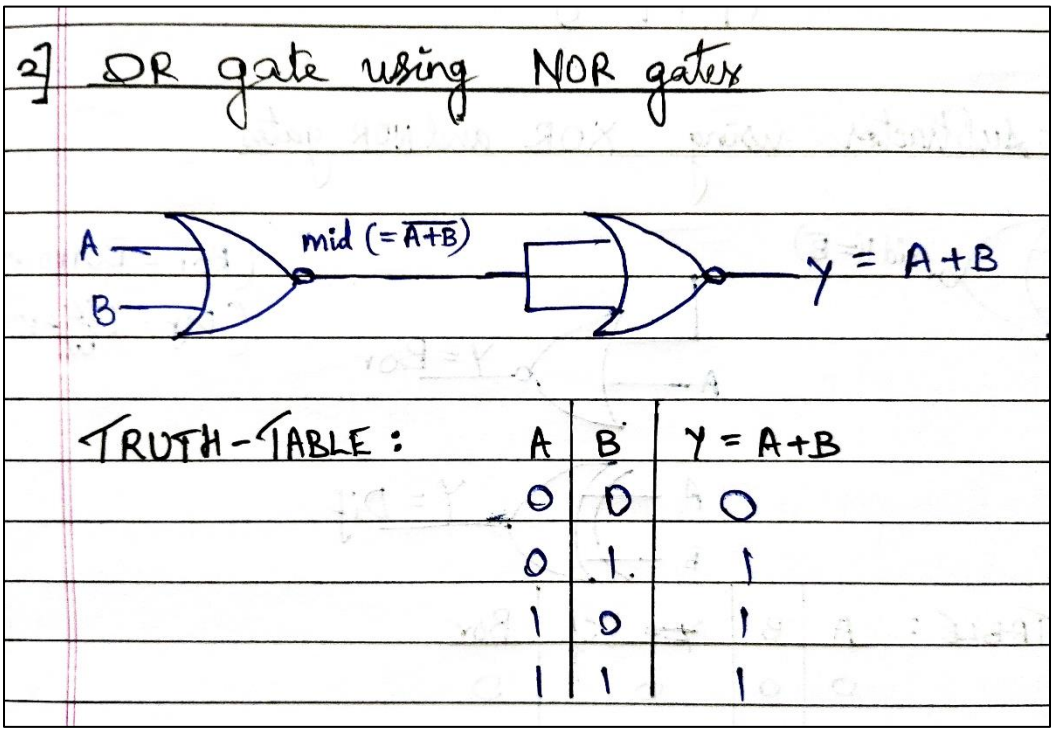
Lab Report (Expt. 1)

- RTL Netlist viewer



❖ OR gate using NOR

- Pen-paper design



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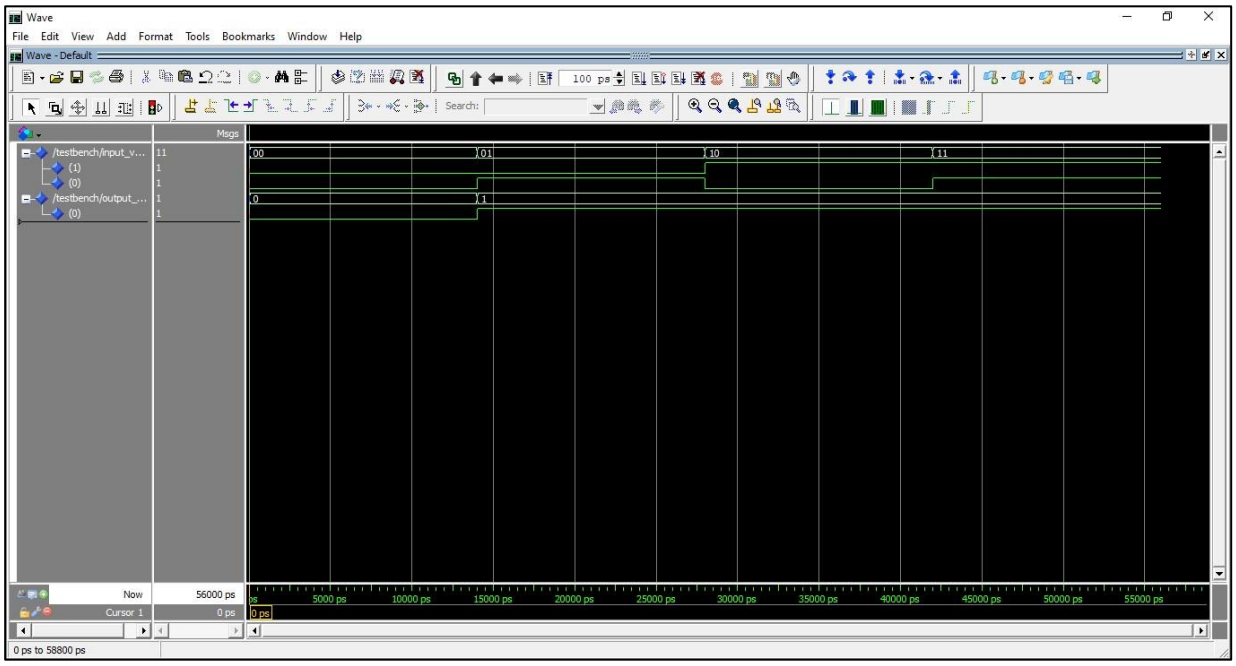
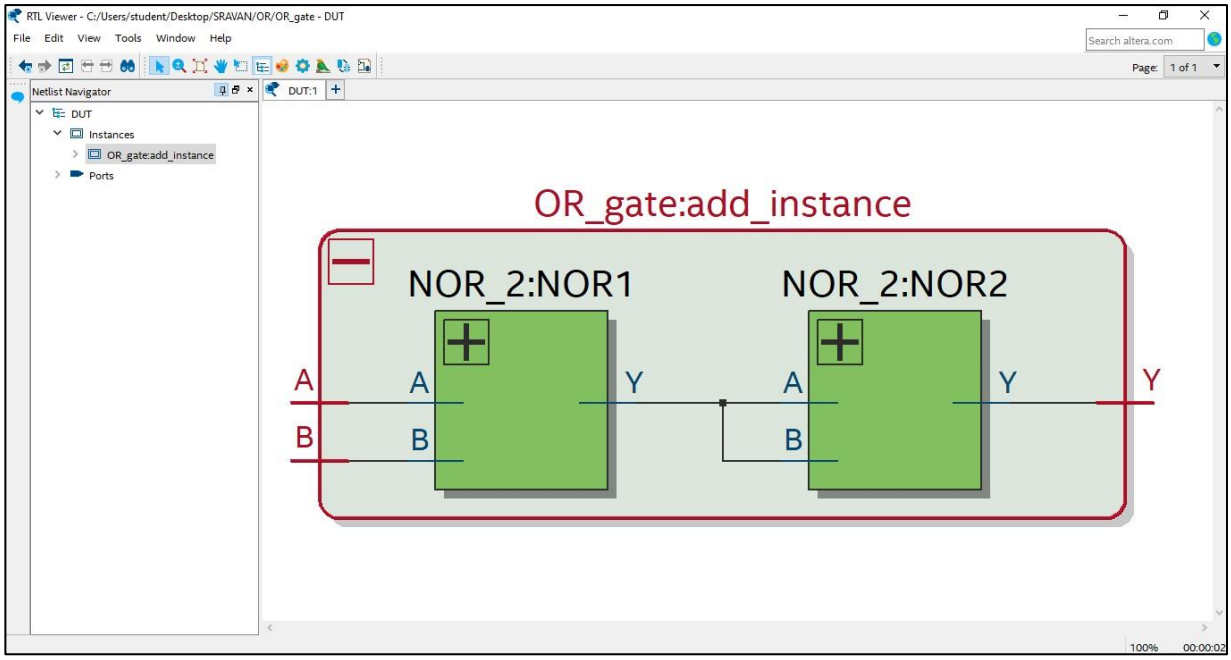
- ModelSim Waveforms



- RTL Netlist viewer



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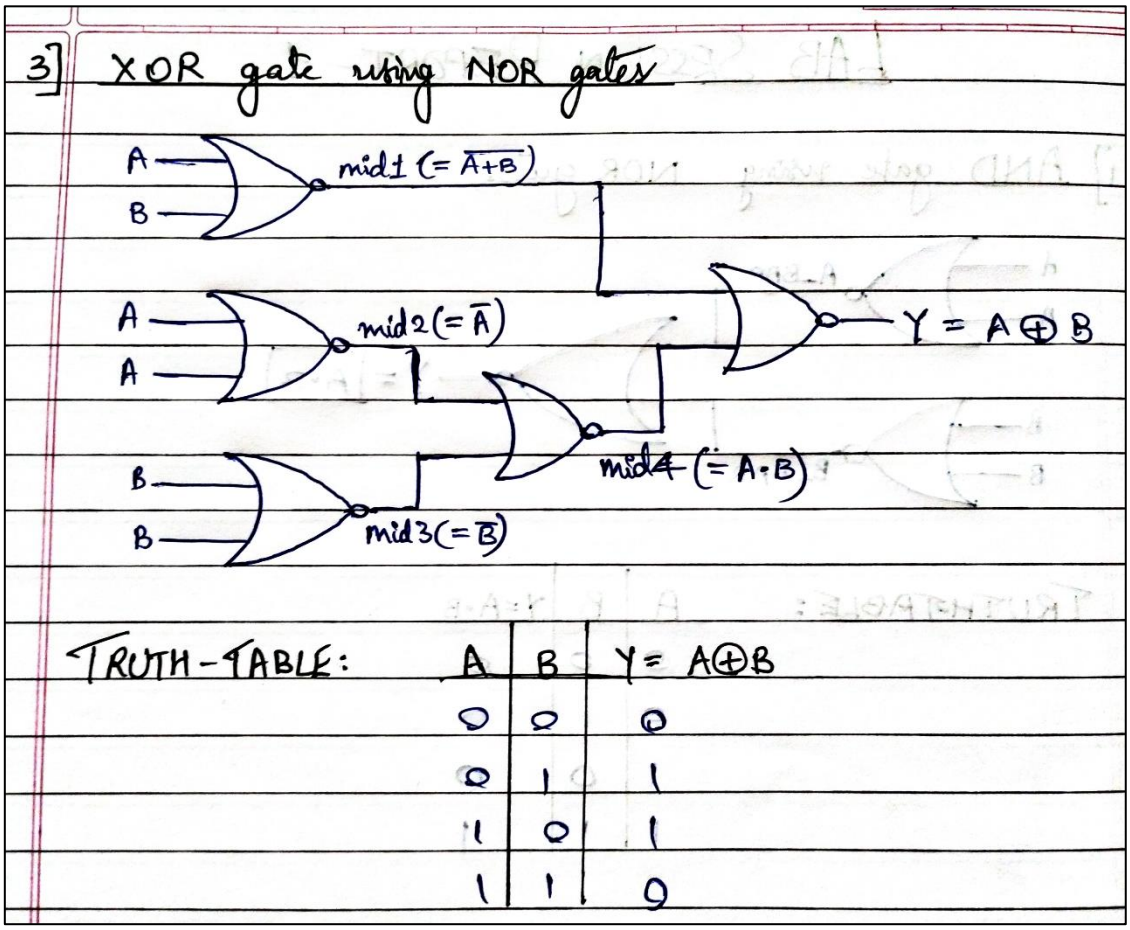
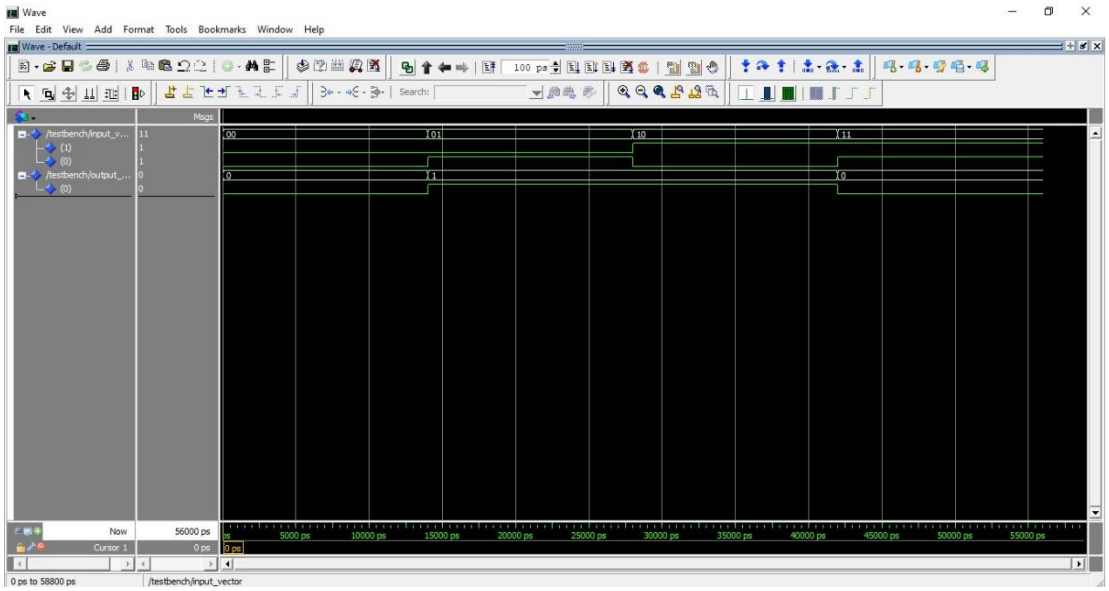
EE214 (Digital Circuits Lab)
Lab Report (Expt. 1)

❖ XOR gate using NOR

- Pen-paper design



- ModelSim Waveforms



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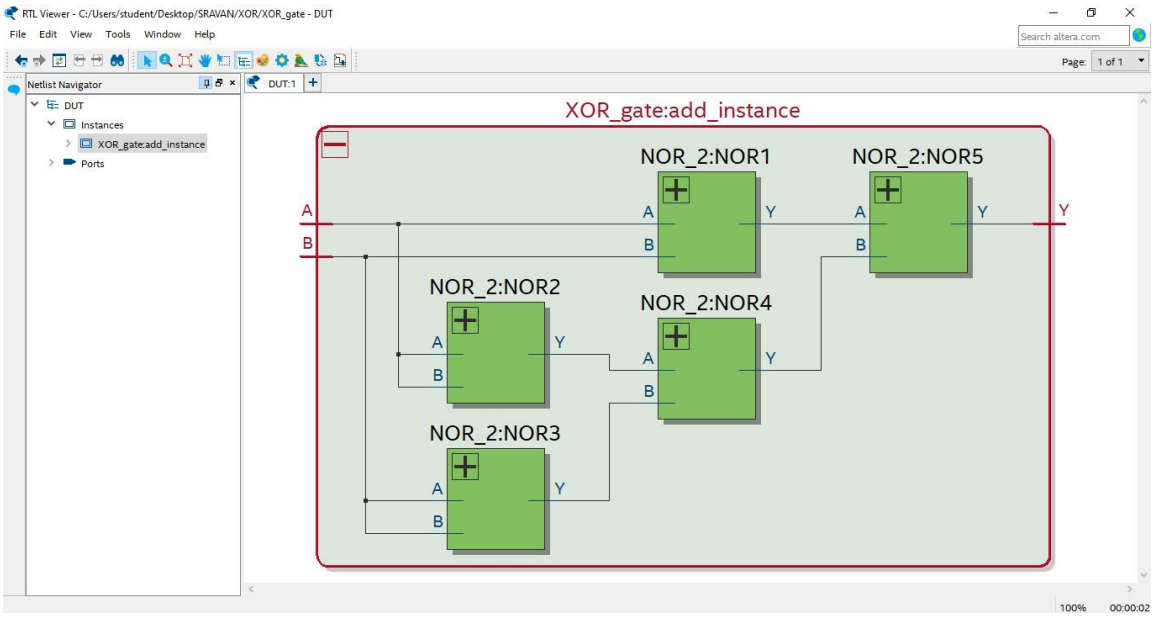
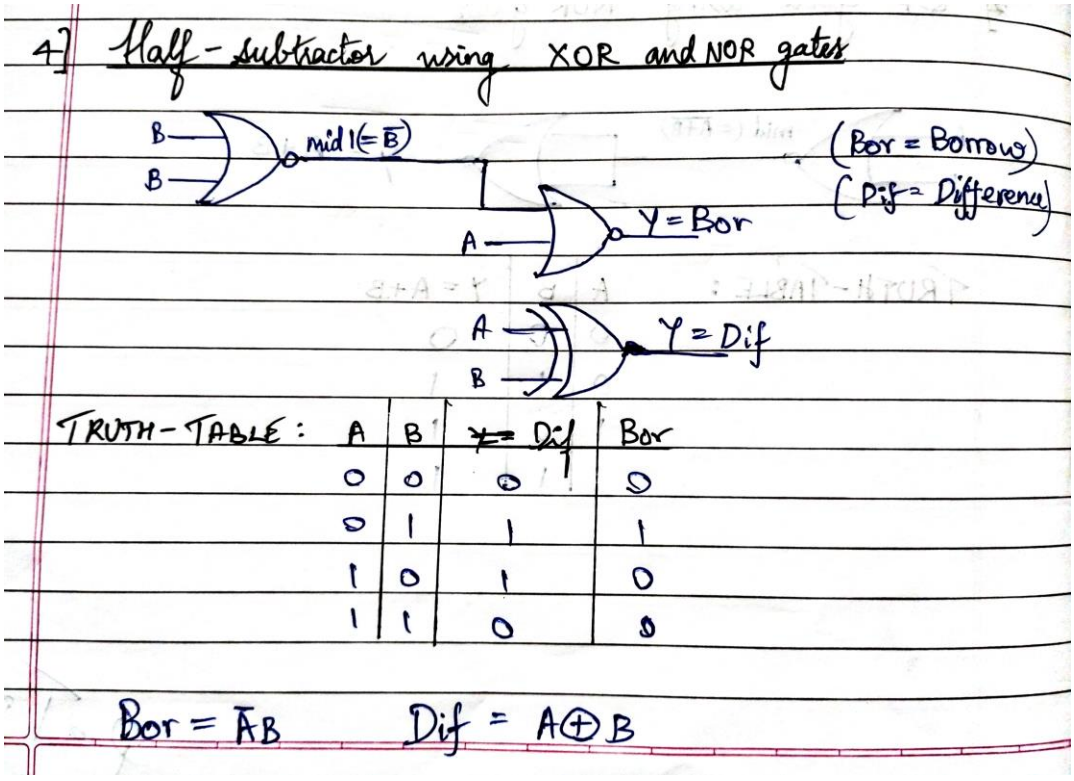
Lab Report (Expt. 1)

- RTL Netlist viewer



❖ AND gate using NOR

- Pen-paper design



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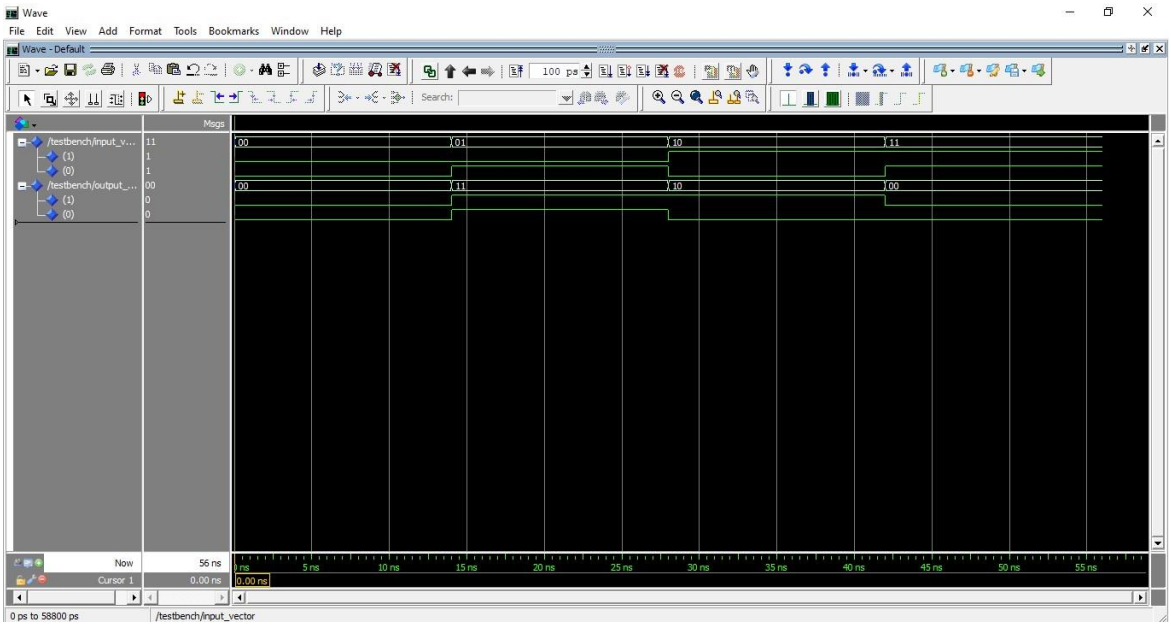
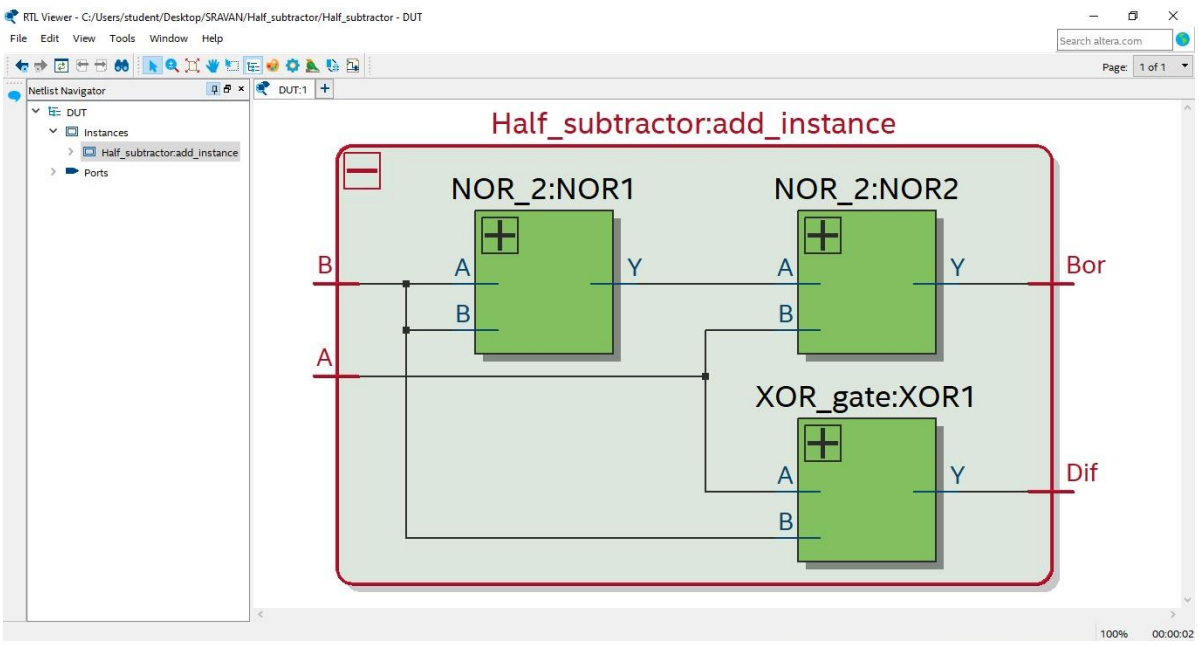
- ModelSim Waveforms



- RTL Netlist viewer



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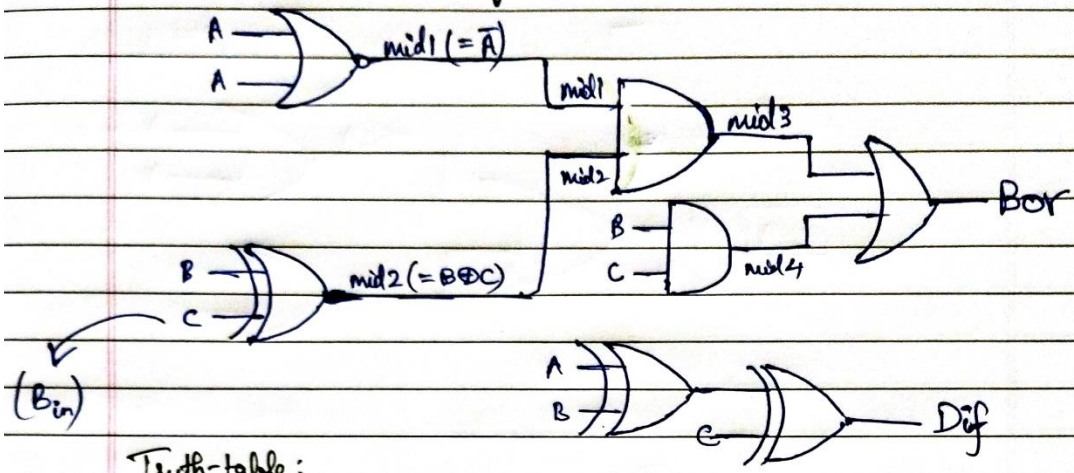
Lab Report (Expt. 1)

❖ AND gate using NOR

- Pen-paper design

5] Full-subtractor using AND, OR, XOR and NOR gates



Truth-table:

A	B	C (= B_{in})	Dif	Bor
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

CONCLUSIONS:

1] A minimum of 3 NOR gates were required to design AND gate.
2] A minimum of 2 NOR gates were required to design OR gate.
3] A minimum of 5 NOR gates were required to design XOR gate.
4] Half subtractor can be built by using 2 NOR gates and a XOR gate.
5] Full subtractor can be built using 3 XOR, 2 AND, 1 OR and 1 NOR gate.

Sayan Dutta
11/08/2023

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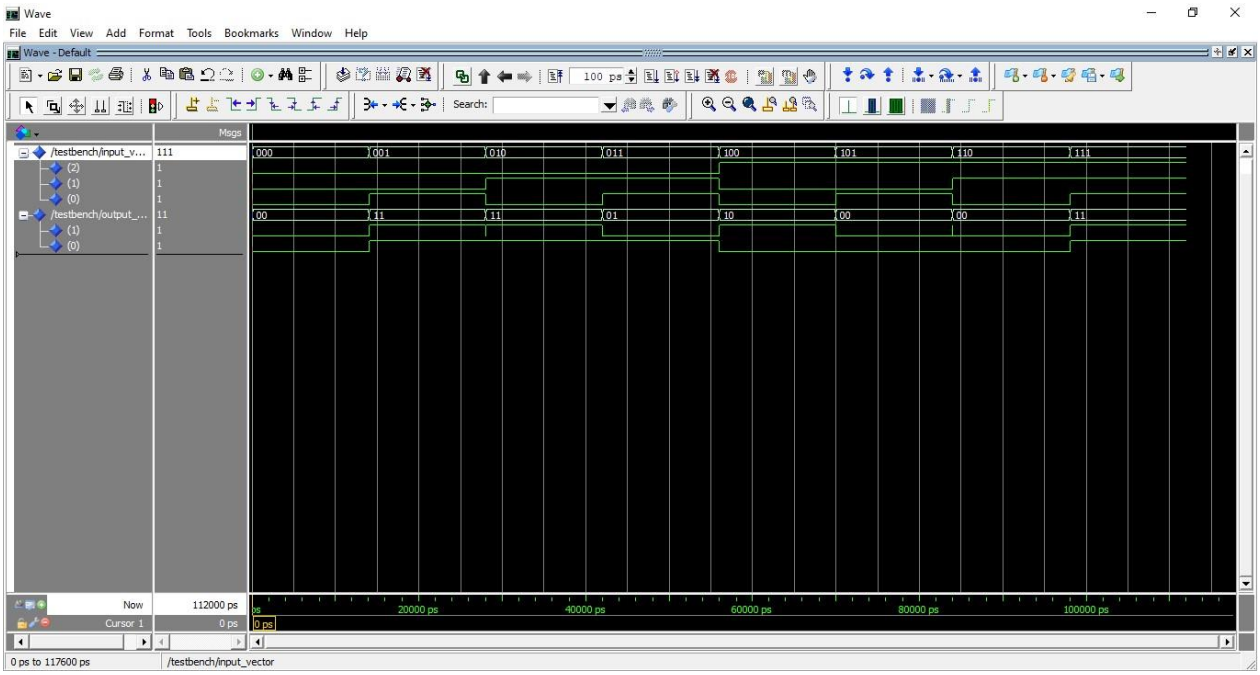
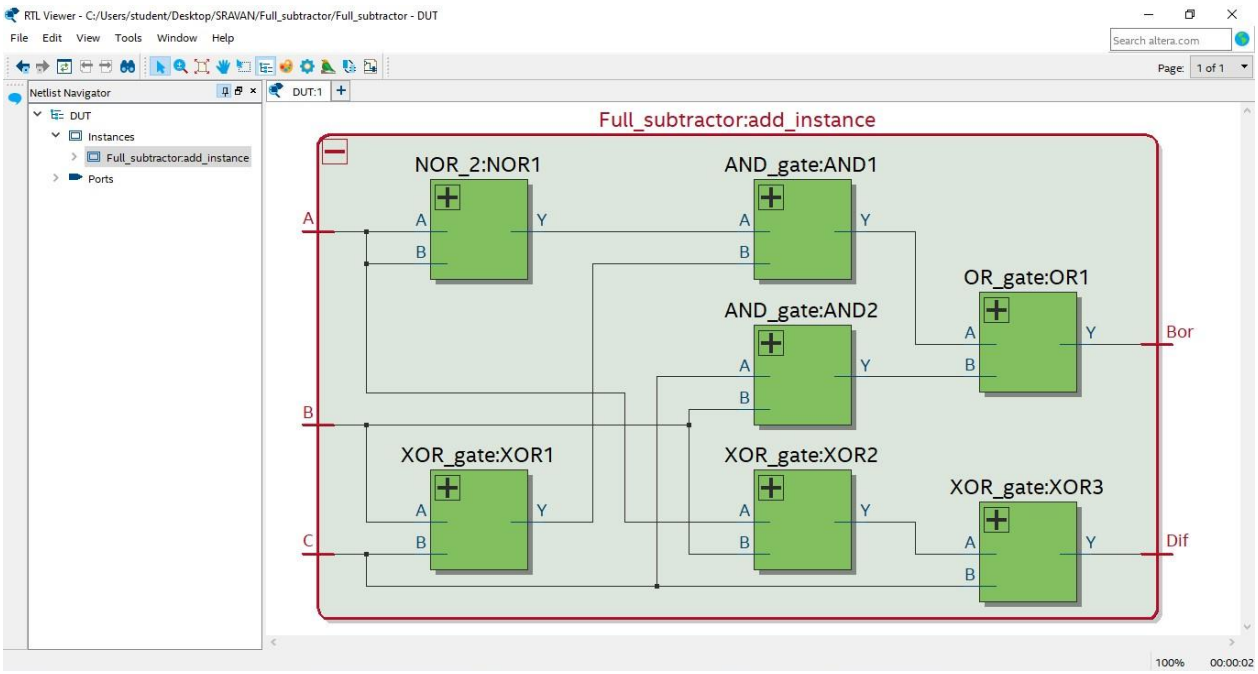
- ModelSim Waveforms



- RTL Netlist viewer



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