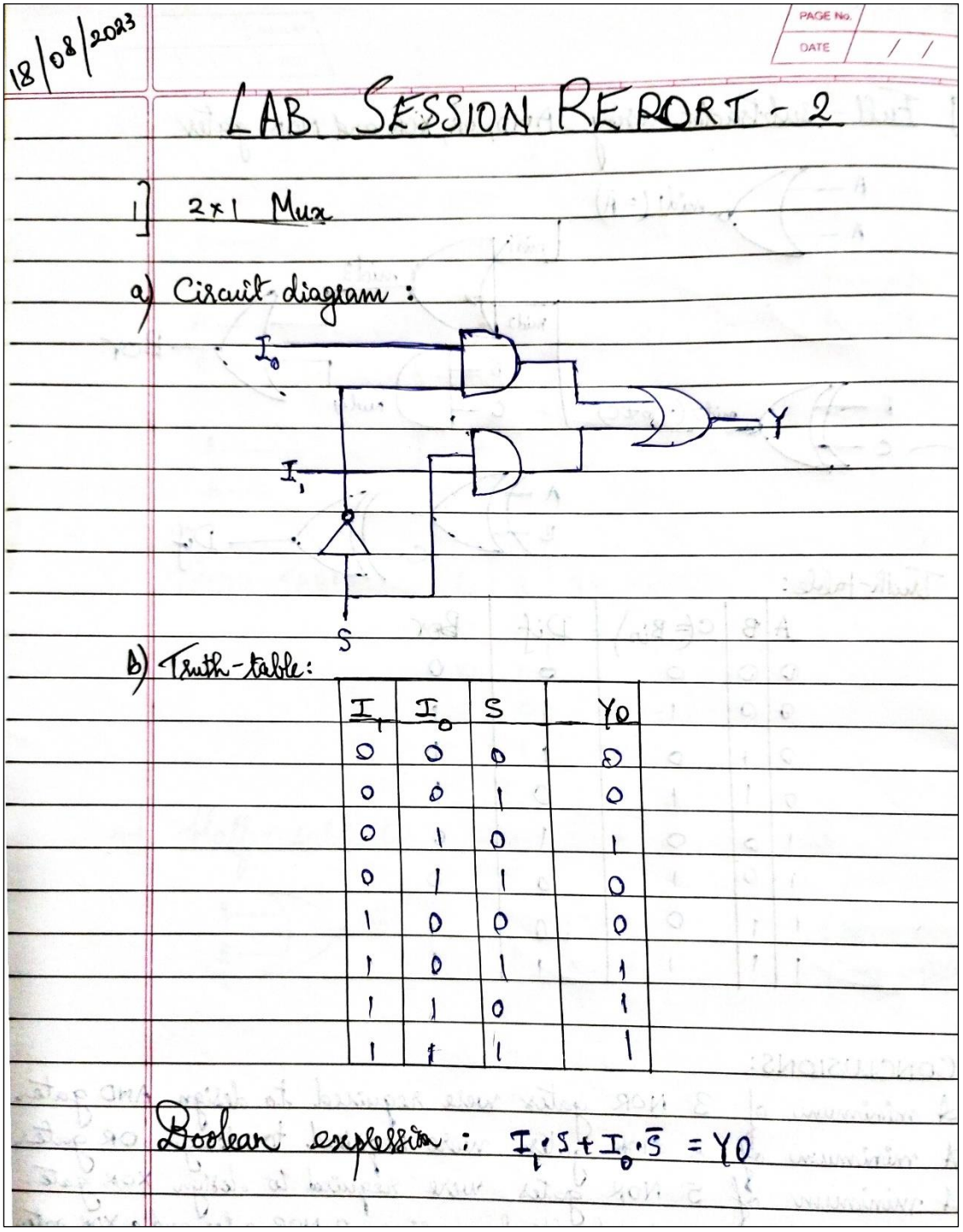
EE-214 (Digital Circuits Lab)
Lab Report (Expt. 2)

❖ 2×1 MUX gate using gates

- Circuit Diagram



18/08/2023

PAGE No.
DATE / /

LAB SESSION REPORT - 2

1] 2×1 Mux

a) Circuit diagram :

b) Truth-table:

I_1	I_0	S	Y0
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Boolean expression : $I_1 \cdot S + I_0 \cdot \bar{S} = Y0$

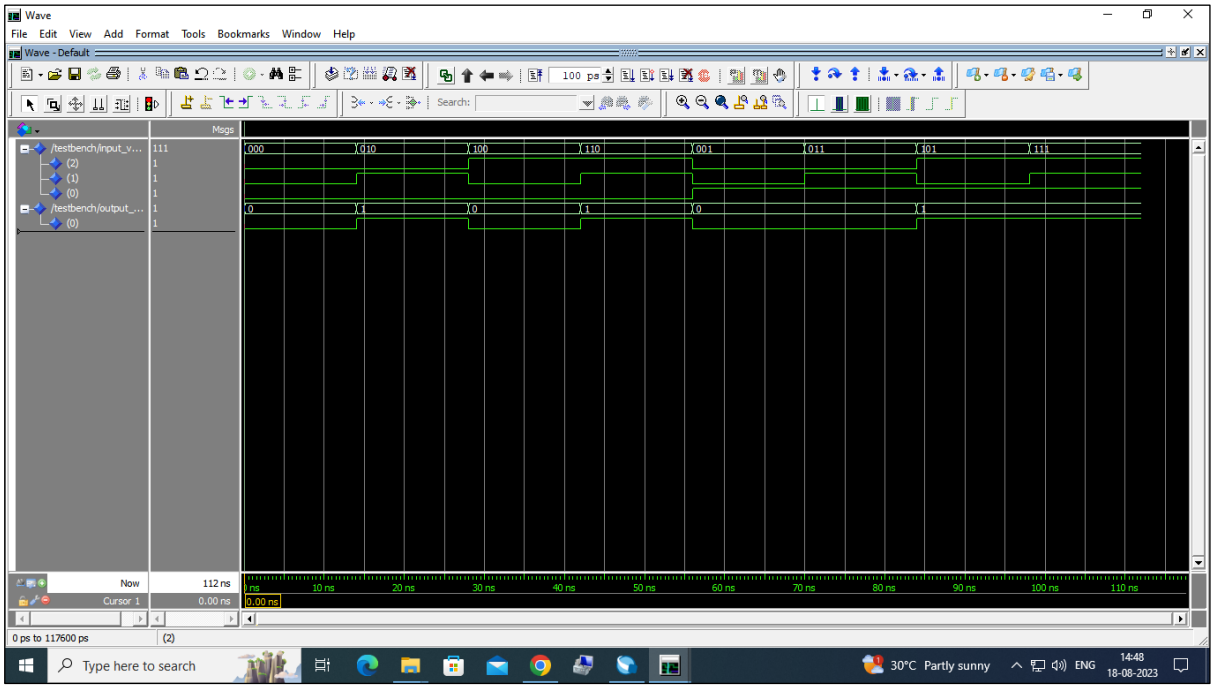
Name: *Sravan K Suresh*

Roll no: 22B3936

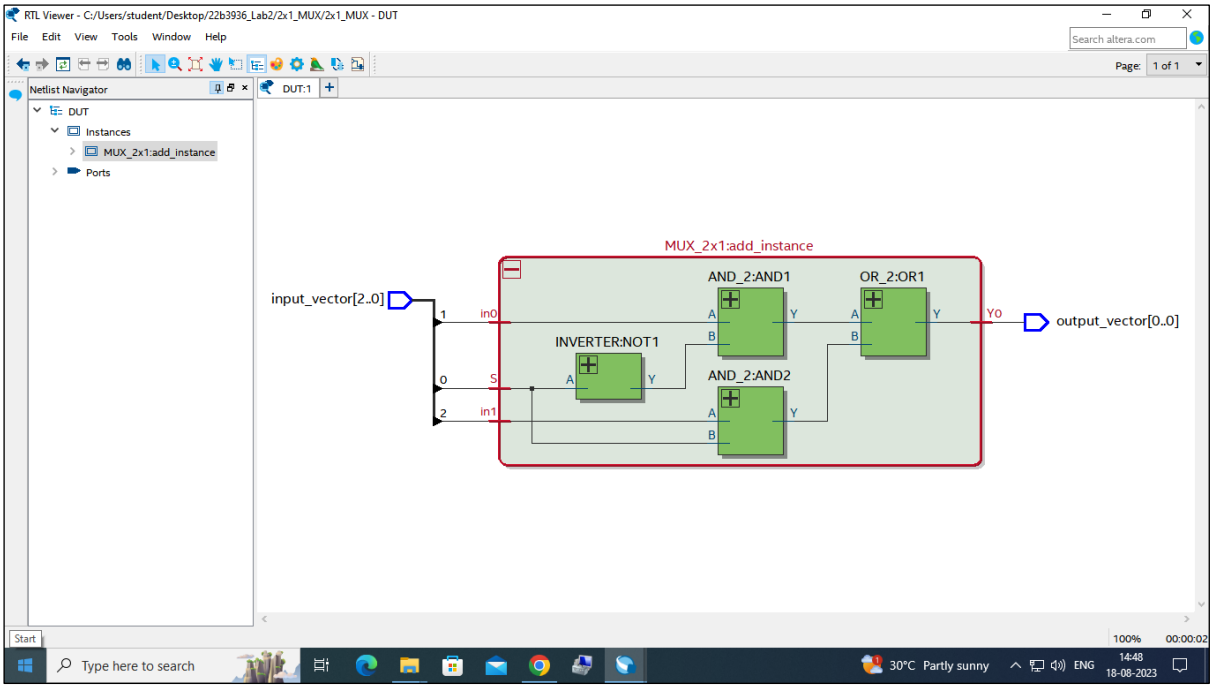
Batch: Friday

EE-214 (Digital Circuits Lab)
Lab Report (Expt. 2)

- ModelSim Waveforms



- RTL Netlist viewer



Name: *Sravan K Suresh*

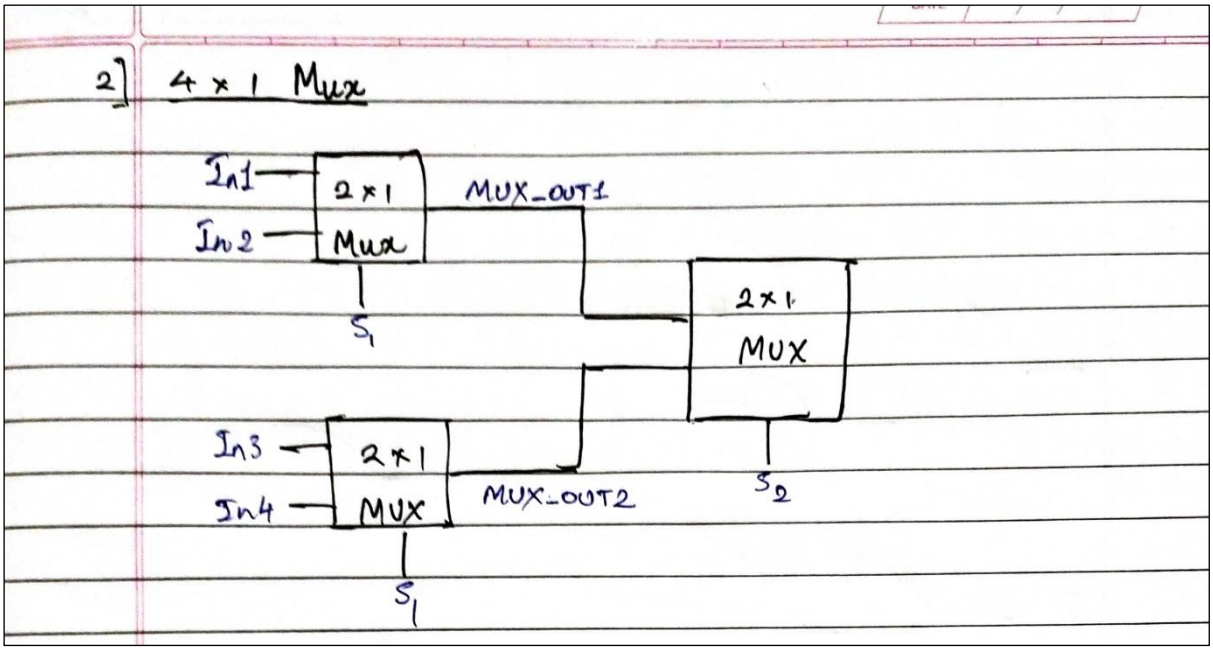
Roll no: 22B3936

Batch: Friday

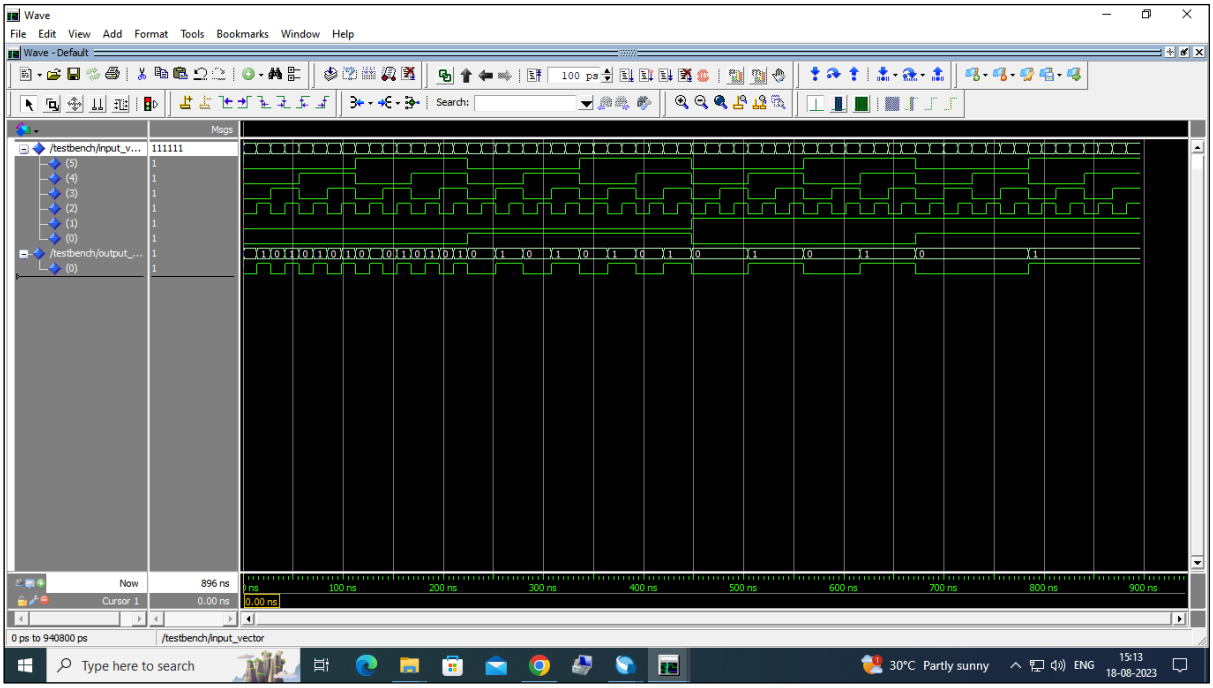
EE-214 (Digital Circuits Lab)
Lab Report (Expt. 2)

❖ 4×1 MUX gate using 2×1 MUX

- Circuit Diagram



- ModelSim Waveforms



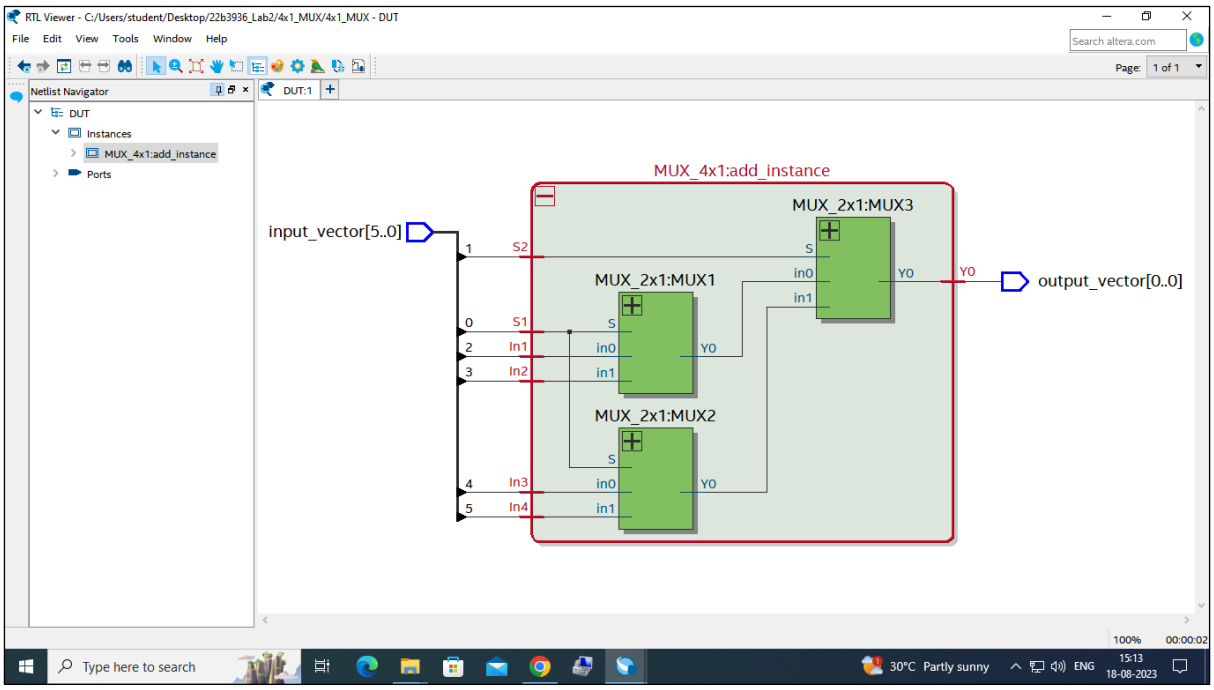
Name: *Sravan K Suresh*

Roll no: 22B3936

Batch: Friday

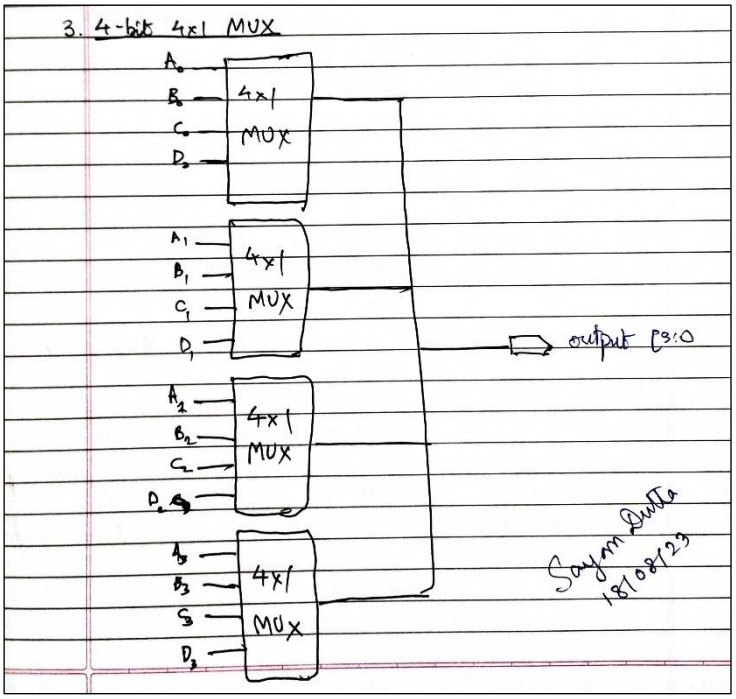
EE-214 (Digital Circuits Lab)
Lab Report (Expt. 2)

- RTL Netlist viewer



❖4-bit 4×1 MUX gate using 4×1 MUX

- Circuit Diagram



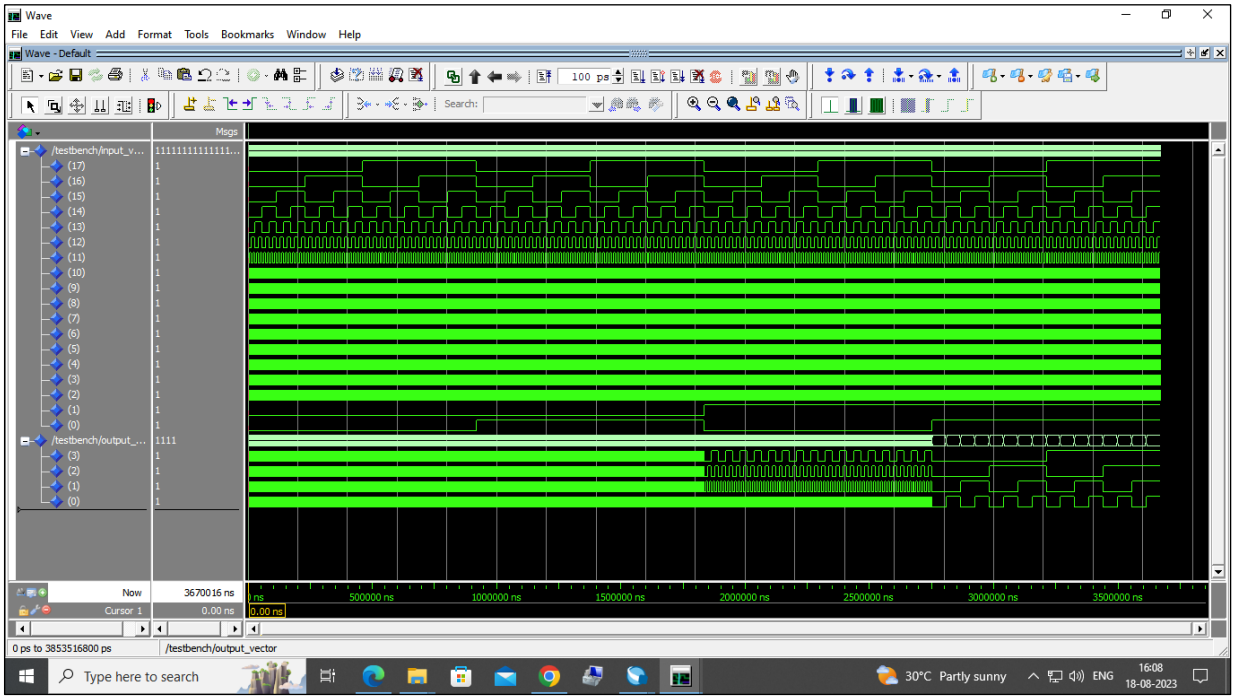
Name: *Sravan K Suresh*

Roll no: 22B3936

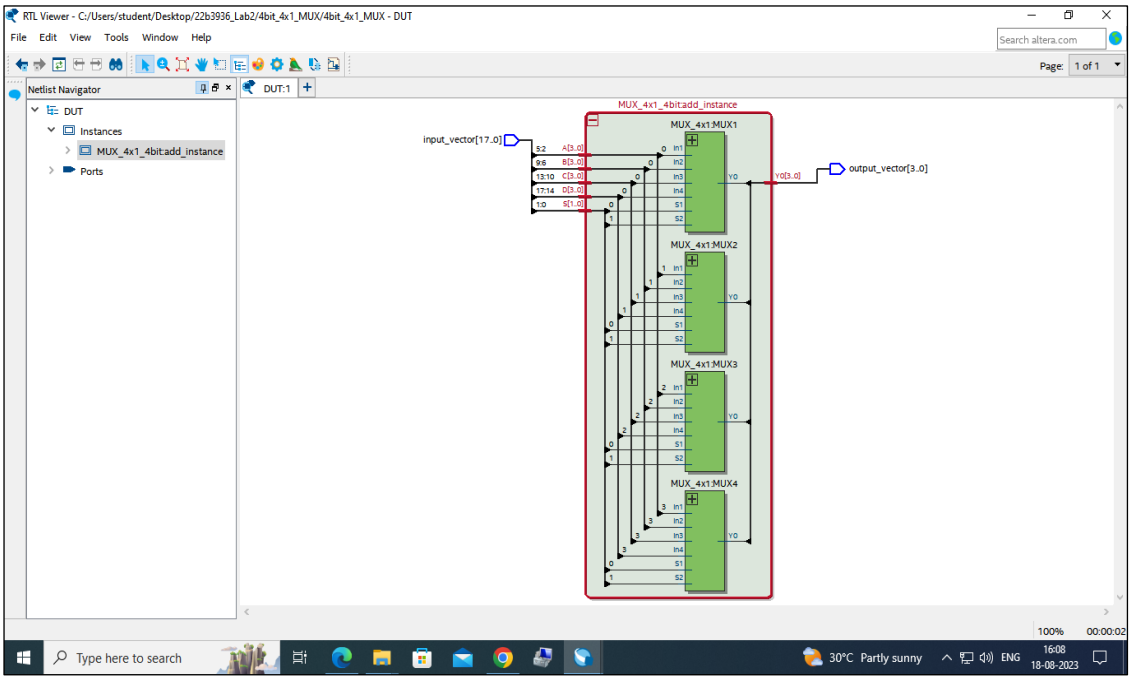
Batch: Friday

EE-214 (Digital Circuits Lab)
Lab Report (Expt. 2)

- ModelSim Waveforms



- RTL Netlist viewer



Name: *Sravan K Suresh*

Roll no: 22B3936

Batch: Friday