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Title Of Project:

Design of 4-bit LUT and analysis of

- **(i)** Transient Response
- **(ii)** Power analysis
- **(iii)** Delay analysis
- **(iv)** Power and delay calculation at corner process

ABSTRACT:

This reports presents the design and analysis of a 4-bit Look-Up Table (LUT) using the Cadence Virtuoso tool for digital circuit applications. The LUT is a fundamental component in Field-Programmable Gate Arrays (FPGAs), enabling flexible implementation of logic functions. In this design, the 4-bit LUT is implemented at the transistor level using CMOS technology. The schematic design process involves the creation of memory cells(D flipflop) and multiplexers to realize the LUT's functionality.

The primary focus of this work includes power and delay optimization for the 4-bit LUT. Power consumption and delay are critical metrics for evaluating the performance of digital circuits, particularly in low-power applications. Post-layout simulations are conducted to analyze the power dissipation and propagation delay. The power is measured in terms of dynamic and static components, and the delay is assessed from input to output transitions under different load conditions.

INTRODUCTION:

LUTs enable the efficient implementation of logic functions by storing precomputed outputs for all possible input combinations. A 4-bit LUT, for instance, can realize any function with four inputs, making it a versatile component in digital designs.

The 4-bit LUT design is implemented using CMOS technology, where the LUT stores 16 possible output values corresponding to the 16 input combinations. A multiplexer-based structure is used to select the correct output for a given input combination.

The power and delay characteristics of the designed LUT are critical for evaluating its performance, especially in low-power and high-speed applications. Delay refers to the time taken for a signal to propagate through the circuit, which directly impacts the operational speed of the system.

To ensure the robustness of the design across varying environmental and process conditions, corner analysis is performed. Corner analysis simulates the circuit under different fabrication process corners (e.g., fast-fast, slow-slow, typical-typical) and varying voltage and temperature conditions. This analysis helps in understanding the worst-case performance of the LUT in terms of power and delay.

LOOK UP TABLE:

A Look-Up Table (LUT) is a fundamental building block in digital systems, particularly in programmable logic devices such as Field-Programmable Gate Arrays (FPGAs). LUTs are used to implement combinational logic functions efficiently by storing precomputed output values for all possible input combinations.

In a general sense, an n-bit LUT can implement any Boolean function with n inputs by storing 2^n output values. For example, a 4-bit LUT, which is the focus of this design, can map 16 different input combinations (from 0000 to 1111) to their respective output values. The LUT behaves as a truth table where each row corresponds to a unique input combination, and the stored value at that location is the desired output.

LUTs are crucial in FPGAs because they provide flexibility in implementing various logic circuits without requiring the circuit to be hardwired. By changing the contents of the LUT, different logic functions can be realized without altering the hardware itself.

As the number of input bits increases, the size of the LUT grows exponentially, which can impact the area, power consumption, and delay of the circuit.

TRUTH TABLE:

A 4-bit LUT can realize any combinational logic function of 4 inputs. With 4 inputs, there are \(2^4 = 16\) possible input combinations. The LUT stores a precomputed output for each combination of the inputs.

-Inputs: A, B, C, D (4 input bits)

- Output: F (Function output)

The truth table for the 4-bit LUT has 16 rows, one for each input combination. The specific values of the output (F) will depend on the particular function the LUT is designed to implement. Below is a generic truth table where the output values can be defined based on the desired logic function.

A	B	C	D	F
0	0	0	0	F(0)
0	0	0	1	F(1)
0	0	1	0	F(2)
0	0	1	1	F(3)
0	1	0	0	F(4)
0	1	0	1	F(5)
0	1	1	0	F(6)
0	1	1	1	F(7)
1	0	0	0	F(8)
1	0	0	1	F(9)
1	0	1	0	F(10)
1	0	1	1	F(11)
1	1	0	0	F(12)
1	1	0	1	F(13)
1	1	1	0	F(14)
1	1	1	1	F(15)

GENERAL BLOCK DIAGRAM OF LUT:

A Look-Up Table (LUT) consists of memory elements and a multiplexer (MUX) that selects the appropriate stored value based on the input combination. The block diagram for an n-bit LUT generally follows the same structure, regardless of the number of inputs.

For a 4-bit LUT, the block diagram will have:

- 4 input bits (A, B, C, D)

- 16 stored values (since \(2^4 = 16\)) corresponding to the possible input combinations

- A 16-to-1 multiplexer to select the appropriate output value based on the inputs.

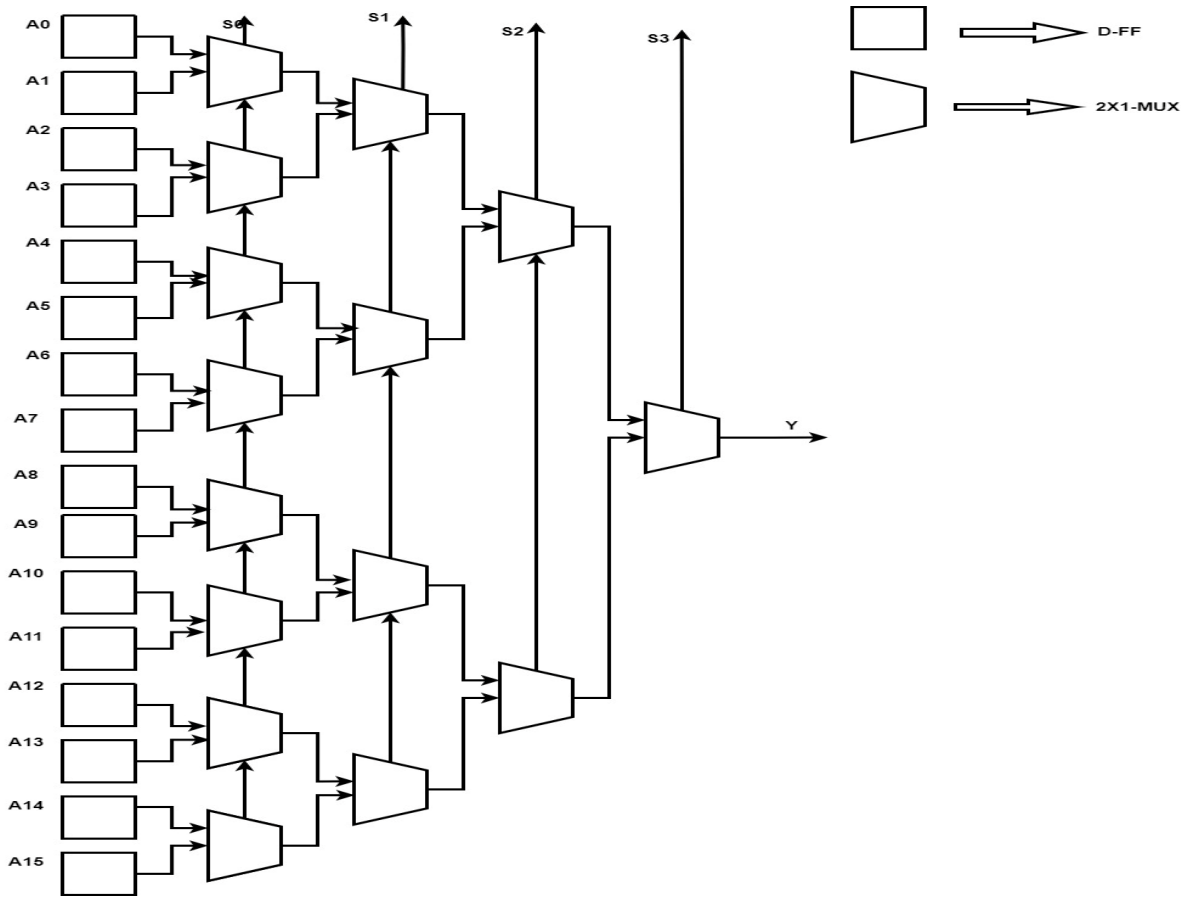

Fig 1:Block Diagram of 4-Bit LUT

BASIC BLOCKS USED IN DESIGN OF LUT:

NOT GATE: Used as inverter. Expression : Y = A';

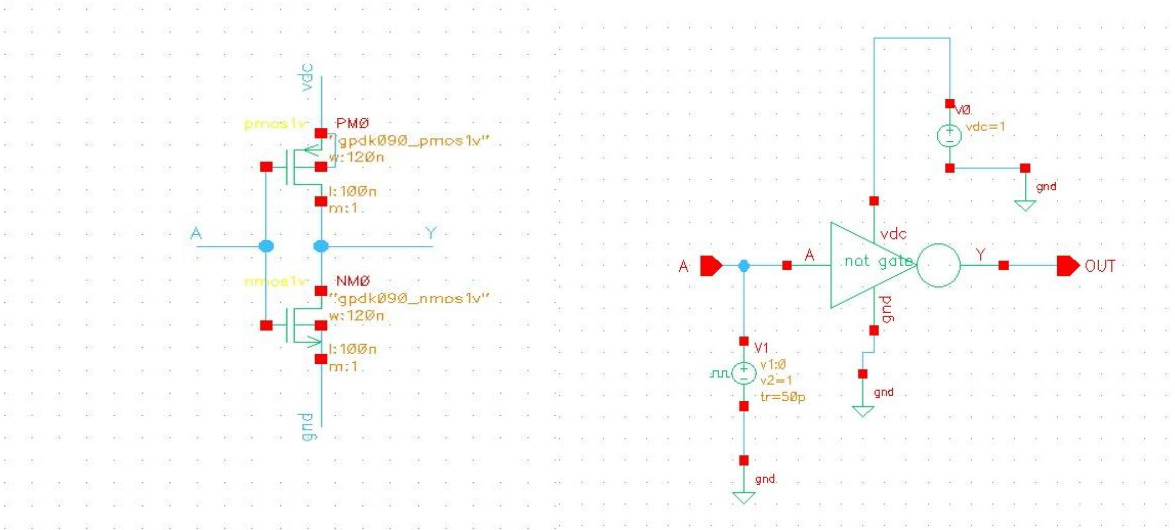

Fig 2:Not Circuit with symbol

AND GATE:

Used for multipliation. Expression: Y=AB;

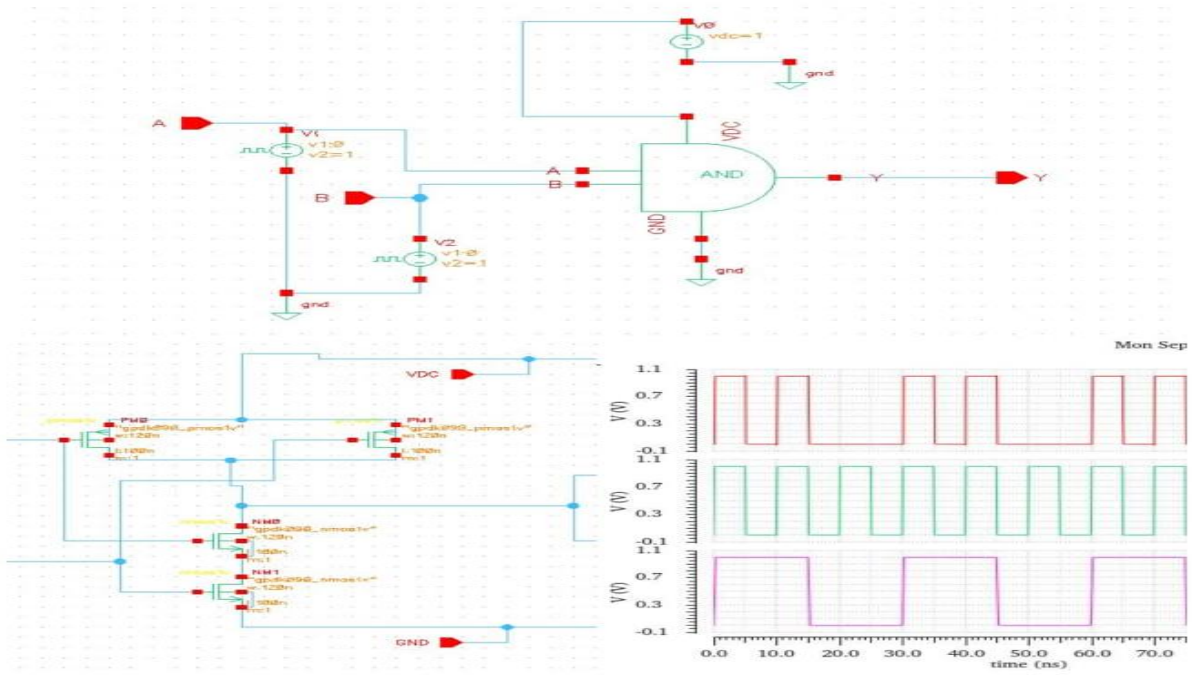

Fig 3: AND Circuit,symbol, and Wave Form

NOR GATE:

It is an inverted OR gate. Expression: Y= (A+B)';

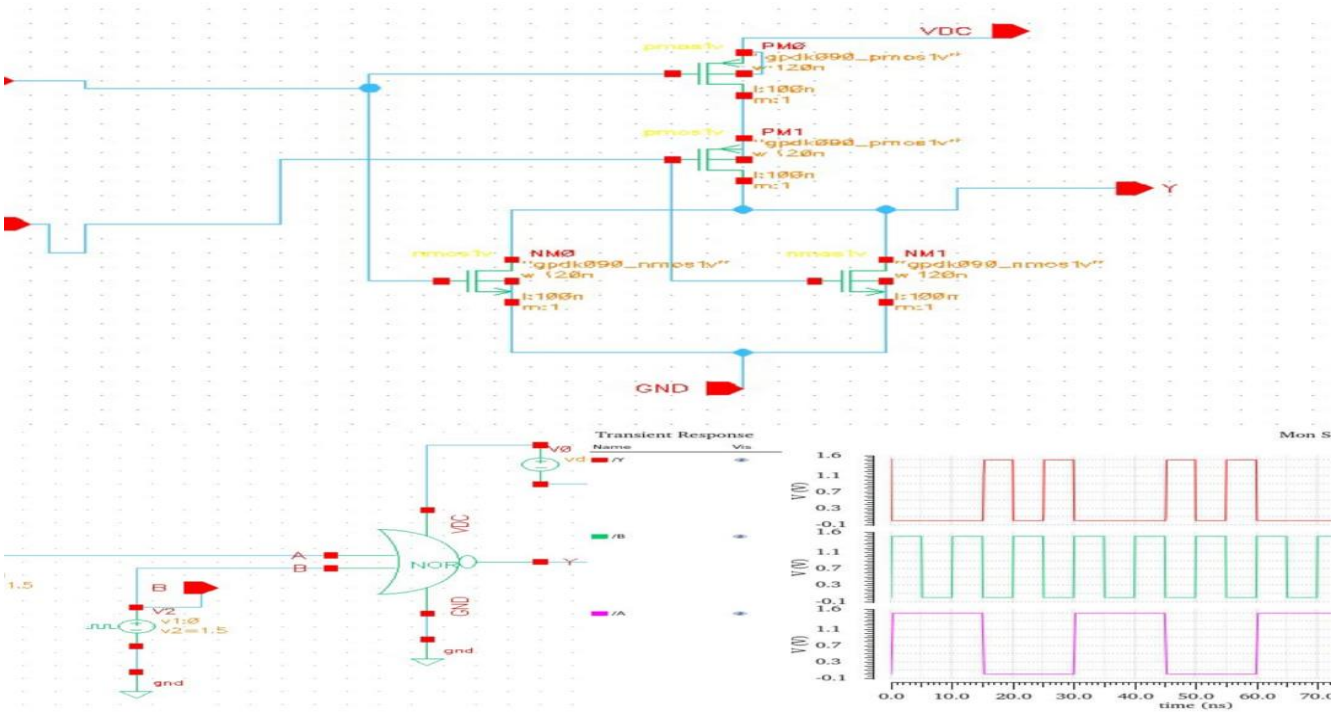

Fig 4: NOR circuit,Symbol, and Wave Form

2X1 MULTIPLEXER:

A multiplexer is a combinational circuit that has many data inputs and a single output, depending on control or select inputs. For N input lines, log2(N) selection lines are required, or equivalently, for 2n2*n* input lines, n selection lines are needed. It has various applications in digital systems such as in microprocessor it is used to select between two different data sources or between two different instructions.

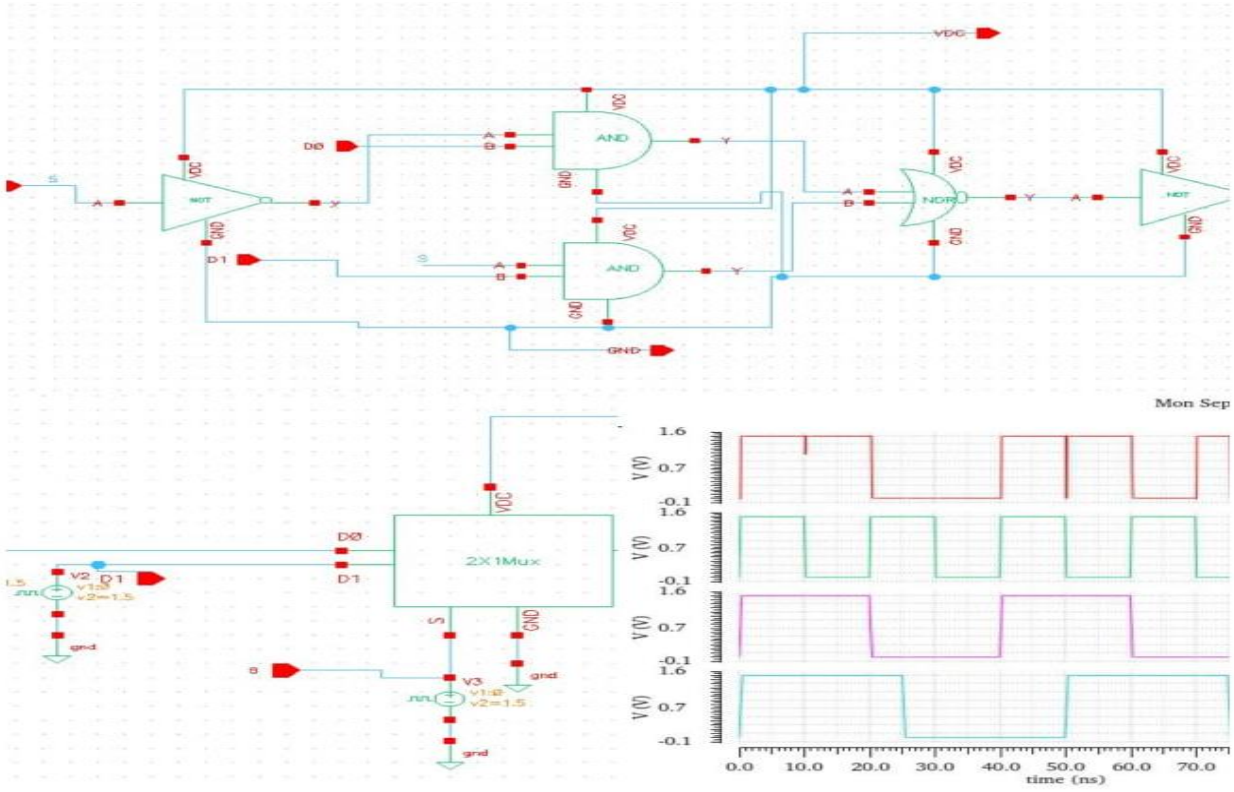

Fig 5: 2x1-MUX circuit, Symbol, and wave Form.

D-FLIFLOP:

It act as a memory element in design of LUT. Flip Flop is an electronic device or to be precise a kind of memory component that can hold one bit of data. A flip flop has two states, that is “SET” and “RESET”. Those states are represented with the binary values 0 and 1. The flip flop remains in its current state until its receives a signal that switches it to opposite state. A clock or pulse signal may “trigger” the flip flop to change state.

D flip flop is an electronic devices that is known as “delay flip flop” or “data flip flop” which is used to store single bit of data.

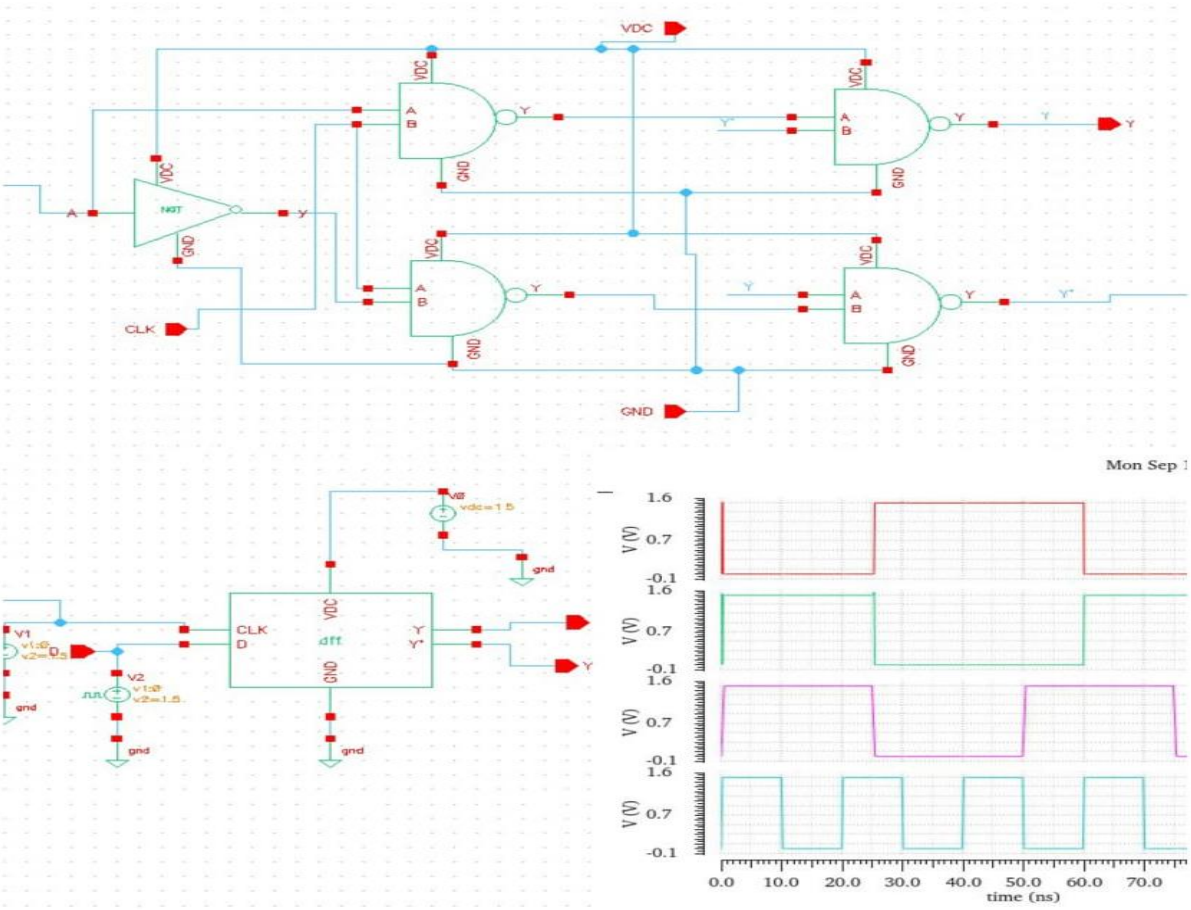

Fig 6: D-Flip Flop Circuit,Symbol, and Waveform

SCHEMATIC OF 4 bit-LUT:

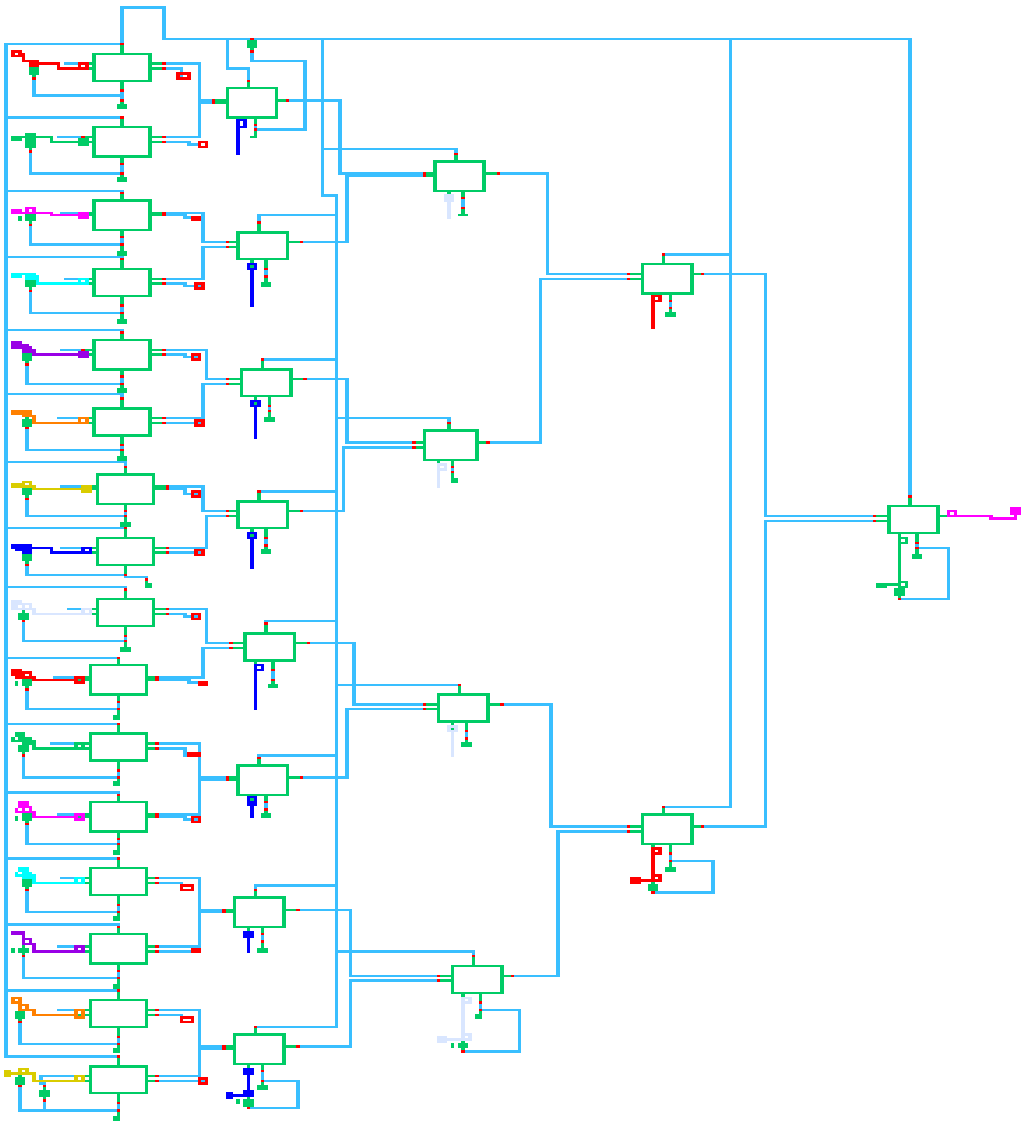

Fig 7: Schematic of 4-bit LUT in Cadence

FUNCTIONS OF LUT:

(i) F = ABCD(4 bit and gate)

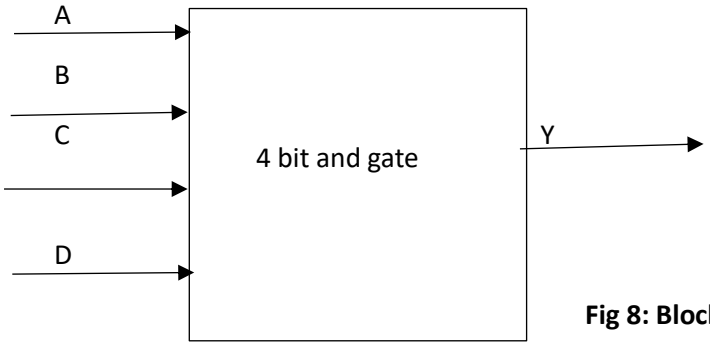

Fig 8: Block Diagram of 4-bit AND gate

TRUTH TABLE:

A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

WAVEFORM FOR FUCNTION 1:

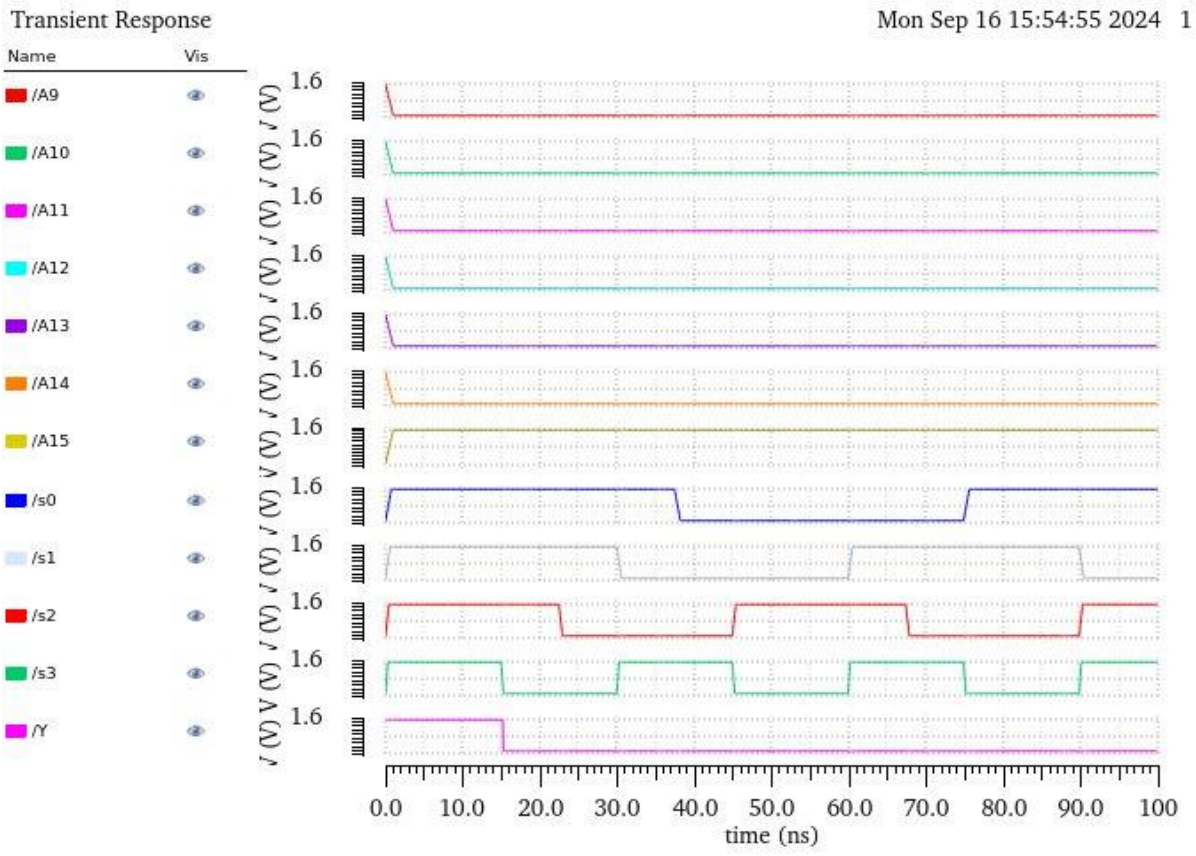

Fig 9: Waveform for Function 1(ABCD) with inputs

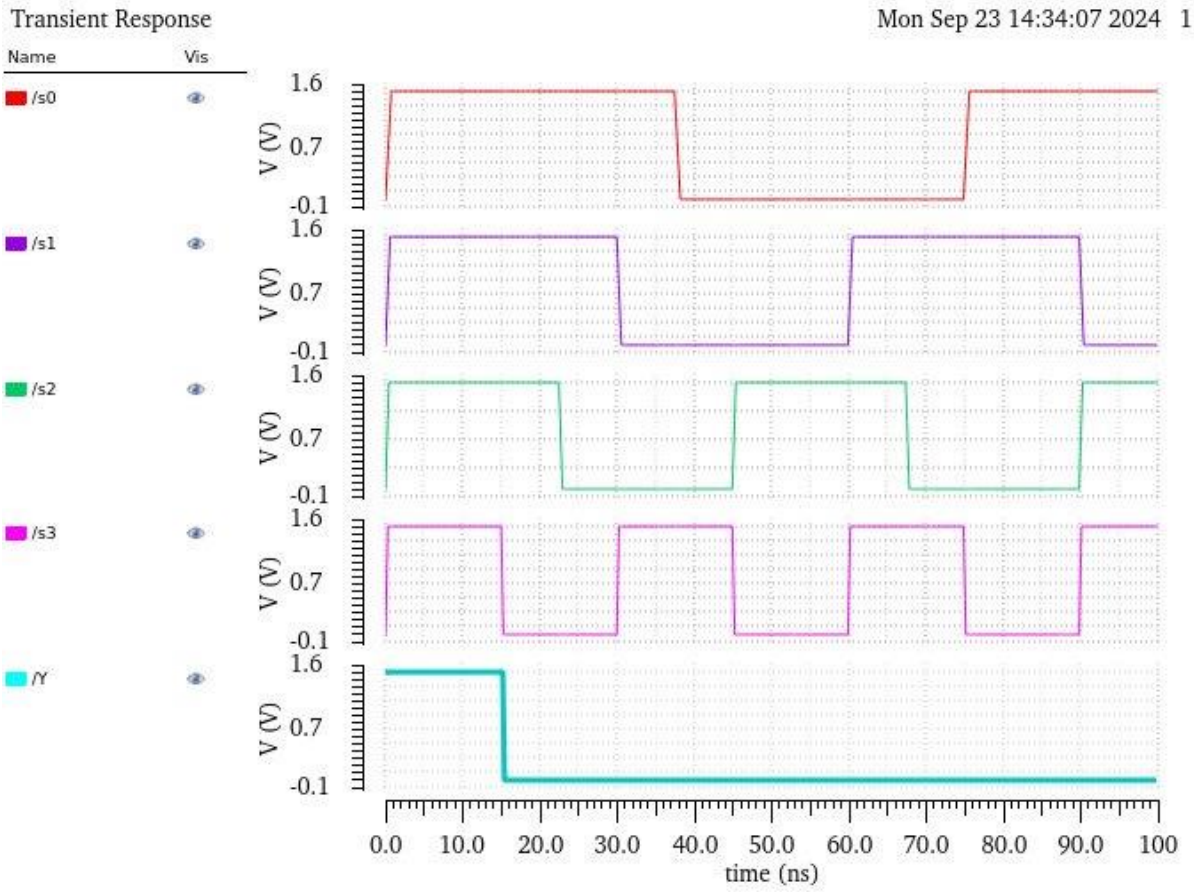

Fig 10: Waveform for function 1(ABCD) with select inputs

(ii) F = A'BCD

TRUTH TABLE:

A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

WAVEFORM FOR FUNCTION 2:

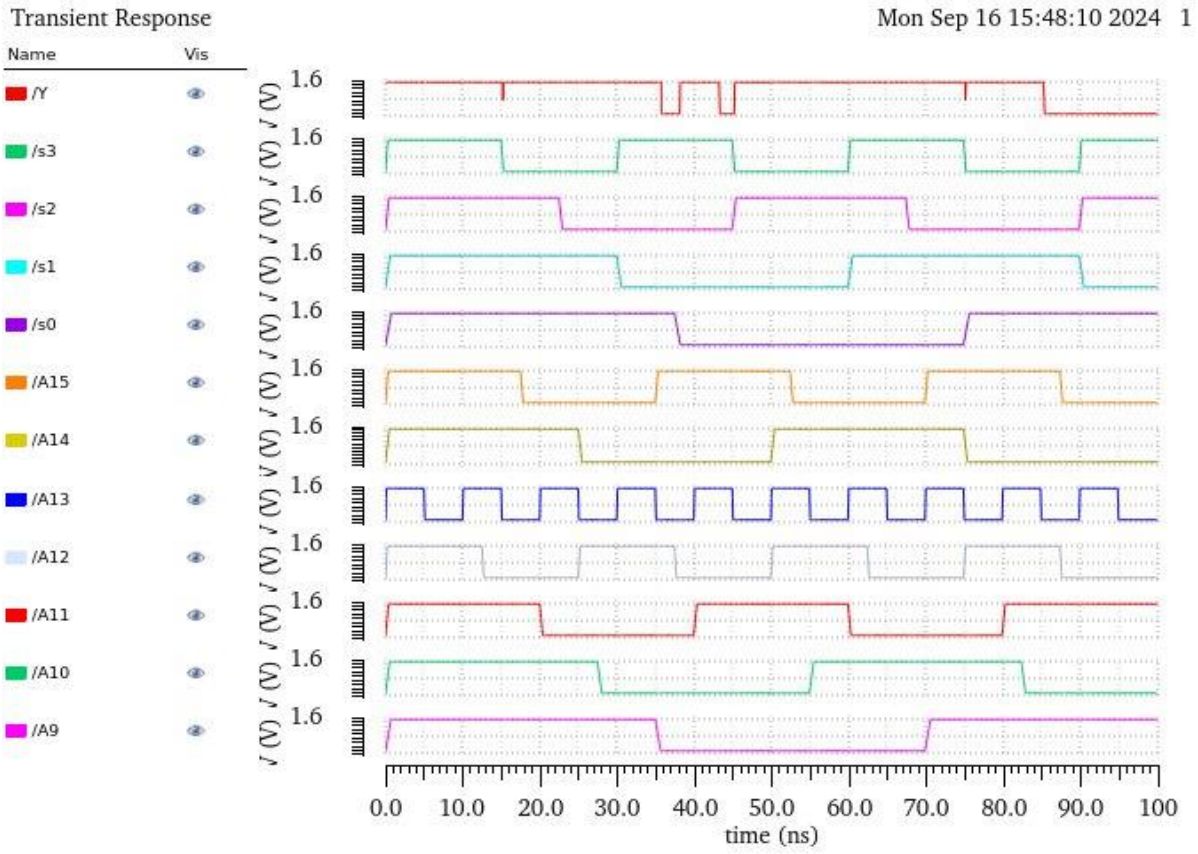

Fig 11: Waveform for function2(A'BCD) with inputs

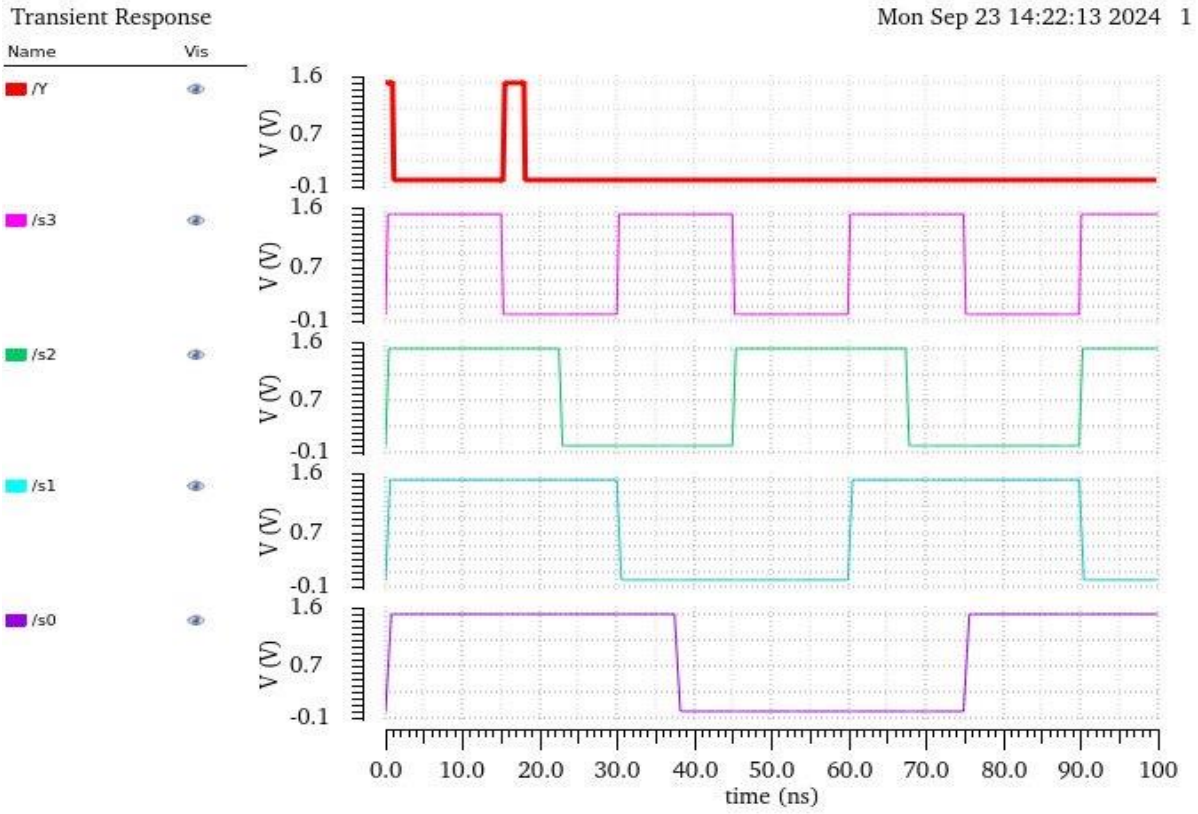

Fig 12: Waveform for function2(A'BCD) with Select lines

AVERAGE POWER CALCULATIONS BY CORNER ANALYSIS:

S.NO	NN	SS	FF	FS
Function 1	111.1E-6	70.07E-6	154.7E-6	143.1E-6
Function 2	111.1E-6	75.98E-6	154.6E-6	143.0E-6

Function 1: ABCD (1111)

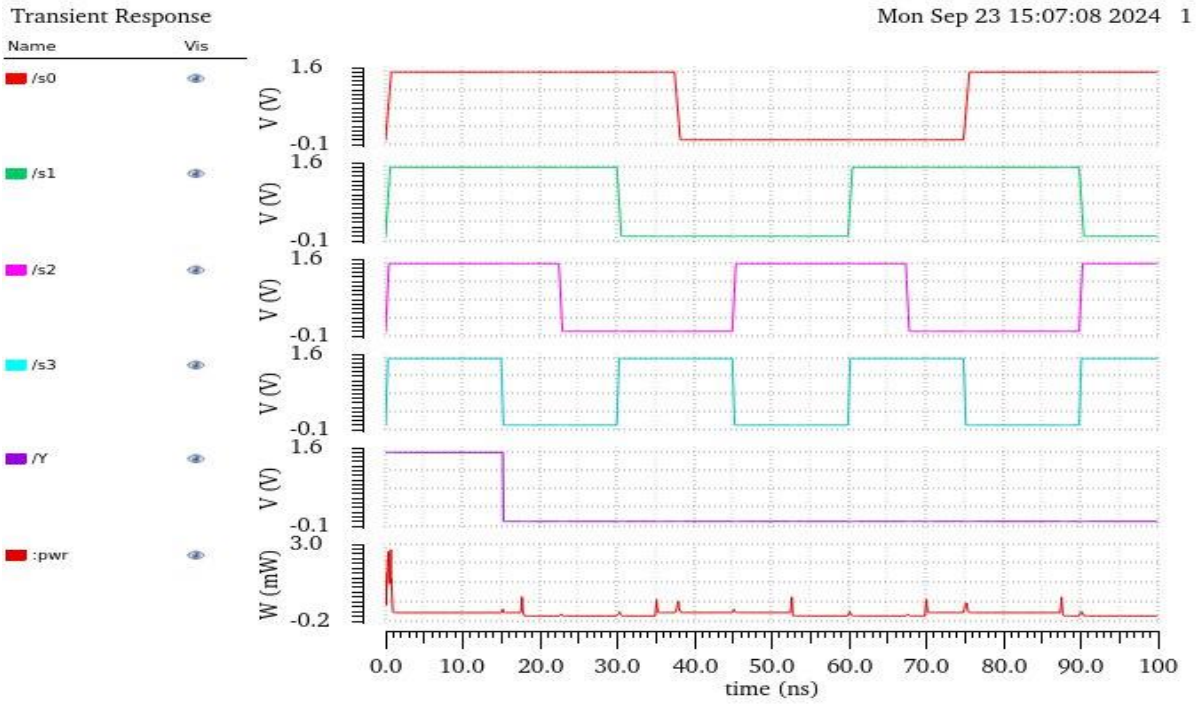

Fig 13: Waveform of power for function1(ABCD)

Function 2: A'BCD (0111) 5

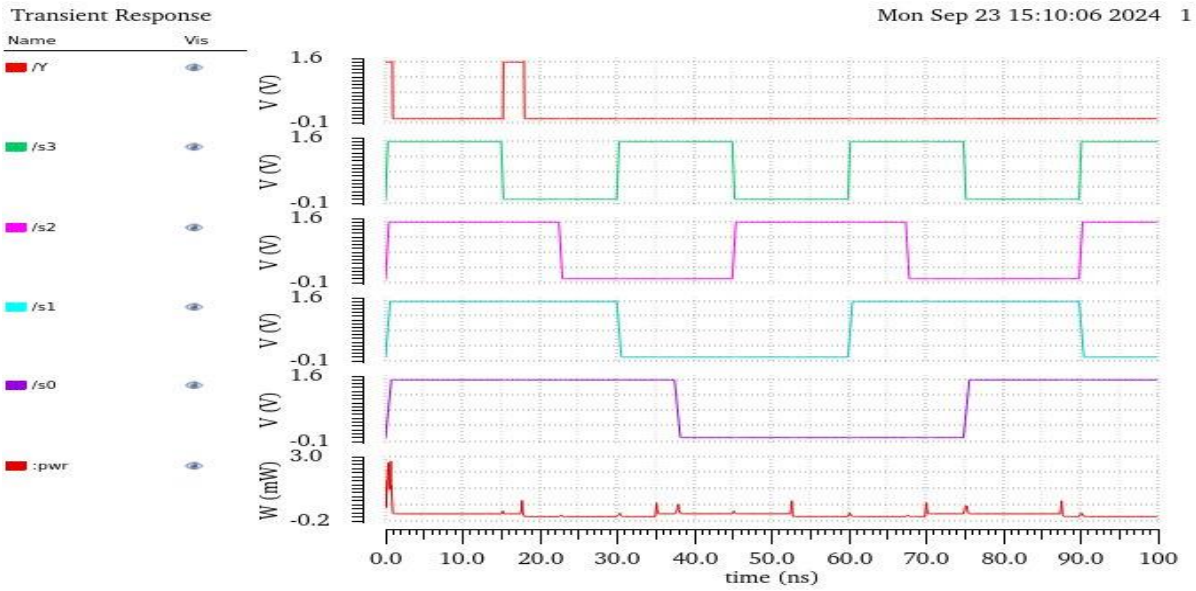

Fig 14: Waveform of power for function2(A'BCD)

Among the value of powers in different corners, maximum power (154.7E-6) obtained in the schematic at the Fast Fast (FF) corner. The minimum power (70.07E-6) obtained at the Slow Slow (SS) corner. At the Nominal Nominal corner, power obtained in the middle range between fast fast and slow slow.

DELAY CALCULATIONS FOR FUNCTION 1:

S.NO	INPUT	OUTPUT	Rising – falling
1.	S0	Y	14.88E-9
2.	S1	Y	14.95E-9
3.	S2	Y	15.02E-9
4.	S3	Y	15.10E-9

These delay values had calculated at the nominal nominal corner. The delay values calculated between one input signal transition to output signal transition. The variations between the different delay values were very small.

CONCLUSION:

The design and implementation of a 4-bit Look-Up Table (LUT) demonstrate the versatility and efficiency of LUTs in digital logic systems, particularly in reconfigurable hardware like FPGAs. By precomputing and storing output values for all possible input combinations, the LUT offers a fast and flexible way to realize any combinational logic function.

Key insights from the project include:

1. Efficient Logic Implementation: The 4-bit LUT can implement any Boolean function with 4 inputs by storing 16 precomputed output values. This flexibility makes it a crucial building block in programmable logic devices, where functions may need to change dynamically without altering hardware.
2. Power and Delay Optimization: The transistor-level implementation of the LUT, particularly with D-FF memory cells and efficient multiplexers, allows for optimizations in power consumption and delay. Proper design choices in these areas help meet the requirements of low-power, high-speed digital systems.
3. Corner Analysis: Through detailed power, delay, and corner analysis, the 4-bit LUT is validated for reliable operation across varying process, voltage, and temperature conditions, ensuring in real-world applications.

In conclusion, the 4-bit LUT offers a fundamental and highly adaptable solution for implementing digital logic. Its speed, flexibility, and scalability make it an indispensable component in modern digital design, particularly for applications requiring reconfigurable logic and efficient combinational function realization. The results of the project highlight the importance of balancing performance metrics such as power, delay, and area in practical circuit design.