IV simulation of NMOS for Long and short Channel

AIM: Simulating I-V Characterstics of Nmos using 180 nm Technology

SOFTWARE USED: cadence Virtuoso

PROCEDURE:

- **Create a Schematic**:
- Open Cadence Virtuoso and create a new schematic cell.
- Place an **NMOS transistor** and connect the **gate** to a **DC voltage source** (VGS), the **drain** to another **DC voltage source** (VDS), and the **source** to ground.
- **Set Simulation in ADE**:
- Launch **ADE L/XL**.
- Set up a **DC Sweep** for **VDS** (sweep from 0.5V to 1.5V).
- **Fix VDS** in 3 steps to plot multiple I-V curves.
- **Run the Simulation**:
- Click **Launch → Run** to simulate the circuit.
- **Plot the Results**:
- After simulation, go to **Results → Direct Plot → DC**.
- Plot **ID vs VGS** for each VDS value. • Do same by fixing Vgs for 3 steps and
- Plot **ID vs VDS** for each VGS value.
- **Save/Export the Plot**:
- Save the plot or export it as needed.
- Export as .CSV file next experiment

Long channel NMOS :

In schematic I have taken

W = 1.8 uM

L = 1.8 uM

For Ids vs Vgs plot :
Sweep Vgs and observe the drain current Id by taking Vds values as 0.5v, 1v ,1.5v
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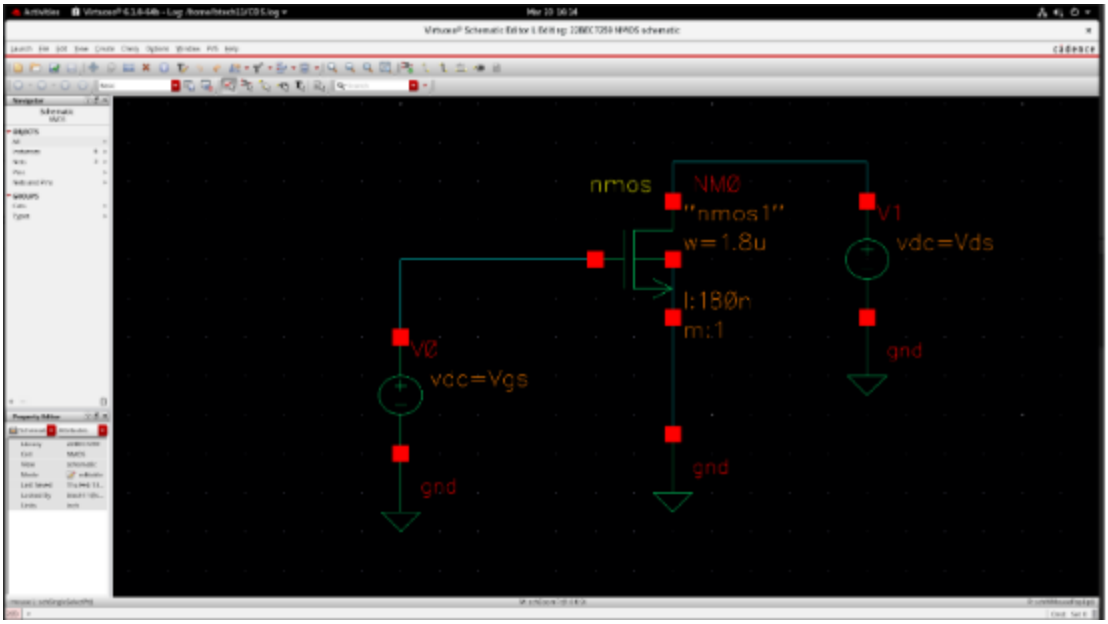
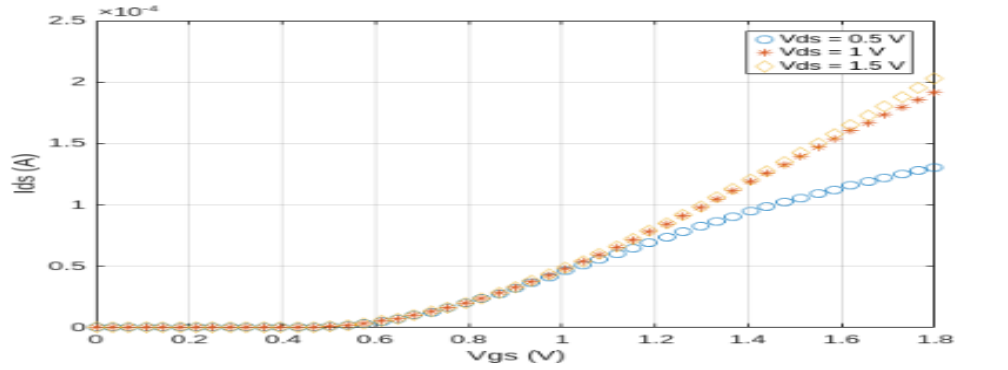
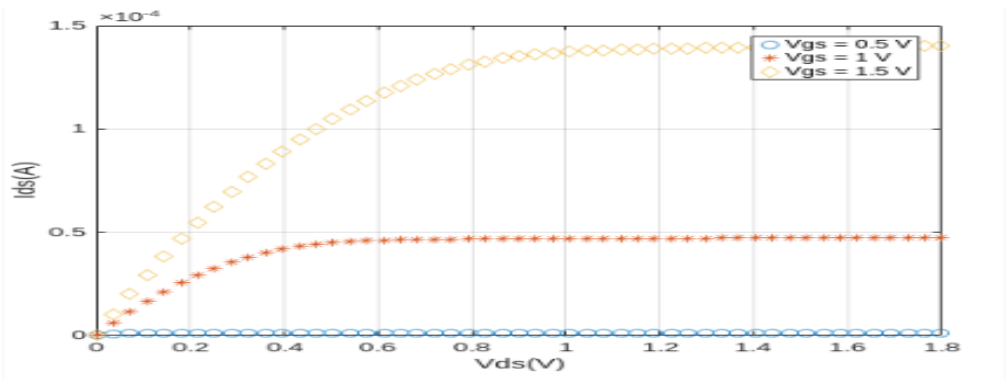
Schematic Representation



Simulation Result :

Id vs Vgs :





Short Channel NMOS:

In schematic I have taken

W = 1.8 uM

L = 0.18

uM For Ids

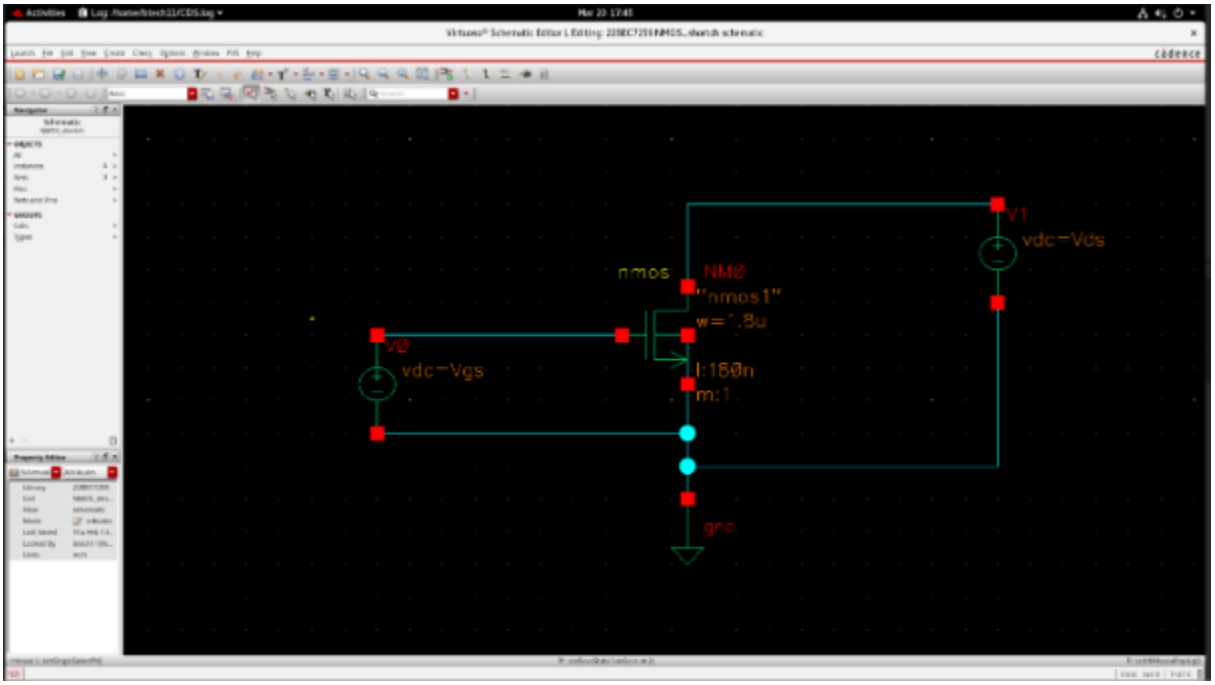
vs Vgs plot :

Sweep Vgs and observe the drain current Id by taking Vds values as 0.5v, 1v ,1.5v For

Ids vs Vds plot :

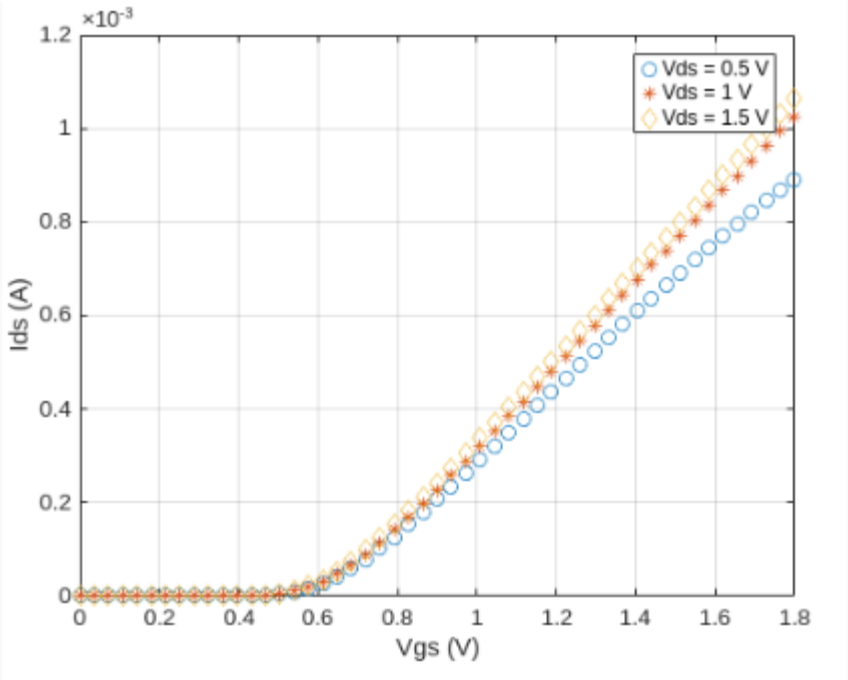
Sweep Vds and observe the drain current Id by taking Vgs values as 0.5v, 1v ,1.5v

Schematic Representation

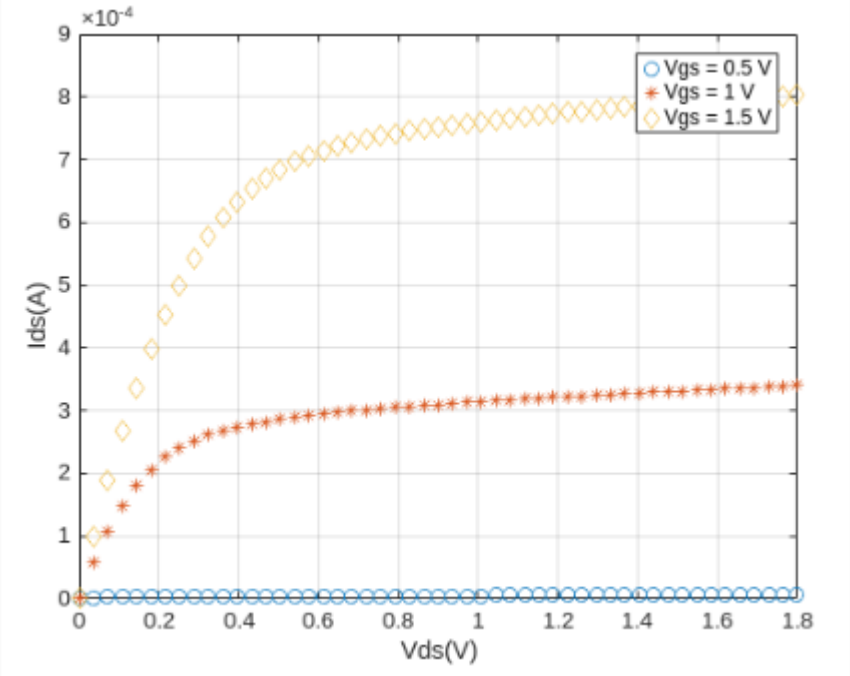


Simulation result :

Id vs Vgs



Id vs Vds



Result:

Simulation of I-V characterstics of Nmos performed