SOURABH TYAGI
LinkedIn || GitHub

E-mail: sourabhtyagi750@gmail.com
Mob: +91 8959541858
Address: Morena, Madhya Pradesh, 476221, India

EDUCATION

- **Vellore Institute of Technology**. **Amaravati-AP, India**
- Pursuing B.Tech in ECE with specialization in VLSI; CGPA: 8.12 June 2022 - June 2026

WORK EXPERIENCE

Summer Intern - CEPDSM at MANIT, Bhopal **June 2024 – July 2024**

- Designed and developed a 3 DOF Robotic Manipulator capable of performing pick-and-place tasks with voice and computer vision control, along with advanced trajectory planning.
- Programming Languages: Python
- Tools & Software: MATLAB, ROS, Autodesk

Treasurer, IEEE MTT **Sep 2023 – Present.**

- VIT-AP University.
- Providing leadership and vision for the organization.
- Developing and implementing strategic plans to achieve organizational goals.

Student Coordinator of VTAPP

- VIT-AP University
- Conducted events like "JUMANJI: Survivor of the Fittest," "Megatron," and "COSMOX" during the tech fest.

SKILLS SUMMARY

Technical Skills

- **Programming Languages:** Python, Java, C
- **Object-Oriented Programming (OOP**): Proficient in OOP principles and methodologies
- **Data Structures and Algorithms (DSA): Strong understanding of data structures and algorithms.**
- **Cloud Computing:** Knowledge of AWS Fundamentals (IaaS, PaaS, SaaS), infrastructure, storage, and networking.
- **Web Development:** Basic knowledge of HTML5 for web page structure and design.
- **Test Equipment:** Proficient in using Multimeter, Signal Generator, and Oscilloscope for circuit testing and debugging.
- **Project Experience:** Used Multimeter, Signal Generator, and Oscilloscope for testing and troubleshooting electronic circuits while designing rectifiers, clippers, and clampers.

VLSI Design

- **HDL Languages**: Verilog, VHDL, SystemVerilog
- **Verification Methodologies**: UVM (Universal Verification Methodology)
- **Physical Design**: Experience in RTL to GDSII flow, floorplanning, placement and routing, clock tree synthesis (CTS), timing closure, and DRC/LVS verification
- **EDA Tools**: Cadence Virtuoso, Xilinx Vivado, LTspice, Multisim, EDA Playground
- **FPGA Development**: Experience with Zynq-7000 and Vivado HLS for high-level synthesis

Programming Tools: PyCharm, Visual Studio Code, Eclipse, IntelliJ IDEA, Keil µVision 4
Soft Skills: Rapport Building, Teamwork, Communication, Problem-Solving.

PROJECTS

AI-Based Blind Stick with Image Detection

- Developed a smart stick for visually impaired individuals to detect object distance and recognize objects using AI, enhancing mobility and safety.
- Integrated sensors to detect the proximity of nearby objects and generate alarm sounds to alert the user.
- Implemented image recognition technology to identify objects and provide voice feedback, allowing users to know the names of objects in their vicinity.
- Designed the system using Python, OpenCV, etc, ensuring real-time object detection and distance calculation.
- Tools & Technologies: Python, OpenCV, TensorFlow, Raspberry Pi.

Design and Implementation of Combinational Circuits using Cadence Virtuoso Links

- **Basic Logic Gates**: Designed Inverter, OR, AND, NAND, NOR, XOR, X-NOR, and Buffer Gates using 90 nm And 45 nm technology on Cadence Virtuoso tools.
- **Arithmetic Circuits**: Designed Half Adder, Full Adder, Half Subtractor, and Full Subtractor using 90 nm technology.
- **Multiplexers and Decoders**: Designed Multiplexers, Demultiplexers, Priority Encoders, and Decoders.
- **Hands-on Experience**: Gained hands-on experience in schematic capture, layout design, and circuit simulation.
- **DRC**: Verified and corrected layout designs to meet 90 nm foundry rules, ensuring manufacturability.
- **LVS:** Ensured accurate layout representation by matching layout with schematic and resolving discrepancies.

Design of a 6T SRAM Cell using Cadence Virtuoso Links

- Designed a 6-Transistor (6T) Static Random Access Memory (SRAM) cell using 90 nm technology in Cadence Virtuoso.
- Simulated and optimized read/write operations to improve key performance metrics, such as power consumption and stability.
- Performed layout design, Design Rule Check (DRC), and Layout Versus Schematic (LVS) checks to ensure design accuracy and fabrication readiness.
- Analyzed critical performance parameters, including Static Noise Margin (SNM), access time, and power dissipation.

ACADEMIC COURSES

- Java with Data Structures and Algorithms (DSA).
- Semiconductor Devices and Circuits
- Microprocessor and Microcontroller
- Analog Devices and Circuits
- NPTEL: Physical Design (RTL to GDS), Static Timing Analysis, CMOS Digital VLSI Design.

CERTIFICATIONS Links

- Summer Intern at MANIT, Bhopal.
- VLSI International Workshop Programming in JAVA.
- MATLAB Onramp.
- VLSI for Beginners.
- Space Science and Technology Awareness Training.