**SOURABH TYAGI**
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## Carrer Objective

Aspiring **VLSI Design Engineer** with a strong foundation in **Digital and Analog Circuit Design**, currently pursuing **B.Tech in ECE** with a specialization in **VLSI**. Experienced in using **Cadence Virtuoso** for designing and simulating **logic gates**, **amplifiers**, and memory circuits including **6T SRAM**. Successfully completed a **50-day design challenge**, showcasing deep hands-on expertise in **schematic**, **layout**, and **validation workflows**. Proficient in **Verilog**, **SystemVerilog**, and **Python**, with a keen interest in contributing to **innovative semiconductor** and **memory technology solutions**.

## WORK EXPERIENCE

**Summer Intern - CEPDSM at MANIT, Bhopal** **June 2024 – July 2024**

- Developed a 3 DOF Robotic Manipulator capable of performing pick-and-place tasks with voice and computer vision control, along with advanced trajectory planning.
- Programming Languages: Python
- **Tools & Software:** MATLAB, ROS, Autodesk

**Treasurer, IEEE MTT**

- Emphasize teamwork and strategic planning skills
- Collaborated with team members to set goals and strategize activities for IEEE events, enhancing team communication and organizational reach.

**Student Coordinator of VTAPP**

- VIT-AP University
- Conducted events like "JUMANJI: Survivor of the Fittest," "Megatron," and "COSMOX" during the tech fest.

## SKILLS SUMMARY

**VLSI Design**

- **HDL Languages**: Proficient in Verilog and System Verilog.
- **Verification Methodologies:** Experienced with UVM (Universal Verification Methodology).
- **EDA Tools:** Skilled in Cadence Virtuoso, Xilinx Vivado, LTspice, Multisim, and EDA Playground.

**Circuit Design & Hardware Testing:**

- **Test and Debug:** Utilized multimeter, signal generator, and oscilloscope for testing and troubleshooting electronic circuits during the design of rectifiers, clippers, and clampers.
- **Analog & Digital Circuit Design**: Experienced in designing power supplies, filters, amplifiers, and logic gates.
- **Mixed-Signal Design:** Proficient in analog circuit design, simulation, and validation using Cadence Virtuoso.

**Technical Skills**

- **Programming Languages:** Python, Java and C.
- **Web Development**: Basic knowledge of HTML5 for web page structure and design.
- **Programming Tools:** PyCharm, Visual Studio Code, Eclipse, IntelliJ IDEA, Keil µVision 4.
- **Object-Oriented Programming (OOP):** Strong understanding of OOP principles and methodologies.
- **Data Structures and Algorithms (DSA):** Solid foundation in data structures and algorithms.

**Soft Skills:**

- Rapport Building, Focused, Teamwork, Communication, Problem-Solving.

## PROJECTS

**Blind Stick with Image Detection**

- Developed a **smart blind stick with ultrasonic sensors** to detect obstacles.
- Integrated **image recognition** for object identification with voice feedback.
- Built the system using Python and OpenCV for real-time object detection and distance estimation.
- **Tools & Technologies:** Python, OpenCV, TensorFlow, Raspberry Pi.

**Design and Implementation of Combinational Circuits using Cadence Virtuoso** **Link**

- Designed **Logic Gates (AND, OR, NAND, NOR, XOR, X-NOR, Inverter, Buffer)** using **90 nm & 45 nm technologies**.
- Created Half Adder, Full Adder, Half Subtractor, and Full Subtractor.
- Implemented **Multiplexers, Demultiplexers, Priority Encoders, and Decoders**.
- Executed both pre-layout and post-layout simulations to verify functionality.

- Performed AV extracted view analysis, with Assura DRC & LVS verification by correcting layouts to meet 90 nm foundry rules**.**

**Analog Circuits Design using cadence virtuoso** **Link**

- Developed analog component including **Common Source Amplifier, Differential Amplifier, and Current Mirror Amplifier** using **GPDK 90nm**.
- Performed DC, AC, and transient analysis for performance evaluation.
- Conducted post-layout simulations & AV extracted view analysis, ensuring compliance through DRC & LVS checks
- Designed **LM741 operational amplifier IC** and performed pre-layout simulations for inverting and non-inverting amplifier configurations using GPDK 90nm technology.

**Design of a 6T SRAM Cell using Cadence Virtuoso** **Link**

- Designed a 6T SRAM memory cell using 90 nm technology with optimized read/write operations.
- Analyzed **Static Noise Margin (SNM)** using the Butterfly Curve and evaluated access time and **power dissipation**.
- Validated layout through post-layout simulations and ensured foundry compliance using Assura DRC & LVS.

## EDUCATION

**Vellore Institute of Technology.** **Amaravati-AP, India**
B.Tech in **Electronics and Communication Engineering (Specialization: VLSI)** **June 2022 - June 2026**

## ACADEMIC COURSES

- **Digital Logic Design,**
- **Analog Devices and Circuits**
- **Semiconductor Device Physics,**
- **Digital System Design for ASICs and FPGAs,**
- **Microprocessor and Microcontroller,**
- **System on Chip (SoC) Design,**
- **CMOS Digital VLSI Design.**
- **HDL Verification and Methodology**

## CERTIFICATIONS Links

- **Summer Intern at MANIT, Bhopal.**
- **VLSI International Workshop**
- **Programming in JAVA.**
- **Data Structures and Algorithms**
- **MATLAB Onramp.**
- **VLSI for Beginners.**
- **Space Science and Technology Awareness Training.**

## Achievements Link

- Successfully completed a **50-day hands-on challenge** focused on **combinational, sequential**, and **analog circuits**.
- Designed and simulated key circuits such as **logic gates**, **flip-flops**, **counters**, **amplifiers**, and a **6T SRAM**.
- Gained expertise in **schematic creation**, **layout design**, and **simulation** using **GPDK 90nm technology**.