SOURABH TYAGI

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Portfolio| GitHub | LinkedIn

EDUCATION

- B. Tech (4th Semester) in ECE spl. in VLSI | VIT AP University   CGPA: 8.5
- Class XII (MP Board) | Bright Career Academy, Ambah.
- Class X (MP Board) | Bright Career Academy, Ambah.

EXPERIENCE

❖ **Treasure, IEEE MTT**
- VIT-AP University | Sep 2023 – Present.
- Providing leadership and vision.
- Developing and implementing strategic plans.

❖ **Student Coordinator of VTAPP**
- VIT-AP University | 22 Mar 2024-23 Mar 2024
- Conducted Event in the tech Fest such as "JUMAN JI: Survivor of fittest", "Megatron", "COSMOX."

SKILLS

- Cadence Virtuoso
- Digital Electronics
- Physical Design
- Verilog for VLSI
- System Verilog for VLSI
- Object-Oriented Programming (OOP)
- Data Structures and Algorithms (DSA)
- Verification and Validation (VCV)
- Strong problem-solving an analytical skill

ACADEMIC PROJECTS

❖ **Major Project: AI Based Blind Stick with Image Detection**
- Developed a device that detects object distance and produces alarm sounds when nearing an object. It also speaks the object's name to the user.

❖ **Minor Projects:**
- Designed Inverter, OR, AND, NOR, XOR, X-NOR Gates, and Flipflop using 90nm Technology on **Cadence Virtuoso** tools.

ACADEMIC COURSE

- Completed Java with Data Structures and Algorithms (DSA) course.
- Acquired knowledge of Verilog for VLSI.
- Semiconductor device and circuits.
- Microprocessor and Microcontroller.
- NPTEL Swayam Courses in Physical Design (RTL to GDS) and Static timing analysis.

CERTIFICATIONS

- Overview of Space Science and Technology
- MATLAB Onramp
- Java Certification

HOBBIES

- ❖ Exploring things and Listen Music.
- ❖ Watching Cricket.