SoC Implementation of a Modulation Classification module for Cognitive Radios

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***Abstract*—The Cognitive radios are intelligent Software Defined radios which is aware of its environment by scanning and identifying spectrum holes. The knowledge of the modulation scheme of the received signal is significant to judge the channel and configure the SDR to transmit and receive. The two broad fields of modulation recognition are pattern recognition and decision theoretic approaches. This paper discusses Zynq implementation of an adaptive modulation recognition system which includes decision theoretic approach and higher order cumulants. Zynq is a SoC with Artix-7 FPGA and dual Core ARM Processor. The highly complex computations like FFT, higher order cumulants computations are implemented in FPGA and neural network algorithms are implemented in the ARM processor. The SNR based higher order cumulants computation will differentiate 16-qam, 32-qam, 64-qam, bpsk, qpsk and 8psk signals. The standard deviation computation of the zero centered instantaneous phase, amplitude and frequency are used to identify the MASK and MFSK signals. The FM signals are identified by the computation of the spectral power density.**

Keywords-Zynq, FPGA, RTL, Cumulants, FFT, Cognitive Radio, SDR.

I. INTRODUCTION

Electromagnetic Spectrum is one of the most scarce and precious natural resource. The usage and allocation of the spectrum is controlled by government agencies. The degree of spectral usage in a particular geographical location varies based on the band and number of users [1]. The knowledge of the received signal properties is useful for proper cognition and SDR configuration, particularly the modulation scheme and symbol rate. Detection of the modulation with minimum false alarm rate is a challenging task. The advanced developments in the communication technology makes the modulation detection more complex. The modulation classification processes mainly involves a feature extraction (FE) module and a classifier module FPGAs are best choice for the implementation of these highly complex algorithms in a time critical system. The work involves the FPGA implementation of combined modulation detection algorithms for feature extraction (FE) for FM, AM and phase modulated signals. The neural network based classifier module is implemented in the ARM Processor. The feature extraction techniques can be categorized based on instantaneous amplitude, phase and frequency, spectral correlation and higher order cumulants. The algorithms are implemented as separate modules in FPGA and finally a decision is made in the ARM processor. The feature parameters are spectral power density of the zero-center normalized instantaneous amplitude for detecting a FM signal, standard deviation of the absolute value of instantaneous amplitude for ASK signal identification and standard deviation of the instantaneous phase for MPSK signals [2] [3]. The Higher order cumulants are used to identify the digitally modulated signals. The fourth, sixth and eighth order cumulants with the measured SNR is used to detect BPSK, QPSK, 8PSK and QAM signals [4]. Figure 1 shows the basic block diagram of the module implemented in the Zynq chip. The IF signal is received by a 16-bit ADC and the sampled data in fed to the FPGA part of the Zynq chip and result is fed to the SDR for configuration.

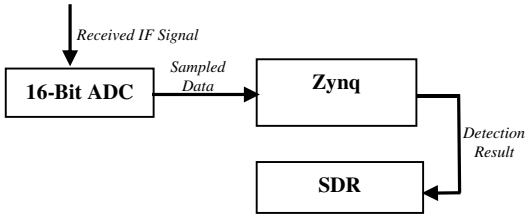

Fig 1: *Block Diagram*

II. SYSTEM ARCHITECTURE AND MODEL

Figure 2 shows the Block Diagram of the entire system. The cognition system is distributed into the Programmable Region (PL) and to the Processing System (PS).

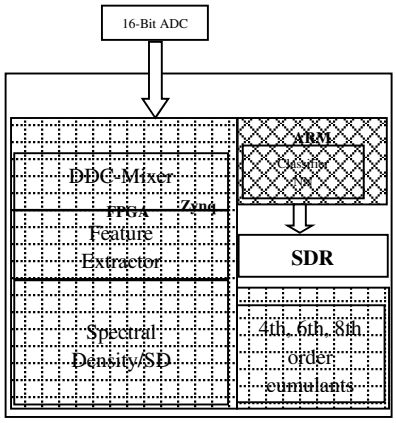

Fig 2: *System Architecture*

PL region is the FPGA and the PS region is the ARM Core. The PL region involves a Digital Down-converter (DDC), a mixer and the feature extraction modules. The PS region includes the classifier modules. The DDC module will receive data from the ADC at a sampling rate of 92.16MHz and at an IF of

22.16MHz.The received signal will be baseband converted and fed to the FE modules. The FE model consists of SPIA model, SDIA model, SDIP model, SDIF model and HOCC models. The SPIA Model will compute the power spectral density of the normalized instantaneous amplitude which is given by the equation

$$\alpha_{max} = \max\left[\frac{|fft\{x_{mn}(i)\}|^2}{Ns}\right] \quad (1)$$

$$x_{mn}(i) = x_n(i) - 1 \quad (2)$$

Where $x_{mn}(i)$ represents the zero-center normalized instantaneous amplitude and Ns represents signal sampling points.

$$x_n = \frac{x_i}{p_a} \quad (3)$$

p_a Indicates the averaged instantaneous amplitude which expressed by the following equation

$$p_a = \frac{1}{N_s}\sum_{i=1}^{N_s} x(i) \quad (4)$$

The α_{max} signal is used to identify the frequency modulated signal because the for FM signals the instantaneous amplitude is always constant and so the spectral density will be zero. The signal envelope of FSK signal is constant so α_{max} can be used to detect the FSK signal also. The instantaneous amplitude of the normalized FM and FSK signals centered to zero is always zero. The SDIA model will compute absolute value of the instantaneous amplitude and then the standard deviation of the will be computed.

$$s_m = \sqrt{\frac{1}{N_s}\left[\sum_{i=1}^{N^s} x_{mn}^2(i)\right] - \left[\sum_{i=1}^{N^s} x_{mn}^2(i)\right]^2} \quad (5)$$

s_m is used to identify between the 4ASK and 2ASK signals as for 2ASK signals the absolute value of the amplitude is constant and so s_{max} is zero, but for 4ASK signals s_m is not zero. The SDIP module will compute the standard deviation of the instantaneous phase.

$$s_{ap} = \sqrt{\frac{1}{C}\left[\sum_{a_n(i>a_i)} \phi_{nl}^2(i)\right] - \left[\frac{1}{C}\sum_{a_n(i>a_i)} |\phi_{nl}(i)|\right]^2} \quad (6)$$

$$s_{dp} = \sqrt{\frac{1}{C}\left[\sum_{a_n(i>a_i)} \phi_{nl}^2(i)\right] - \left[\frac{1}{C}\sum_{a_n(i>a_i)} \phi_{nl}(i)\right]^2} \quad (7)$$

s_{ap} for USB signal, LSB signal and AM signal is zero because it does contain the absolute value of the phase information. s_{ap} is mainly used to identify between MPSK and MASK signals. Similarly s_{dp} is to identify between the AM and ASK signals.

$$s_{af} = \sqrt{\frac{1}{C}\left[\sum_{a_n(i>a_i)} f_N^2(i)\right] - \left[\frac{1}{C}\sum_{a_n(i>a_i)} f_N(i)\right]^2} \quad (8)$$

s_{af} is the standard deviation of the normalized instantaneous frequency centered at zero. The standard deviation for 2FSK signal is zero and not zero for 4FSK signal so this parameter can be used to differentiate between a 2FSK and 4FSK signal. The results of these modules are fed to the classifier module implemented in the ARM processor.

The Identification of the digitally modulated signals are conducted using the higher order cumulants. The fourth, sixth, and eighth order cumulants are computed to identify between the BPSK, QPSK, 8PSK and QAM signals. Following equations are used to compute the cumulants [5],

$$Z_{63} = \frac{1}{N}\sum_{n=1}^{N} y_n^3\, y_n^{*3} - 9Z_{42}Z_{21} - 6Z_{21}^3 \quad (9)$$

$$Z_{42} = \frac{1}{N}\sum_{n=1}^{N} |y_n|^4 - |Z_{20}|^2 - 2Z_{21}^2 \quad (10)$$

$$Z_{21} = \frac{1}{N}\sum_{n=1}^{N} |y_n|^2 \quad (11)$$

$$Z_{20} = \frac{1}{N}\sum_{n=1}^{N} y_n^2 \quad (12)$$

$$Z_{40} = \frac{1}{N}\sum_{n=1}^{N} y_n^4 - 6Z_{20}^2 \quad (13)$$

$$\mu_{40} = \frac{1}{N}\sum_{n=1}^{N} y_n^4 \quad (14)$$

$$\mu_{80} = \frac{1}{N}\sum_{n=1}^{N} y_n^8 \quad (15)$$

$$Z_{80} = \mu_{80} - 35\mu_{40}^2 - 630Z_{40}^4 + 420Z_{20}^2 \quad (16)$$

Z_{63} Computed using equation 9 is used to differentiate between the PSK signals and QAM signals. The Z_{63} value is compared with the specific threshold and based on the results the signal is grouped under either PSK or QAM.

$$P_8 = \frac{Z_{80}}{Z_{40}^2} \quad (17)$$

P_8 Computed using equation 7 is used to distinguish between 8PSK and QPSK signals. Differentiating between the QAM signals is not discussed in this Paper. SNR of the received signals are also computed for proper grouping given by the equation [6]

$$snr = \frac{P_s}{P_n} \quad (18)$$

A neural network with decision theory is used for classification. The NNs have self-learning and self-adaptability, so the decision threshold is automatically calculated with self-learning capability. The basic Back propagation algorithm is used with the number of feature parameters decide the number of input nodes and the modulation schemes addressed decides the number of output nodes. In this model there are five input nodes and eight output nodes.

III. SIMULINK MODELS

The Fixed point Simulink models of all the equations are designed using Matlab fixed point tool box. Data types and tools are available with fixed point tool-box for developing fixed point algorithms. The implementation of these algorithms require more number of multipliers and adders so controlling the bit growth is a challenging task. The Fixed point tool box provide options for better precision, overflow and range controlling [7].

Figure 3 shows the fixed point Simulink model for the computation of power spectral density of the instantaneous amplitude of the received signal. The Key block is a 1024-point FFT computing module with output bit width of 32-bit.

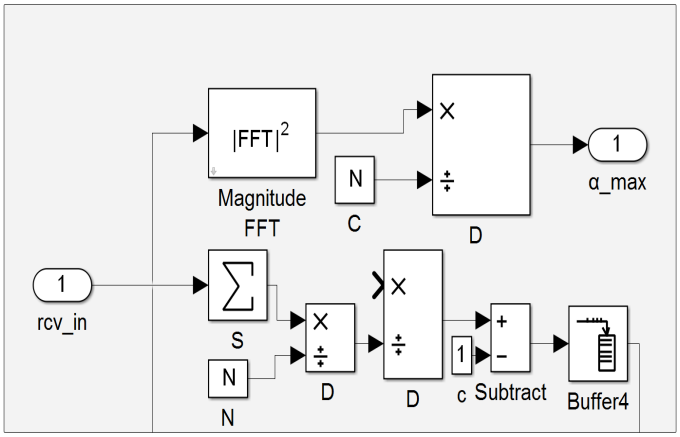

Fig 3: *Simulink model for equation 1*

The Simulink model for equation five is shown in figure 4 which will compute the standard deviation of the instantaneous amplitude. The received input data is 16-bit wide and same bit width is maintained for the output also. Computation of absolute value and accumulation is the critical operations as these operations will lead more bit growth.

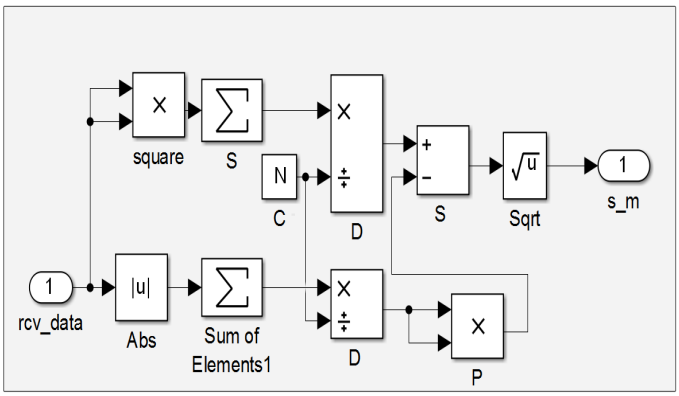

Fig 4: *Simulink model for equation 5*

The standard deviation of the instantaneous phase and absolute value of the instantaneous phase of the received signal is computed using the Simulink models shown in the figures 6 and 5 respectively. A complex to angle converter block is used to generate the phase value of the received signal which will accept a complex signal in double or single format. The output of all the blocks are maintained to maximum bit width of 24.All these blocks will support the advanced quantization operations and overflow detection.

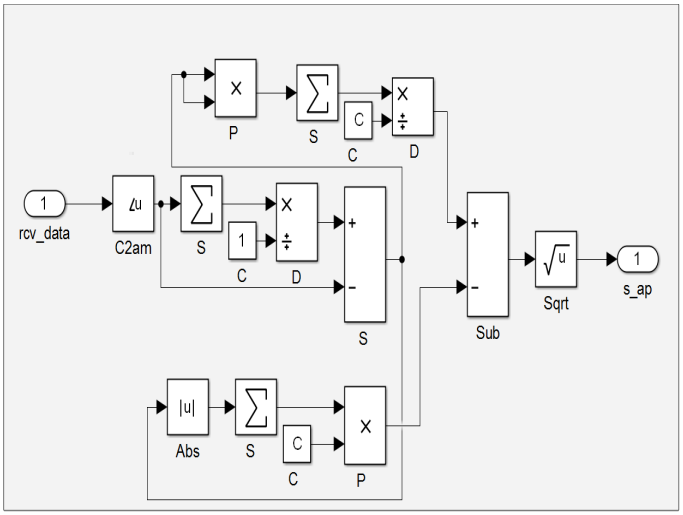

Fig 5: *Simulink model for equation 6*

The Higher order cumulants are computed using the Simulink models shown in the figures 7 and 8.The blocks mainly involves multiplication and summation.

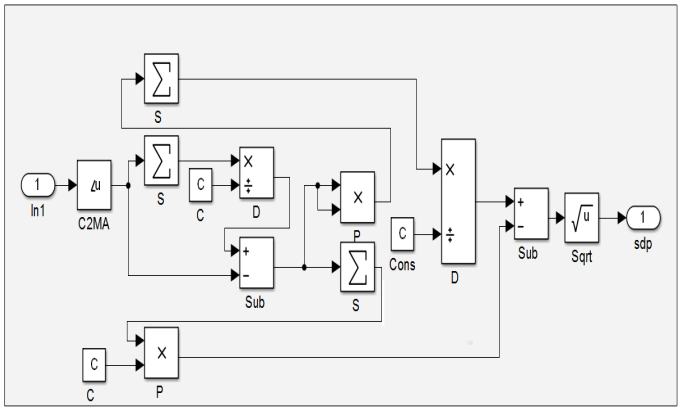

Fig 6: *Simulink model for equation 7*

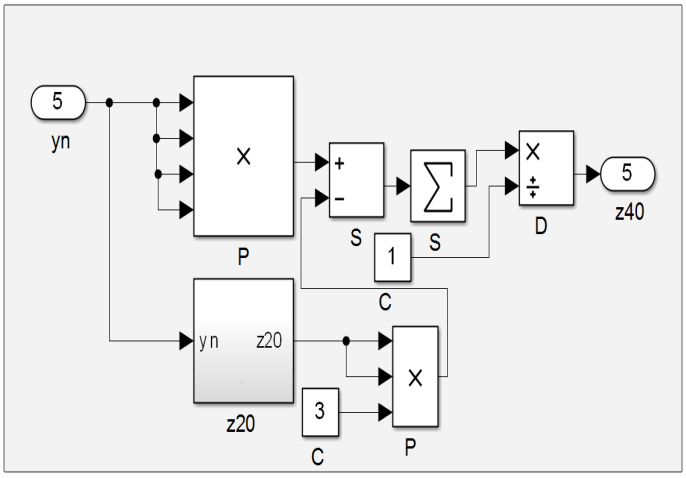

Fig 7: *Simulink model for 4th order Cumulants*

Majority blocks are selected from the HDL Coder libraries so that VHDL or Verilog Code scan be generated for implementation.

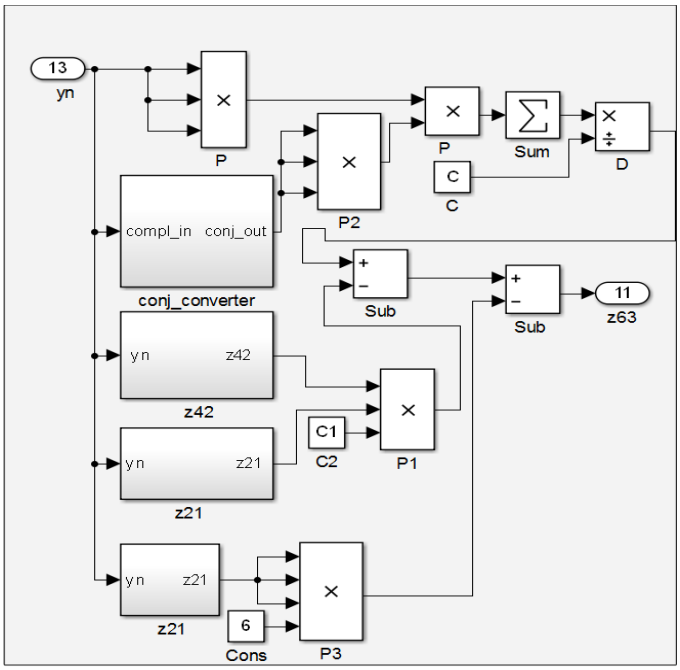

Fig 8: *Simulink model for 6th order Cumulants*

The subsystems used to generate the lower order cumulants are also shown in the figures.

IV. System Generator Models

The entire system is implemented in a custom designed Zynq board with a 16-ADC card. The major tools used for design are Xilinx system generator, SDK and Vivado

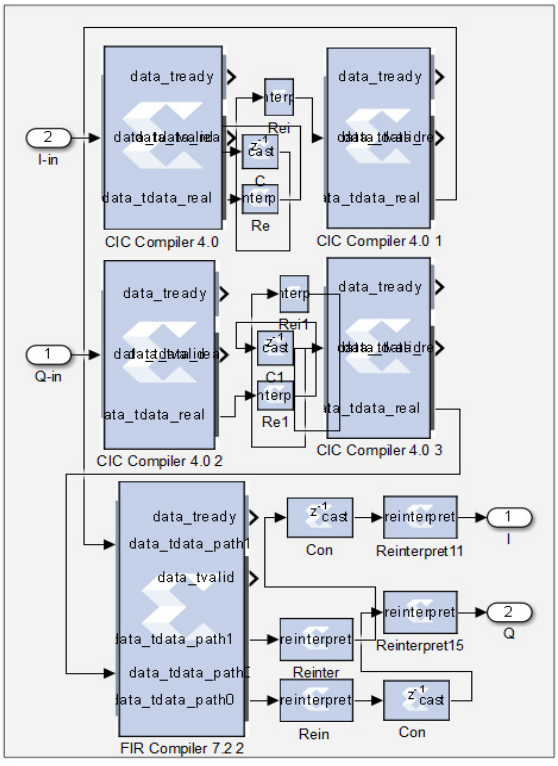

Fig 9: *Digital down Converter*

The standard deviation computation, power spectral computation and the HOC computation are designed with the IP cores provided by the Xilinx which includes FFT module, Square root calculator, Divider generator and phase generator.

The system starts with a Digital Down converter (DDC).Figure 9 shows the system generator model of the DDC block. The DDC converts the IF data to baseband. The DDC is designed with CIC filters and FIR Compilers. CIC filter is Cascaded integrator comb filter which is used when the down sampling rate is large [9], [10].The architecture of the CIC filter multiplier independent and it highly efficient in implementing DDC and DUC with high sampling rate changes [11].
The down converted data is fed to the HOC computing module, PSD and SD computing modules. For the power spectral computation of the instantaneous aptitude Xilinx FFT IP core is used. The XILINX FFT IP uses the cooley-Tukey FFT algorithm for implementation or DFT computation and the block provided a high speed AXI4 interface [12]. The input data is given complex data of N-samples represented as two 32 bit floating point numbers. Another critical task is the division operation and square root operation.

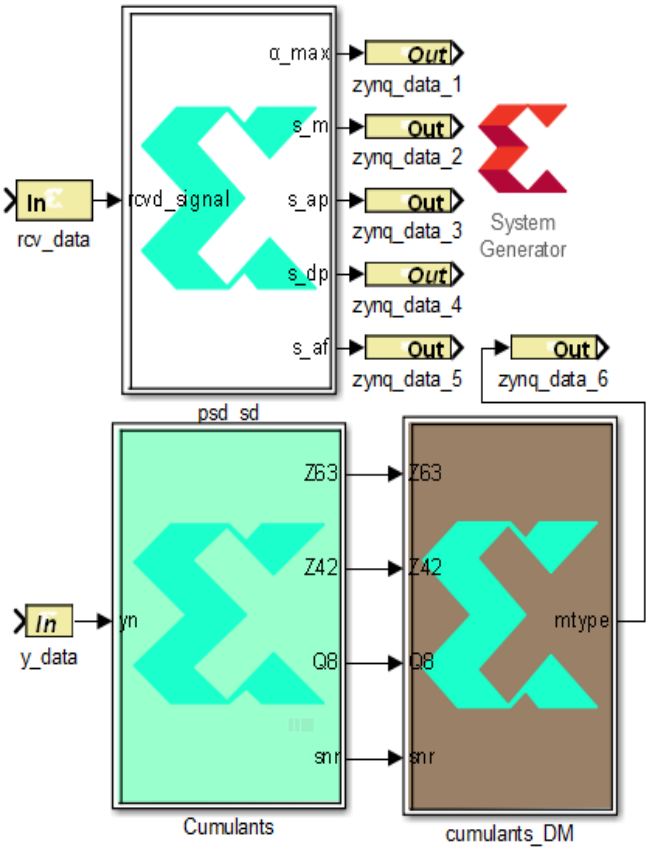

Fig 10:Feature Extraction module

The square root operation and the angle computation is performed using the Cordic algorithm. Figure 10 shows the system generator model of the Feature extractor. The design is grouped into three subsystems. Finally the output of each subsystem is transferred to the Zynq module. The back propagation neural network is implemented in the Zynq-ARM Processor.

V. HARDWARE IMPLEMENTATION AND TEST RESULTS

FPGA implementation of the feature extractor implemented using the Xilinx Vivado and EDK, and the feature classifier is implemented in the ARM using SDK. The maximum operating frequency of the FPGA in 92.16MHz with average resource utilization of 50%.

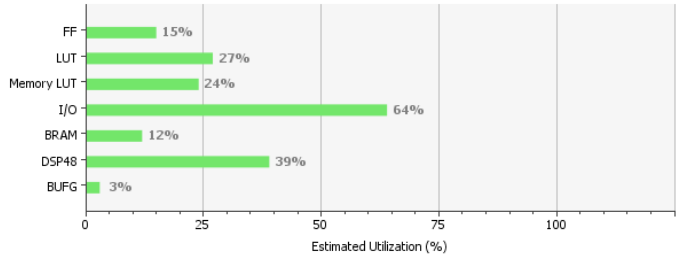

Fig 10:Resouce utilization

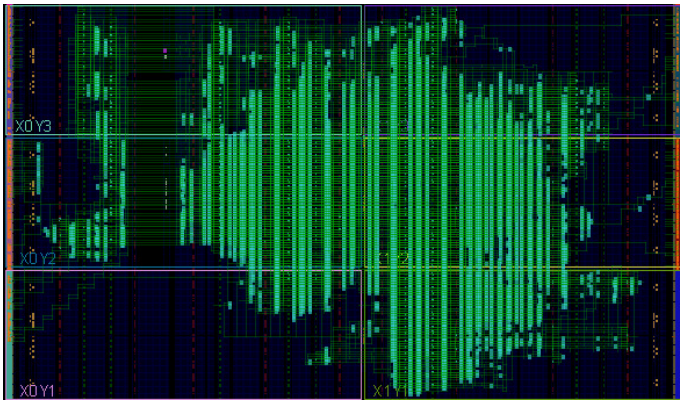

Fig 11:On-Chip View

Figure 10 and 11 shows the resource utilization and on chip view of the implemented system in ARTIX 7 FPGA.

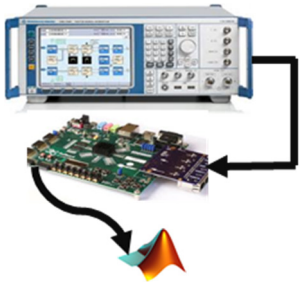

Fig 12:Test set-up

Figure 12 shows the test setup for the system which mainly include an R&S vector signal generator and the Zynq based board. Signals with different modulation schemes and noise level are generated using the R & S generator and the output is analyzed using MATLAB by hardware in the loop simulation. Figure 13 shows the Matlab generated plots SNR vs feature parameters for various modulations. The figures shows that when the SNR is too low it is difficult to differentiate between the modulations. For example in Figure 12 when the SNR is below 0 DB it is difficult to differentiate between the QPSK and BPSK signals. Similarly in figure 14 it is difficult to identify between the 2ASK and 4ASK Signals.

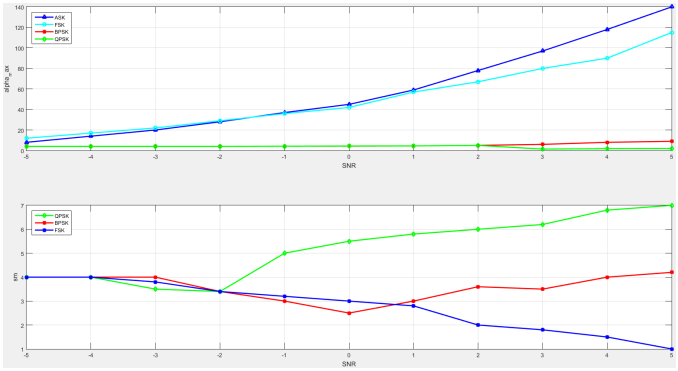

Fig 12: α_{max} and s_m for various modulations

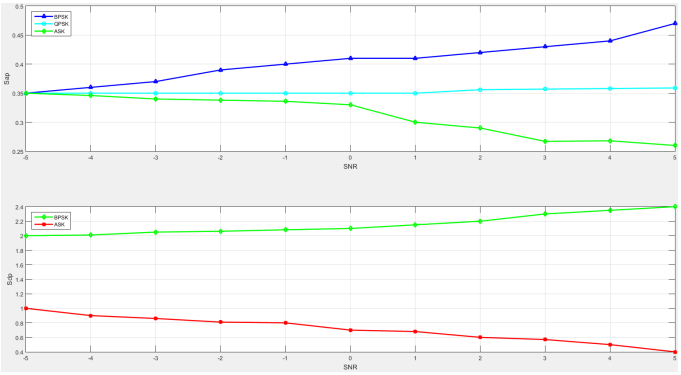

Fig 13: s_{ap} and s_{dp} for various modulations

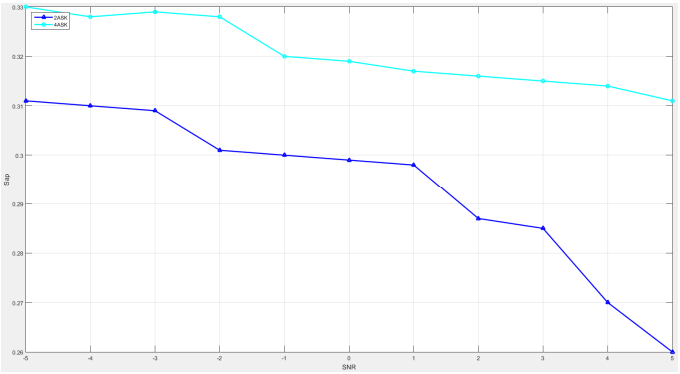

Fig 14: s_{af} of various modulations

Table 1 shows the detection rate for varrious modulaion schemes at a SNR of 0 dB.

Modulation	Detection %
BPSK	98
QPSK	94
FSK	95
ASK	90
QAM	85

TABLE I. Detection rate

CONCLUSION

The paper focused on the FPGA-ARM implementation of a combined modulation detection algorithm. The work involves the identification of various phase modulated, amplitude modulated and frequency modulated signals at various SNR values. The combined use of neural network and decision theory resulted in better recognition of the modulation schemes. The FPGA implementation using pipelined FFT and FIR Compilers helped to reduces the recognition time with minimum resources. The Digital down converters are designed using the CIC compilers to reduce the resource utilization including multipliers.

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