Design and Hardware Implementation of Reconfigurable Nano Satellite Communication System Using FPGA Based SDR for FM/FSK Demodulation and BPSK Modulation

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***Abstract*— Communication system is one of the major areas in which digital signal processing finds direct application. Recent advances in signal processing have helped in enormously reducing the complexity of communication system design and also in improving the performance of the system. Software Defined Radio (SDR) enables in-orbit re-configurability of frequency, modulation scheme, data rate, bandwidth and channel coding in the case of satellite communication systems where component change is not possible after launch. This paper describes the design and hardware implementation of SDR type communication system based on FPGA for a nano satellite. The major functions carried out onboard are FM/FSK demodulation for tele command uplink and BPSK modulation with raised cosine filtering for telemetry downlink. The full system is designed and implemented based on Microsemi Smartfusion2 FPGA. For hardware evaluation of the system, Virtex-6 FPGA with high speed analog daughter card is employed. Test results are also provided at the end of the paper along with implementation of re-configurability.**

***IndexTerms*—FM, FSK, BPSK, raised cosine filter, under sampling, quadrature sampling, FPGA, digital receiver, SDR, NCO, digital filter, FIR filter, satellite, nano satellite, communication**

I. INTRODUCTION

Universities worldwide are keen in setting-up Nano-satellite projects in order to enable students to expose on satellite technology. In order to achieve the scientific goals of the mission, a robust and agile communications system is necessary. The major functions carried out by communication subsystem are tele command uplink and telemetry downlink.

The whole communication system consists of an uplink receiver, a downlink transmitter and the corresponding antennae. The proposed uplink frequency is 435.06 MHz and the downlink frequency is 145.95 MHz. The receiver chain amplifies the signal and down converts it to intermediate frequency (IF). It also performs FM and FSK demodulation where the two FSK tones are 1.2 kHz and 2.2 kHz at a baud rate of 1.2 kbps, FM modulated with a deviation of 3.5 kHz. The transmitter chain performs multiplexing of the data coming from different channels for a total data rate of 9.6 kbps, raised cosine filtering, BPSK modulation, up conversion to VHF frequency and amplification to the required power levels.

II. SOFTWARE DEFINED RADIO

Software Defined Radio (SDR) includes software based structures instead of physical circuits to make some radio system operations such as filtering, mixing and etc. In an embedded project, it is possible to change software parts or critical parameters easily; therefore, SDR has a flexible structure and it is available for remote control, error fixing and expanding. These features are very useful and beneficial for space systems. There is no chance to modify a physical circuit to change frequency, filter order or modulation type in the space; however, you can modify a code to obtain these features.

III. DIGITAL RECEIVER ARCHITECTURE SELECTION

The demand for flexible radios is increasing day-by-day. Recent improvements in analog-to-digital converter technology have led to the development of software defined radios with digital receivers. In a software defined radio receiver, wideband analog-to-digital conversion that captures software defined radio node is performed closer to the antenna. In addition to the improved flexibility of use with

multiple standards over multiple frequency bands, digital receivers offer potential savings in power consumption, circuit area and cost, and can potentially realize performance improvements resulting from the use of digital filters.

The definition of a digital or software defined radio receiver is general and encompasses numerous architectures with various types of analog front ends. These architectures include direct RF sampling, RF sub-sampling, IF sampling, and IF sub-sampling.

IV. UNDER SAMPLING

In signal processing, under sampling is a technique where one samples a band pass-filtered signal at a sample rate below its Nyquist rate (twice the upper cut-off frequency), but is still able to reconstruct the signal. When one under samples a band pass signal, the samples are indistinguishable from the samples of a low-frequency alias of the high-frequency signal. Such sampling is also known as band pass sampling, harmonic sampling, IF sampling, and direct IF-to-digital conversion. A popular application of under sampling is in digital receivers [1].

V. QUADRATURE SAMPLING AND QUADRATURE DEMODULATION

Quadrature demodulation is one of the basic forms of digital demodulation which can eliminate the problem of spectral overlap which may occur in normal real down conversion. The principle is based on Hilbert Transform and Pre-envelope. The complex baseband envelope of a real signal can be extracted by just multiplying the signal by sine and cosine waveforms of the center frequency and low pass filtering [2].

Quadrature sampling is a technique where one samples a signal at 4 times its frequency, so that the multiplications by sines and cosines required for its conversion to complex baseband signal can be simplified to be just multiplications by 0,1,0,-1 and 1,0,-1,0 patterns respectively which can be easily implemented in hardware [3].

VI. FM DEMODULATION ALGORITHMS

Frequency Modulation (FM) is one of the widely used analog modulation schemes. Different algorithms are available for implementing FM demodulation in the digital domain [4].

Arc tan algorithm is one of the most famous algorithms for FM demodulation. But due to the requirement of very large memory space for the implementation of Look Up Table (LUT), differentiated arc tan algorithm is preferred in practice for satellite applications [5].

VII. FSK DEMODULATION ALGORITHMS

Frequency Shift Keying (FSK) is widely used in satellite and launch vehicle tele command. There are several algorithms available for the demodulation of FSK signal [6]. Cross-Differentiate-Multiplier (CDM) type of demodulator [7] is implemented in the present design.

VIII. BPSK MODULATION WITH RAISED COSINE FILTERING

Binary Phase Shift Keying (BPSK) is the basic and simplest digital modulation scheme which is used in satellite telemetry, especially deep space telemetry. The principle of BPSK modulation is to shift the carrier phase by 0º or 180º depending on whether the data bit is a 0 or 1. The analog method of implementing BPSK modulation is using a double balanced mixer. In an FPGA, the same can be simply implemented by inverting the output of an NCO (Numerically Controlled Oscillator) when the input bit is a 1 and not when it is a 0.

A raised cosine filter [8] is a low-pass filter which is commonly used for pulse shaping in communication systems. The frequency response of a perfect raised cosine filter is symmetric with respect to 0 Hz, and is divided into three parts: it is flat (constant) in the pass-band; it sinks in a graceful cosine curve to zero through the transition region; and it is zero outside the pass-band. The behavior of a real filter is an approximation to this response.

IX. SYSTEM DESIGN

The design process of any communication system starts with the link budget analysis [9] which will suggest the amount of power to be transmitted by the transmitter and the sensitivity of the receiver to be designed. Based on detailed analysis, the modulation scheme for telemetry transmitter was selected as BPSK (Binary Phase Shift Keying). The transmitted power should be +23 dBm minimum. The sensitivity of the tele command receiver should be -105 dBm minimum.

The block diagram of the complete communication system is shown in Fig. 1.

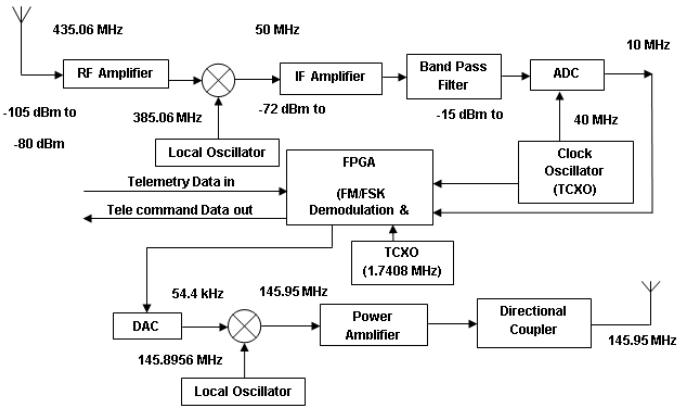

Fig 1. Simplified block diagram of FPGA based communication system

The incoming signal from the antenna is first amplified and down-converted to an IF of 50 MHz. The output of the IF amplifier is under sampled by a high speed ADC at a sampling speed of 40 MHz. The output of ADC will be 10 MHz (50 MHz -40 MHz). The most critical task in the implementation of a digital receiver is the selection of the ADC (Analog to Digital Converter) [10]. After detailed studies, AD9266 (16

Bit, 65 MSPS) ADC from Analog Devices was selected. One of the major factors which decide the dynamic range of a digital receiver is the clock jitter [11]. In order to get excellent jitter performance, a Temperature Compensated Crystal Oscillator (TCXO) is used as the sampling clock for the ADC, which will provide clock for the FPGA also. FSK demodulation will consider the input to be an FM signal with center frequency of 1.7 kHz ((1.2+2.2)/2). It generates sine and cosine at this frequency by an NCO which is clocked with a 1.7408 MHz TCXO (1.7 kHz = 1.7408 MHz/1024). The tele command data, after FM and FSK demodulation, is sent to the On Board Computer (OBC) in the satellite for required action.

The telemetry data from payloads will be interfaced with the FPGA for AX.25 framing, raised cosine filtering and further BPSK modulation on a 54.4 kHz carrier generated by the NCO with 1.7408 MHz clock (54.4 kHz = 1.7408 MHz/32). The modulated data will be given to a DAC (Digital to Analog Converter) for conversion to the analog form. This will be further up converted to the required frequency (145.95 MHz) using a mixer (RMS-1 from Mini circuits) and local oscillator. Further the signal will be amplified to the required power levels and sent to the antenna for transmission to the ground station.

X. MATLAB SIMULATION RESULTS

A 10 MHz carrier (simulating the under sampled output of ADC) is generated in MATLAB which is modulated with 1.2 kHz and 2.2 kHz tones with 3.5 kHz deviation using FSK/FM. The modulated signal is fed to the demodulator section which first samples the signal at 40 MHz. Then quadrature down conversion is implemented by multiplications with 1, 0,-1, 0 and 0, 1, 0, -1 patterns for the I and Q arms respectively. Then the signals are filtered and passed to the demodulator block. The demodulator works on the differentiated arc tan algorithm. The simulation result of FM demodulator block is shown in Fig. 2.

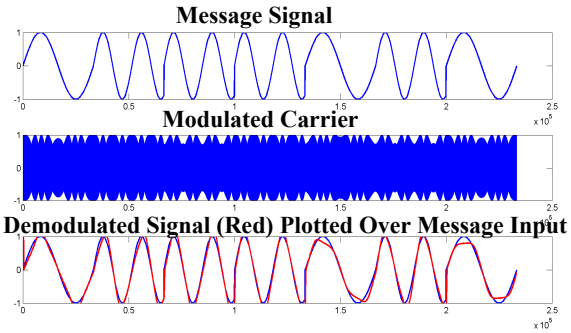

Fig 2. MATLAB Simulation Result of FM Demodulator

The output of FM demodulator is filtered and then fed to the FSK demodulation block which is again implemented based on the CDM algorithm. The simulation result of FSK demodulator block is shown in Fig. 3. The output of FSK demodulator is just a delayed version of the input, the delay being proportional to the processing time.

The transmitter base band section filters the data using raised cosine roll off filter and then performs BPSK modulation. The simulation results of 9600 baud data modulating a 54.4 kHz carrier after raised cosine roll-off filtering with a 64 tap filter is shown in Fig. 4.

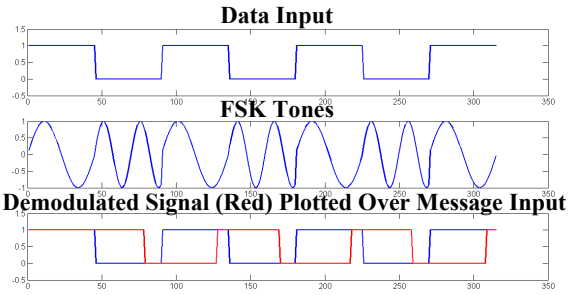

Fig 3. MATLAB Simulation Result of FSK Demodulator

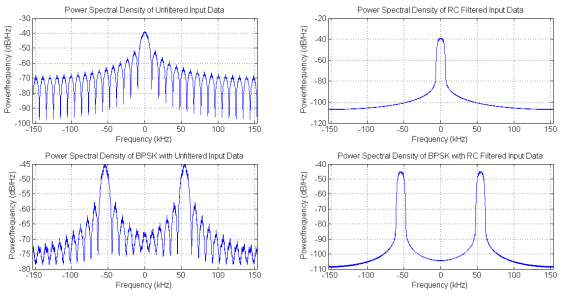

Fig 4. MATLAB Simulation Result of BPSK Modulator

XI. VHDL SIMULATION RESULTS

The design was validated in Micro semi Smart fusion 2 FPGA. Libero IDE tool was used for the VHDL coding of the system. Model Sim simulation tool was used for simulation of the complete system. The simulation results are shown in Figs.5, 6 and 7.

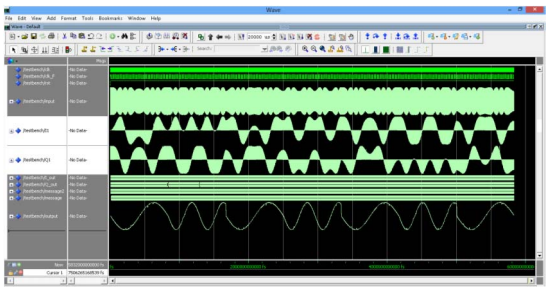

Fig 5. VHDL Simulation Result of FM demodulator block

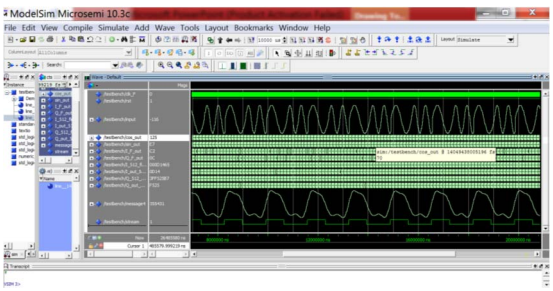

Fig. 6. VHDL Simulation Result of FSK demodulator block

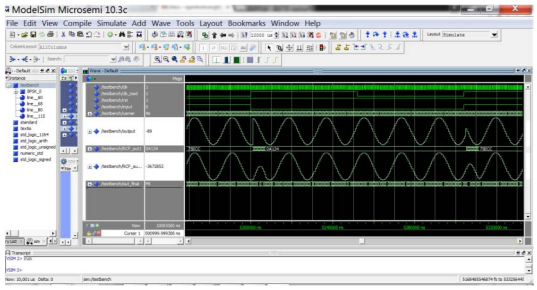

Fig. 7. VHDL Simulation Result of BPSK modulator without and with raised cosine filtering

XII. HARDWARE EVALUATION RESULTS

For hardware validation of the system, Virtex-6 FPGA with high speed analog [12] was selected. The interfacing of the two cards is shown in Fig. 8 and the complete test setup is shown in Fig. 9. The ML605 board enables hardware and software developers to create or evaluate designs targeting the Virtex-6 XC6VLX240T-1FFG1156 FPGA. The FMC150 is a four-channel, ADC/DAC FMC daughter card. The card provides two 14-bit A/D channels and two 16-bit D/A channels, which can be clocked by an internal clock source (optionally locked to an external reference) or an external sample clock.

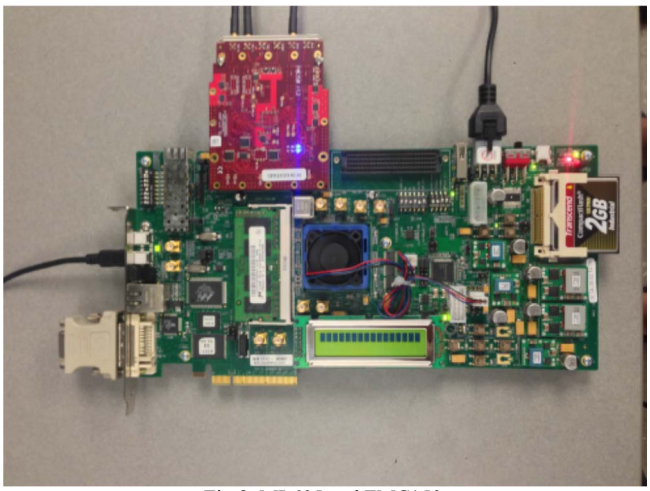

Fig 8. ML605 and FMC150

For evaluation of the performance of FM demodulator, the vector signal generator is internally modulated with pure tones of 1.2 kHz and 2.2 kHz frequencies at deviation of 3.5 kHz. The modulated output is fed to the ADC on-board FMC-150 card through BNC to MMCX coaxial cable. The data after digitization is processed by the FPGA. The final demodulated output will be given to the DAC and the output of which is verified on the oscilloscope. Since there is a high pass filter at 3.2 MHz at the output of DAC, in order to evaluate the performance of FM demodulator alone, all the frequencies of message signal were scaled up simultaneously so that the two tones are at 1 MHz and 2 MHz and the FM deviation is 3 MHz. Fig. 10 shows the oscilloscope waveforms of modulation input, modulated carrier and the demodulated output at the output of DAC.

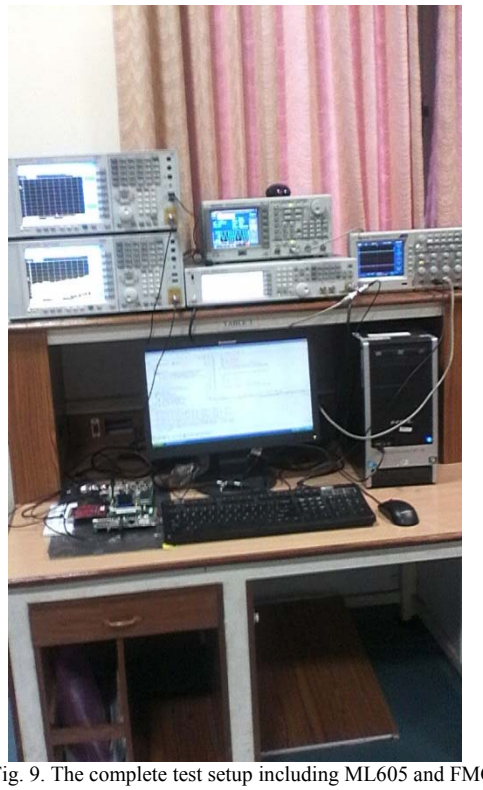

Fig. 9. The complete test setup including ML605 and FMC150

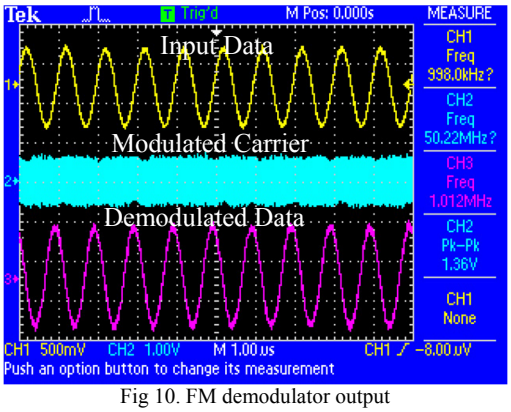

Fig 10. FM demodulator output

For evaluation of the cascaded performance of FM/FSK demodulator, waveform generator is internally FSK modulated with tones of frequencies 1.2 kHz and 2.2 kHz at baud rate of 1.2 kbps. The FSK modulated output is fed to the modulation input port of vector signal generator. The signal generator is FM modulated with the externally FSK modulated data at deviation of 3.5 kHz. The FSK/FM modulated carrier is fed to FMC-150 and after digitization to ML-605 board. Fig. 11 shows the power spectrum of FSK/FM modulated carrier and Fig. 12 shows the oscilloscope waveforms of FSK modulated tones input and the FM/FSK demodulated bit stream output.

For evaluation of the performance of BPSK modulator with raised cosine filtering, external data from waveform generator is fed to the FPGA through its GPIO port.

The data after raised cosine filtering will modulate the internally generated 54.4 kHz carrier and the output will be given to the oscilloscope and spectrum analyser after conversion to the analog form by the DAC onboard FMC-150 card. Again since the daughter card does not support low frequencies, a 1.5 MHz internally generated carrier is modulated with 300 kHz data for evaluation purpose. Fig. 13 shows the oscilloscope waveforms of input data and the BPSK modulated carrier with unfiltered data. Fig. 14 shows the power spectrum of BPSK modulated carrier with unfiltered data.

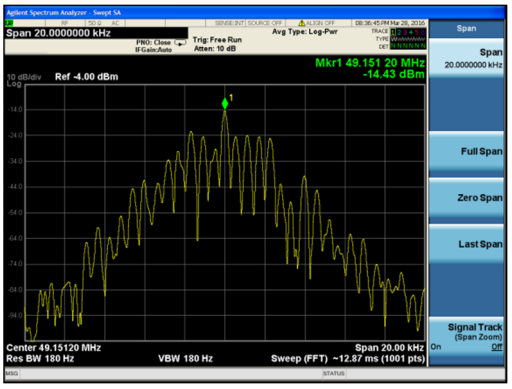

Fig 11. Power spectrum of FSK/FM modulated carrier

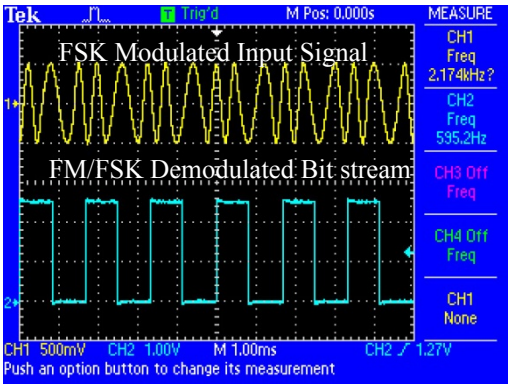

Fig 12. FM/FSK demodulator output

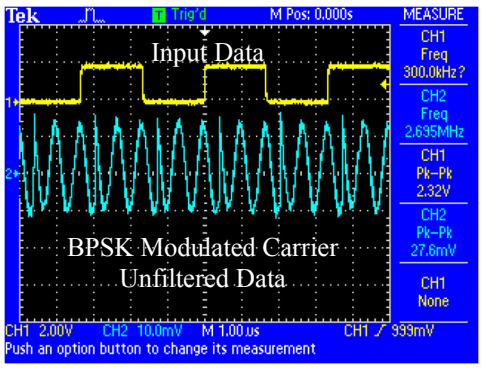

Fig 13. BPSK waveform with unfiltered data input

Fig. 15 shows the oscilloscope waveforms of input data and the BPSK modulated carrier with raised cosine filtered data. Fig. 16 shows the power spectrum of BPSK modulated carrier with raised cosine filtered data.

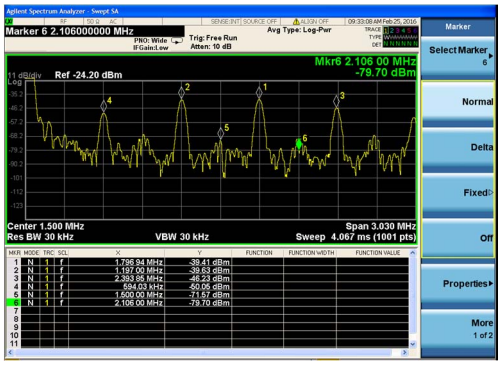

Fig 14. BPSK modulated spectrum with unfiltered data input

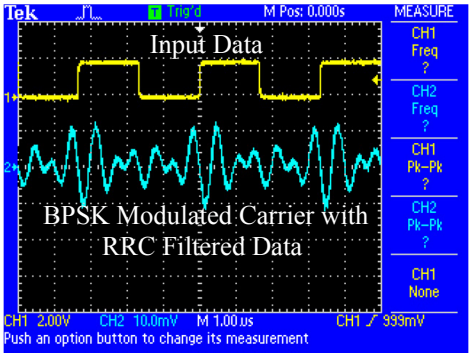

Fig 15. BPSK waveform with RRC filtered data input

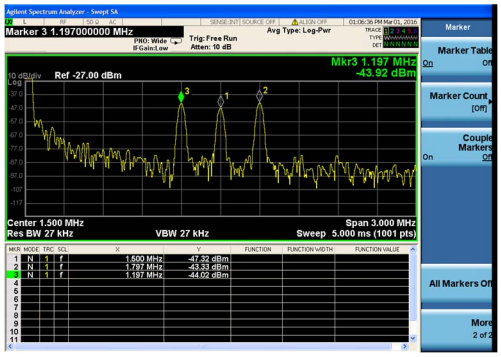

Fig 16. BPSK modulated spectrum with RRC filtered data input

XIII. IMPLEMENTATION OF RE-CONFIGURABILITY

Frequency, modulation scheme, data rate, bandwidth and power are the five major parameters which can be reconfigured in-orbit for satellite communication systems. Each of these can be reconfigured from the ground depending on the requirement and various other considerations like interference and link availability.

For example, if interference is observed in a particular downlink frequency, it can be switched to another frequency by just sending a command from the ground station and hence varying the tuning word for the downlink transmitter NCO. By providing a single control line, 2 frequencies can be set, 4 frequencies by 2 control lines and upto 2^n frequencies by n control lines. The feature has been implemented in the present design and has been evaluated for performance upto 16 spot frequencies.

Similarly downlink modulation scheme can be changed from BPSK to QPSK, GMSK or any other scheme as per the system requirement. This has been evaluated successfully for the simple case of change from BPSK to QPSK. Data rate can be adjusted depending upon link budget availability. Similarly power and bandwidth can be traded off depending on whether the system is power limited or band limited and various other considerations.

XIV. CONCLUSION

This paper described the design and implementation of an on-board communication system for a nano satellite with FPGA based SDR. All the design aspects were touched upon starting from link budget analysis to the hardware realization through MATLAB simulation and VHDL implementation. As an alternative for the validation of the hardware design, testing with Virtex-6 FPGA development kit along with high speed analog daughter card has been carried out and the test results are as per expectation. Various re-configurability options have also been implemented which is one of the important aspects of SDR based systems.

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