EE3300 : Analog Circuits
Mini Project 3

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1 Question 1

1.1 Problem Statement

1. Design a two-stage opamp (miller-compensated) in 65 nm CMOS process with the following specifications:

. • Supply voltage: 1.1 V.

. • Input common-mode voltage: 0.55 V.

. • Load capacitance: 10 pF.

. • Unity gain bandwidth: 10 MHz.

. • Phase-margin: 60 degrees.

. • DC gain $\geq$ 40 dB

. • Slew rate $\geq$ 10V/µs.

Objective is to minimize power consumption while satisfying the above specifications.
Design should include biasing circuitry.
Submit hand calculations used to find:

. • First and second stage transconductance.

. • Miller cap and/or zero-nulling resistor.

. • First and second stage bias-current.

Submit the netlist and the following frequency responses:

. • Bode plot.

. • Common-mode rejection ratio (CMRR).

. • Power-supply rejection ratio (PSRR).

1.2 Spice Netlist

Bodeplot

M1 N003 Vn N004 N004 NMOS l=L w=W1 ad='2*65n*W1' as='2*65n*W1' pd='2*(2*65n+W1)' ps='2*(2*65n+W1)' m=M
M2 N001 Vp N004 N004 NMOS l=L w=W2 ad='2*65n*W2' as='2*65n*W2' pd='2*(2*65n+W2)' ps='2*(2*65n+W2)' m=M
M3 VDD N003 N003 VDD PMOS l=L w=W3 ad='2*65n*W3' as='2*65n*W3' pd='2*(2*65n+W3)' ps='2*(2*65n+W3)' m=M
M4 VDD N003 N001 VDD PMOS l=L w=W4 ad='2*65n*W4' as='2*65n*W4' pd='2*(2*65n+W4)' ps='2*(2*65n+W4)' m=M
M5 N004 Vb VSS VSS NMOS l=L w=W5 ad='2*65n*W5' as='2*65n*W5' pd='2*(2*65n+W5)' ps='2*(2*65n+W5)' m=M
M6 VDD N001 Out VDD PMOS l=L w=W6 ad='2*65n*W6' as='2*65n*W6' pd='2*(2*65n+W6)' ps='2*(2*65n+W6)' m=M
M7 Out Vb VSS VSS NMOS l=L w=W7 ad='2*65n*W7' as='2*65n*W7' pd='2*(2*65n+W7)' ps='2*(2*65n+W7)' m=M
Cc N002 Out 2.3p
M9 Vb Vb VSS VSS NMOS l=L w=W9 ad='2*65n*W9' as='2*65n*W9' pd='2*(2*65n+W9)' ps='2*(2*65n+W9)' m=M
I1 VDD Vb 23µ
CL Out 0 10p
V1 VDD 0 1.1
V2 0 VSS 1.1
vcm N006 0 0.55
vin N005 0 0 AC 1
E1 Vp N006 N005 0 0.5
E2 Vn N006 N005 0 -0.5
M8 N001 VDD N002 N002 NMOS l=L w=W2 ad='2*65n*W2' as='2*65n*W2' pd='2*(2*65n+W2)' ps='2*(2*65n+W2)' m=M
.model NMOS NMOS
.model PMOS PMOS
.lib standard.mos
.param L=1u M=1 W1=1.6u W2=1.6u W3=35u W4=35u W5=2.14u W6=160u W7=4u W8=25u W9=2.14u
.include 65nm_NMOS_bulk.pm
.include 65nm_PMOS_bulk.pm
.ac dec 1000 1m 1G
.backanno
.end

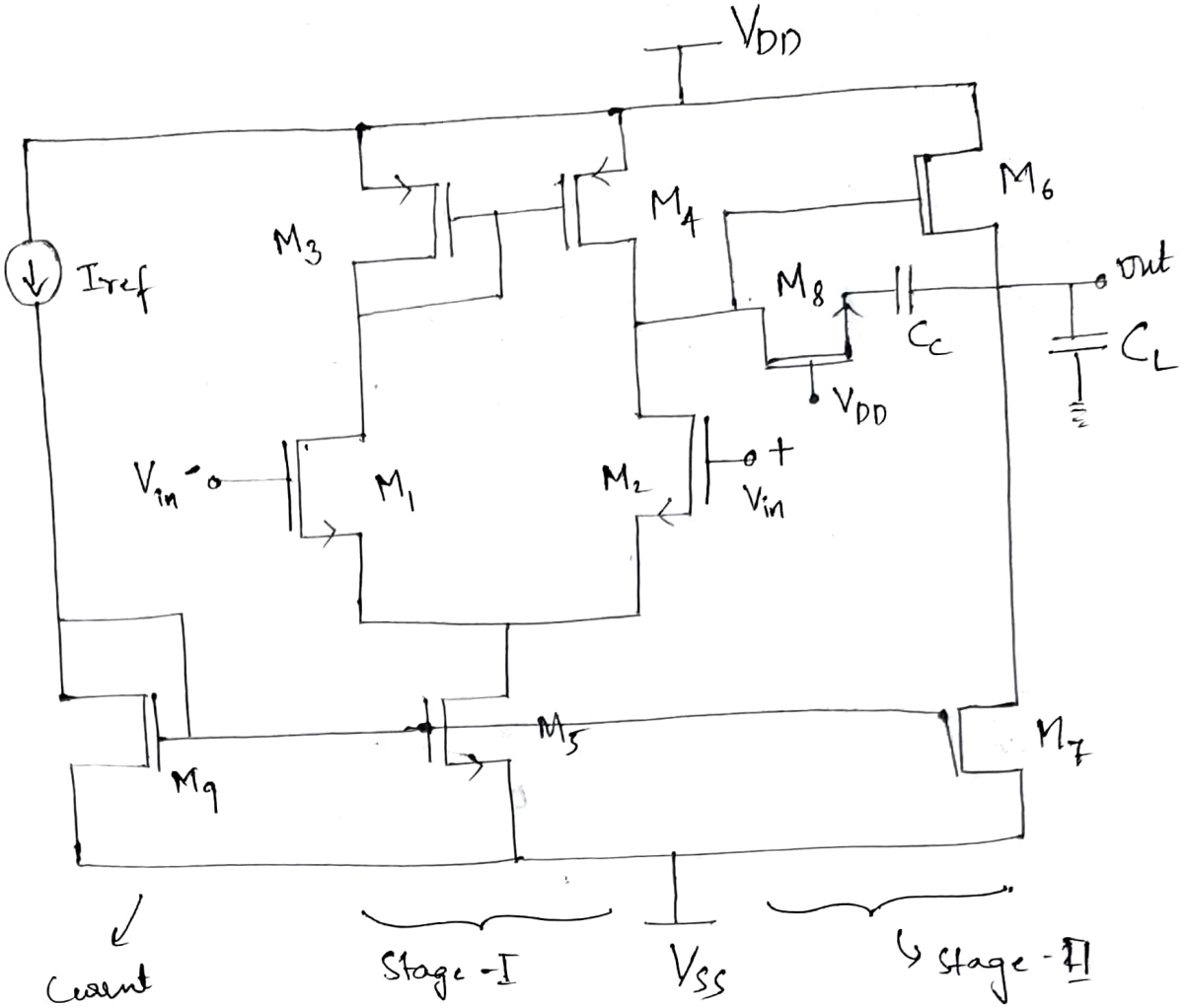
CMRR

```
XX1 VDD N001 N003 Out VSS twostageopamp
V1 VDD 0 1.1
V2 0 VSS 1.1
R1 Out N001 1Meg
R2 N001 N002 1Meg
R3 N003 N002 1Meg
R4 0 N003 1Meg
V3 N002 0 0.55 AC 1
C1 Out 0 10p

* block symbol definitions
.subckt twostageopamp VDD Vn Vp Out VSS
M1 N003 Vn N004 N004 NMOS l=L w=W1 ad='2*65n*W1' as='2*65n*W1' pd='2*(2*65n+W1)'
ps='2*(2*65n+W1)' m=M
M2 N001 Vp N004 N004 NMOS l=L w=W2 ad='2*65n*W2' as='2*65n*W2' pd='2*(2*65n+W2)'
ps='2*(2*65n+W2)' m=M
M3 VDD N003 N003 VDD PMOS l=L w=W3 ad='2*65n*W3' as='2*65n*W3' pd='2*(2*65n+W3)'
ps='2*(2*65n+W3)' m=M
M4 VDD N003 N001 VDD PMOS l=L w=W4 ad='2*65n*W4' as='2*65n*W4' pd='2*(2*65n+W4)'
ps='2*(2*65n+W4)' m=M
M5 N004 N005 VSS VSS NMOS l=L w=W5 ad='2*65n*W5' as='2*65n*W5' pd='2*(2*65n+W5)'
ps='2*(2*65n+W5)' m=M
M6 VDD N001 Out VDD PMOS l=L w=W6 ad='2*65n*W6' as='2*65n*W6' pd='2*(2*65n+W6)'
ps='2*(2*65n+W6)' m=M
M7 Out N005 VSS VSS NMOS l=L w=W7 ad='2*65n*W7' as='2*65n*W7' pd='2*(2*65n+W7)'
ps='2*(2*65n+W7)' m=M
Cc1 N002 Out 2.3p
M8 N005 N005 VSS VSS NMOS l=L w=W9 ad='2*65n*W9' as='2*65n*W9' pd='2*(2*65n+W9)'
ps='2*(2*65n+W9)' m=M
I1 VDD N005 23µ
M9 N001 VDD N002 N002 NMOS l=L w=W2 ad='2*65n*W2' as='2*65n*W2' pd='2*(2*65n+W2)'
ps='2*(2*65n+W2)' m=M
.param L=1u M=1 W1=1.6u W2=1.6u W3=35u W4=35u W5=2.14u W6=160u W7=4u
W8=25u W9=2.14u
.include 65nm_NMOS_bulk.pm
.include 65nm_PMOS_bulk.pm
.ends twostageopamp
.model NMOS NMOS
.model PMOS PMOS
.lib C:standard.mos
.ac dec 1000 1m 1G
.backanno
.end
```

PSRR

```
XX1 VDD Out N001 Out VSS twostageopamp
V1 VDD 0 1.1 AC 1
V2 0 VSS 1.1
V3 N001 0 0.55
C1 Out 0 10p

* block symbol definitions
.subckt twostageopamp VDD Vn Vp Out VSS
M1 N003 Vn N004 N004 NMOS l=L w=W1 ad='2*65n*W1' as='2*65n*W1' pd='2*(2*65n+W1)'
ps='2*(2*65n+W1)' m=M
M2 N001 Vp N004 N004 NMOS l=L w=W2 ad='2*65n*W2' as='2*65n*W2' pd='2*(2*65n+W2)'
ps='2*(2*65n+W2)' m=M
M3 VDD N003 N003 VDD PMOS l=L w=W3 ad='2*65n*W3' as='2*65n*W3' pd='2*(2*65n+W3)'
ps='2*(2*65n+W3)' m=M
M4 VDD N003 N001 VDD PMOS l=L w=W4 ad='2*65n*W4' as='2*65n*W4' pd='2*(2*65n+W4)'
ps='2*(2*65n+W4)' m=M
M5 N004 N005 VSS VSS NMOS l=L w=W5 ad='2*65n*W5' as='2*65n*W5' pd='2*(2*65n+W5)'
ps='2*(2*65n+W5)' m=M
M6 VDD N001 Out VDD PMOS l=L w=W6 ad='2*65n*W6' as='2*65n*W6' pd='2*(2*65n+W6)'
ps='2*(2*65n+W6)' m=M
M7 Out N005 VSS VSS NMOS l=L w=W7 ad='2*65n*W7' as='2*65n*W7' pd='2*(2*65n+W7)'
ps='2*(2*65n+W7)' m=M
Cc1 N002 Out 2.3p
M8 N005 N005 VSS VSS NMOS l=L w=W9 ad='2*65n*W9' as='2*65n*W9' pd='2*(2*65n+W9)'
ps='2*(2*65n+W9)' m=M
I1 VDD N005 23µ
M9 N001 VDD N002 N002 NMOS l=L w=W2 ad='2*65n*W2' as='2*65n*W2' pd='2*(2*65n+W2)'
ps='2*(2*65n+W2)' m=M
.param L=1u M=1 W1=1.6u W2=1.6u W3=35u W4=35u W5=2.14u W6=160u W7=4u
W8=25u W9=2.14u
.include 65nm_NMOS_bulk.pm
.include 65nm_PMOS_bulk.pm
.ends twostageopamp
.model NMOS NMOS
.model PMOS PMOS
.lib C:standard.mos
.ac dec 1000 1m 1G
.backanno
.end
```

Two stage - opamp (Miller Compensated)



Circuit diagram

$$A(s) = \frac{A_0\left(1 - \frac{s}{z}\right)}{\left(1 - \frac{s}{p_1}\right)\left(1 - \frac{s}{p_2}\right)}$$

$$z = \frac{g_{m6}}{C_c} \qquad p_1 = \frac{GB}{A_v(0)} \Rightarrow \text{Since } 20\log(A_v) = 20\log\left(\frac{GB}{p_1}\right)$$

$$p_2 \cong \frac{g_{m2}}{C_L}$$

$$PM = 180^\circ - \tan^{-1}\left(\frac{w}{|P_1|}\right) - \tan^{-1}\left(\frac{w}{|P_2|}\right) - \tan^{-1}\left(\frac{w}{|z|}\right) = 60^\circ$$

$w = GB$, $z > GB \Rightarrow z = 10GB$

$$\Rightarrow \quad 180^\circ - \tan^{-1}\left(A_V(0)\right) - \tan^{-1}\left(\frac{GB}{|P_2|}\right) - \tan^{-1}(0.1) = 60^\circ$$

$= 90^\circ$

$$\Rightarrow \quad |P_2| \geq 2.215\, GB$$

$$|z_1| \geq 10GB \Rightarrow \frac{g_{m6}}{C_c} \geq 10\,\frac{g_{m1}}{C_c}$$

$$\Rightarrow \quad g_{m6} \geq 10\, g_{m1}$$

$$|P_2| \geq 2.215\, GB$$

$$\Rightarrow \quad \frac{g_{m6}}{C_L} \geq \frac{g_{m1}}{C_c} \times 2.215$$

$$\Rightarrow \quad \boxed{C_c \geq 0.2215\, C_L}$$

$C_L = 10pF \Rightarrow C_c \geq 2.215pF$, $\boxed{C_c = 2.3pF}$

Given Slew rate $= \frac{I_5}{C_c} > 10V/\mu s$

$$\Rightarrow \quad I_5 \geq 2.3 \times 10^{-12} \times 10 \times 10^{6}$$

$$\Rightarrow \quad I_{5min} = 23\,\mu A$$

Now we know $g_{m6} = 10 g_{m1}$

$$A_0 = \frac{2 g_{m1} g_{m6}}{P_5 P_6 (\lambda_2 + \lambda_4)(\lambda_6 + \lambda_7)}$$

From Mini-project-1

$K_n' = 569\mu$ (short)

$K_n' = 541\mu$ (long)

$K_p' = 184\mu$ (short)

$K_p' = 491\mu$ (long)

$\lambda_n = 0.87$

$\lambda_p = 1.14$

$$A_0 \geq 40dB \Rightarrow \frac{2 g_{m1} \times 10 g_{m1}}{23 \times 10^{-6} \times 4 \times \frac{g_{m6}^2}{2 K_p' \left(\frac{W}{L}\right)_6}} > 100$$

$$\Rightarrow \boxed{\left(\frac{W}{L}\right)_6 > 19.5}$$

To find g_{m_1}

$$g_{m_1} = GBC_c = 2\pi \times 10 \times 10^6 \times 2.3 \times 10^{-12} = 144.5\ \mu\Omega^{-1}$$

$$g_{m_6} = 10\, g_{m_1} = 1.44\ m\Omega^{-1}$$

Input Common mode range

$$V_{SS} + V_{DSat_5} + V_{DSat_1} + V_{TN} < V_{icm} < V_{DD} - V_{DSat_3} - V_{Tp} + V_{TN}$$

$V_{icm} = 0.55V$, $V_{DSat} = 0.2V$, $|V_{Tp}| = 0.4V$

$$\Rightarrow \quad 0.55 > V_{SS} + 0.8$$

$$\Rightarrow \quad V_{SS} < -0.25$$

Let's take $V_{SS} = -V_{DD} = -1.1V$

$0.55 < 1.1 - 0.2 - 0.4 + 0.4$ → verified.

$$\left(\frac{W}{L}\right)_{3,4} > \frac{I_5}{K_p \left[V_{DSat_3}\right]^2}$$

$$\Rightarrow \boxed{\left(\frac{W}{L}\right)_{3,4} > 1.6}$$

Now $S_{1,2}$

$$\left(\frac{W}{L}\right)_{1,2} = \frac{g_{m_1}^2}{2K_n' I_1} = \frac{(144\times10^{-6})^2}{2\times 569\times10^{-6}\times\frac{23}{2}\times10^{-6}}$$

$$\left(\frac{W}{L}\right)_{1,2} = 1.6$$

Similar to $S_{3,4}$

$$V_{DSat5} = 0.2$$

$$S_5 \geq \frac{2I_5}{K_n'(V_{DSat5})^2} = 2$$

$$\Rightarrow \left(\frac{W}{L}\right)_5 \geq 2$$

From DC balance equations

$$V_{SG6} = V_{SG4}$$

$$S_6 = \frac{g_{m6}}{g_{m4}} S_4$$

$$\Rightarrow \left(\frac{W}{L}\right)_6 = 22.15\sqrt{\left(\frac{W}{L}\right)_4} > 125$$

$$\Rightarrow \left(\frac{W}{L}\right)_4 > 31$$

Therefore let's take $\left(\frac{W}{L}\right)_{3A} = 35$

$$\Rightarrow \left(\frac{W}{L}\right)_6 = 131$$

$$I_6 = \frac{(g_{m6})^2}{2K_p \times \left(\frac{W}{L}\right)_6} = 43\,\mu A$$

$$\left(\frac{W}{L}\right)_7 = \left(\frac{W}{L}\right)_5 \times \frac{I_6}{I_5} \geq 3.74$$

Let's take $S_7 = 4 \Rightarrow S_5 = 2.14$

Now Nulling Resistor

for z to on top of P_2

$$R_z = \frac{1}{g_{m6}}\left(\frac{C_L + C_c}{C_c}\right)$$, Since R_z is realised using NMOS

$$\Rightarrow \left(\frac{W}{L}\right)_8 = \frac{\left(\frac{W}{L}\right)_6}{1 + \frac{C_L}{C_c}} = 25$$

Let Recheck the gain:

$$A_0 = \frac{2 g_{m1} g_{m6}}{I_6(\lambda_6+\lambda_7)(I_5)(\lambda_2+\lambda_4)}$$

$$= \frac{2 \times 10 \times (141 \times 10^{-6})^2}{13 \times 10^{-6} \times 4 \times 23 \times 10^{-6}} \geq 104$$

Final Sizings

$S_{1,2} = 1.6$, $S_{3,4} = 35$, $S_5 = 2.14$, $S_6 = 131$

$S_7 = 4$, $S_8 = 25$

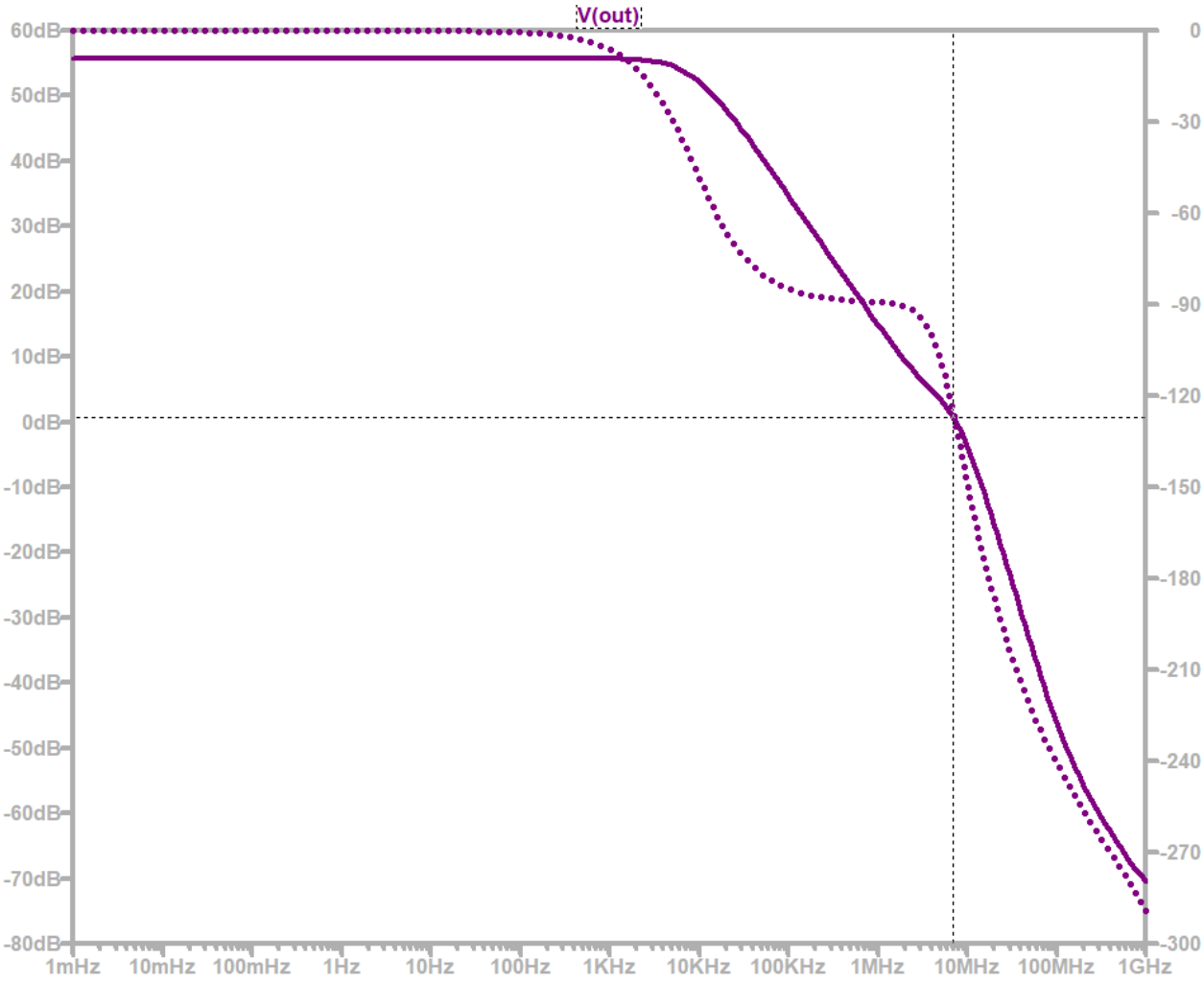
Sanity check ✓

For DC balance

$$\frac{S_6}{S_4} = \frac{2S_7}{S_5} = \frac{131}{35} = 2 \times \frac{4}{2.14} \text{ (verified)}$$

1.3 Plots

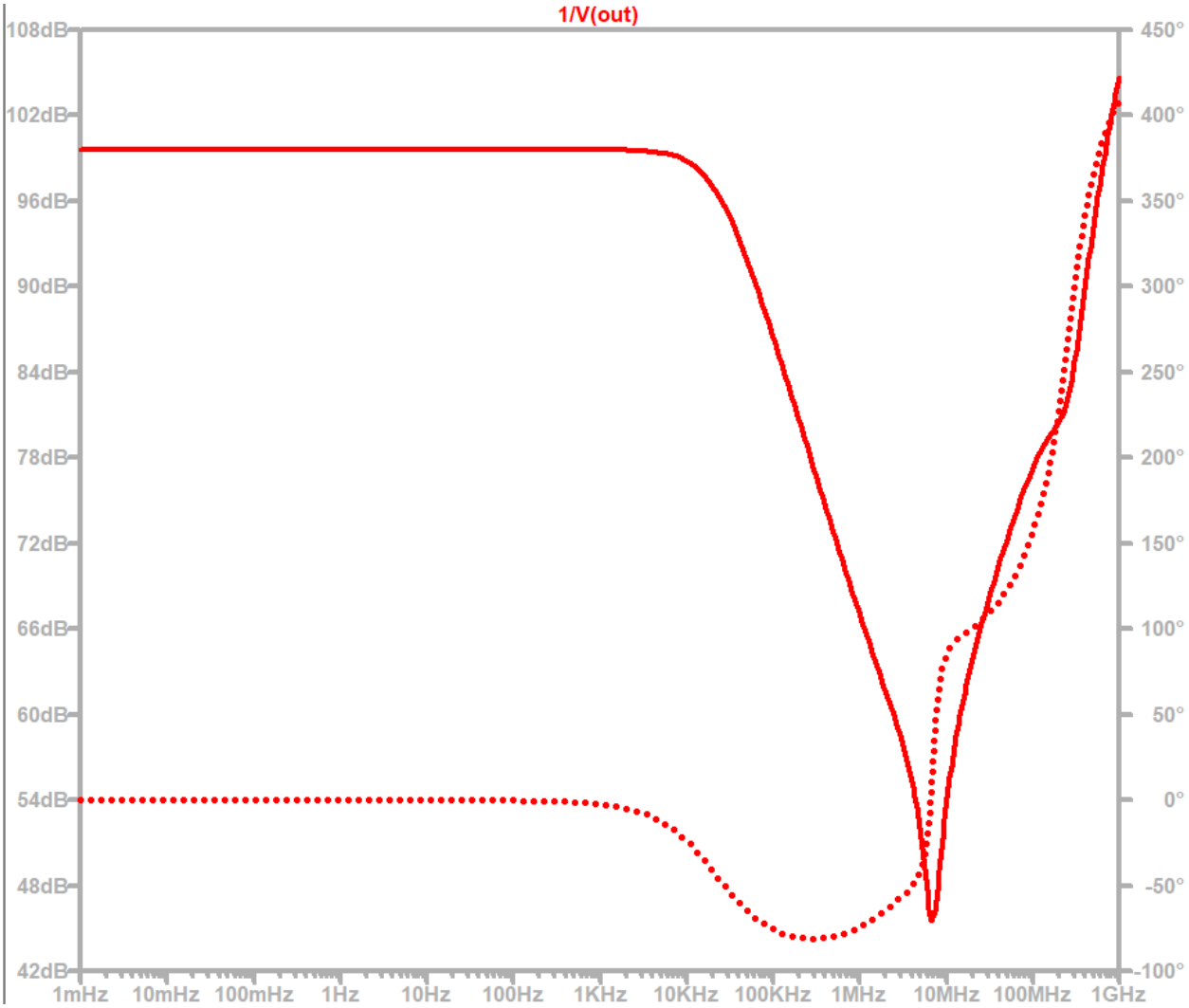
Bodeplot



Bode plot

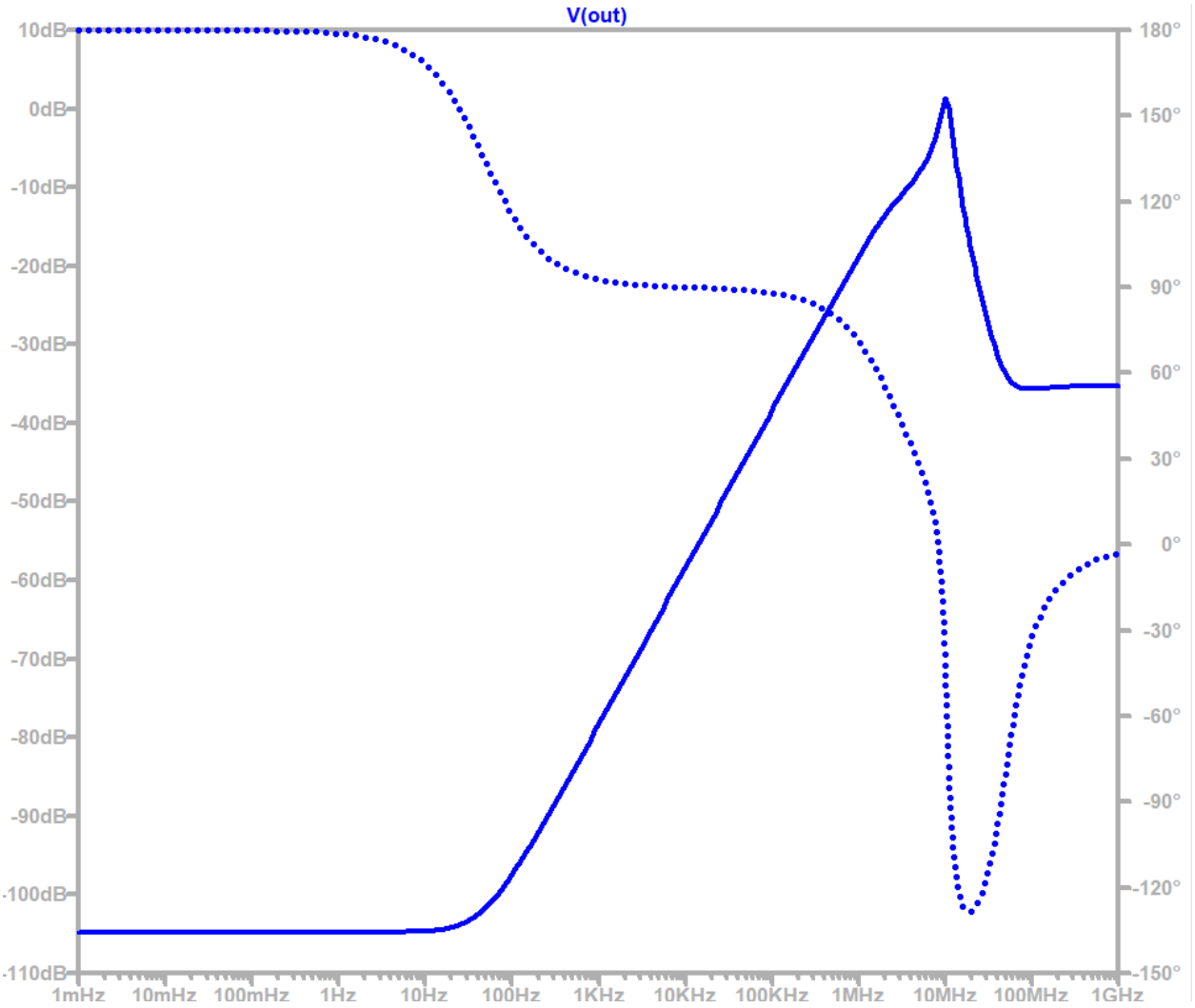
- We can see that the device satisfies all specified design requirements from the plot.

Common-mode rejection ratio (CMRR)



CMRR

Power-supply rejection ratio (PSRR)



PSRR

2 Question 2

2.1 Problem Statement

2. Connect the above op-amp in unity-gain feedback and submit the following plots:

. • Step-response when the output starts slewing for both positive and negative steps.

. • Output vs input when input DC voltage is varied from 0 V to supply voltage.

. • Output spectrum when (0.1 sin $2\pi 1000t$) V is applied at the input. Also calculate the total harmonic distortion (THD).

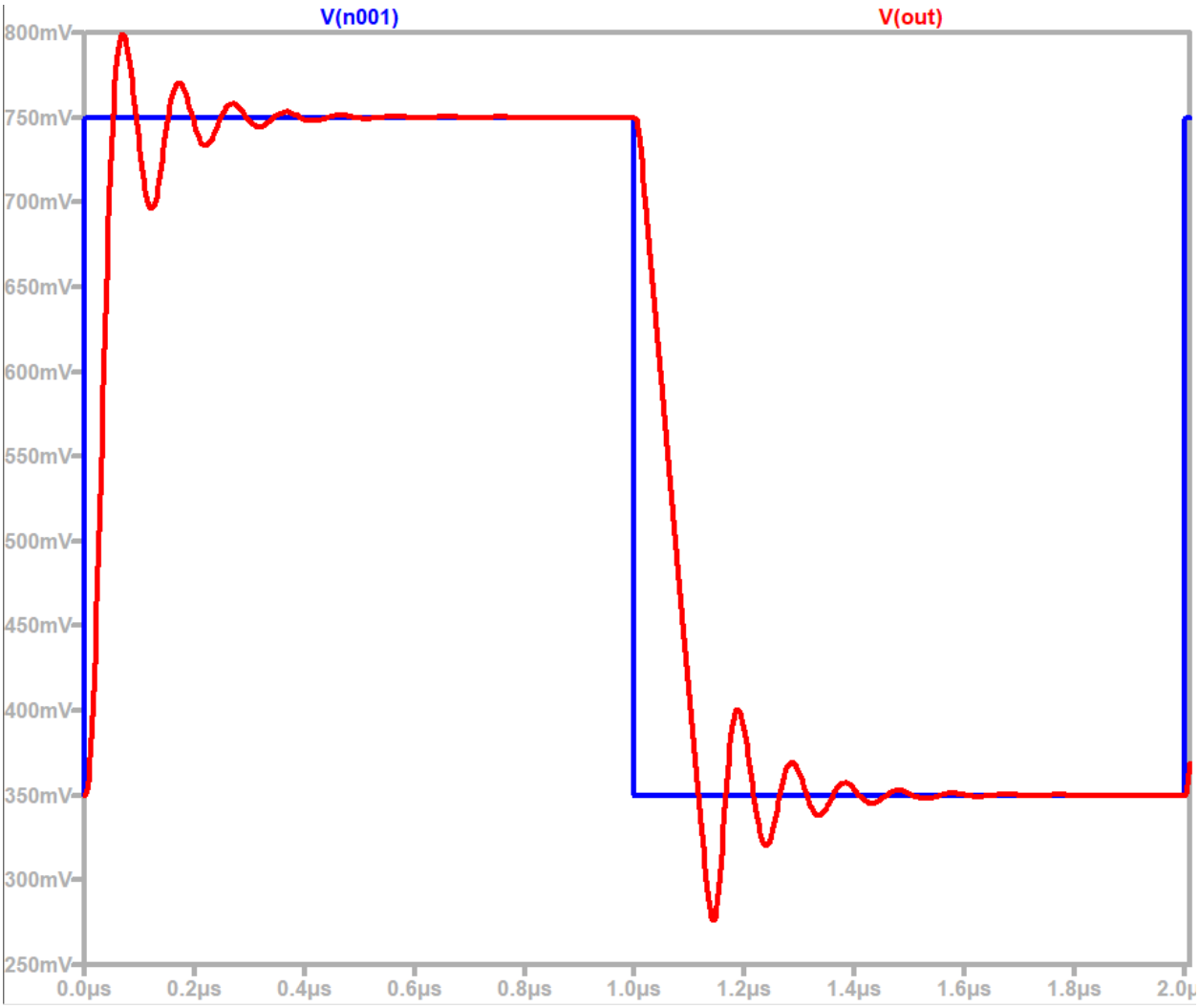
2.2 Spice Netlist

XX1 VDD Out N001 Out VSS twostageopamp
V1 VDD 0 1.1
V2 0 VSS 1.1
V3 N001 0 SINE(0 0.1 1k)
C1 Out 0 10p

* block symbol definitions
.subckt twostageopamp VDD Vn Vp Out VSS
M1 N003 Vn N004 N004 NMOS l=L w=W1 ad='2*65n*W1' as='2*65n*W1' pd='2*(2*65n+W1)' ps='2*(2*65n+W1)' m=M
M2 N001 Vp N004 N004 NMOS l=L w=W2 ad='2*65n*W2' as='2*65n*W2' pd='2*(2*65n+W2)' ps='2*(2*65n+W2)' m=M
M3 VDD N003 N003 VDD PMOS l=L w=W3 ad='2*65n*W3' as='2*65n*W3' pd='2*(2*65n+W3)' ps='2*(2*65n+W3)' m=M
M4 VDD N003 N001 VDD PMOS l=L w=W4 ad='2*65n*W4' as='2*65n*W4' pd='2*(2*65n+W4)' ps='2*(2*65n+W4)' m=M
M5 N004 N005 VSS VSS NMOS l=L w=W5 ad='2*65n*W5' as='2*65n*W5' pd='2*(2*65n+W5)' ps='2*(2*65n+W5)' m=M
M6 VDD N001 Out VDD PMOS l=L w=W6 ad='2*65n*W6' as='2*65n*W6' pd='2*(2*65n+W6)' ps='2*(2*65n+W6)' m=M
M7 Out N005 VSS VSS NMOS l=L w=W7 ad='2*65n*W7' as='2*65n*W7' pd='2*(2*65n+W7)' ps='2*(2*65n+W7)' m=M
Cc1 N002 Out 2.3p
M8 N005 N005 VSS VSS NMOS l=L w=W9 ad='2*65n*W9' as='2*65n*W9' pd='2*(2*65n+W9)' ps='2*(2*65n+W9)' m=M
I1 VDD N005 23µ
M9 N001 VDD N002 N002 NMOS l=L w=W2 ad='2*65n*W2' as='2*65n*W2' pd='2*(2*65n+W2)' ps='2*(2*65n+W2)' m=M
.param L=1u M=1 W1=1.6u W2=1.6u W3=35u W4=35u W5=2.14u W6=160u W7=4u W8=25u W9=2.14u
.include 65nm_NMOS_bulk.pm
.include 65nm_PMOS_bulk.pm
.ends twostageopamp
.model NMOS NMOS
.model PMOS PMOS
.lib C:standard.mos
.tran 4m
.four 1kHz V(out)
.backanno
.end

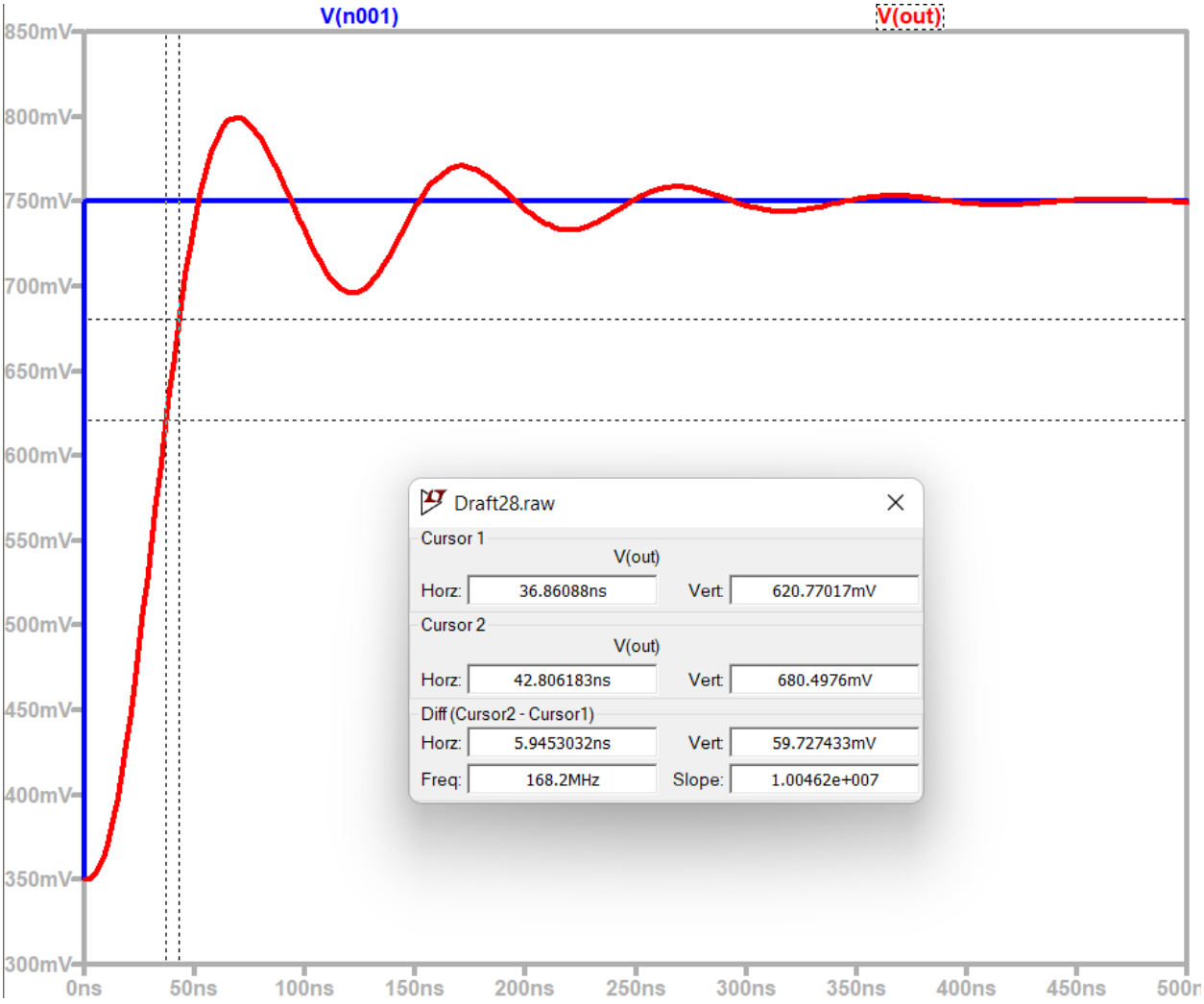
2.3 Plots

Step Response



Output Response for pulse

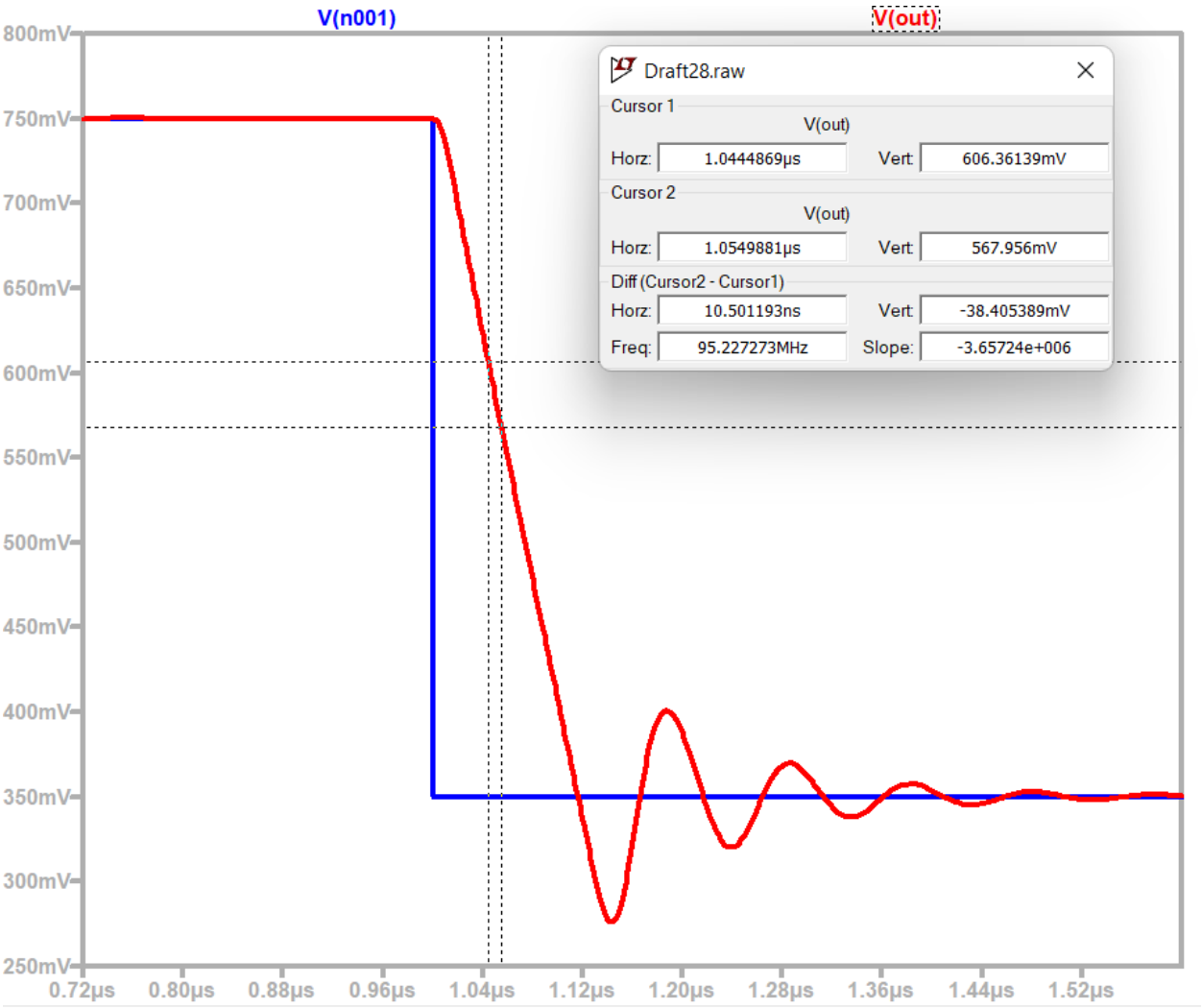
Positive Step



Positive Step Response

- Positive slew rate is 10.04 V/µs.

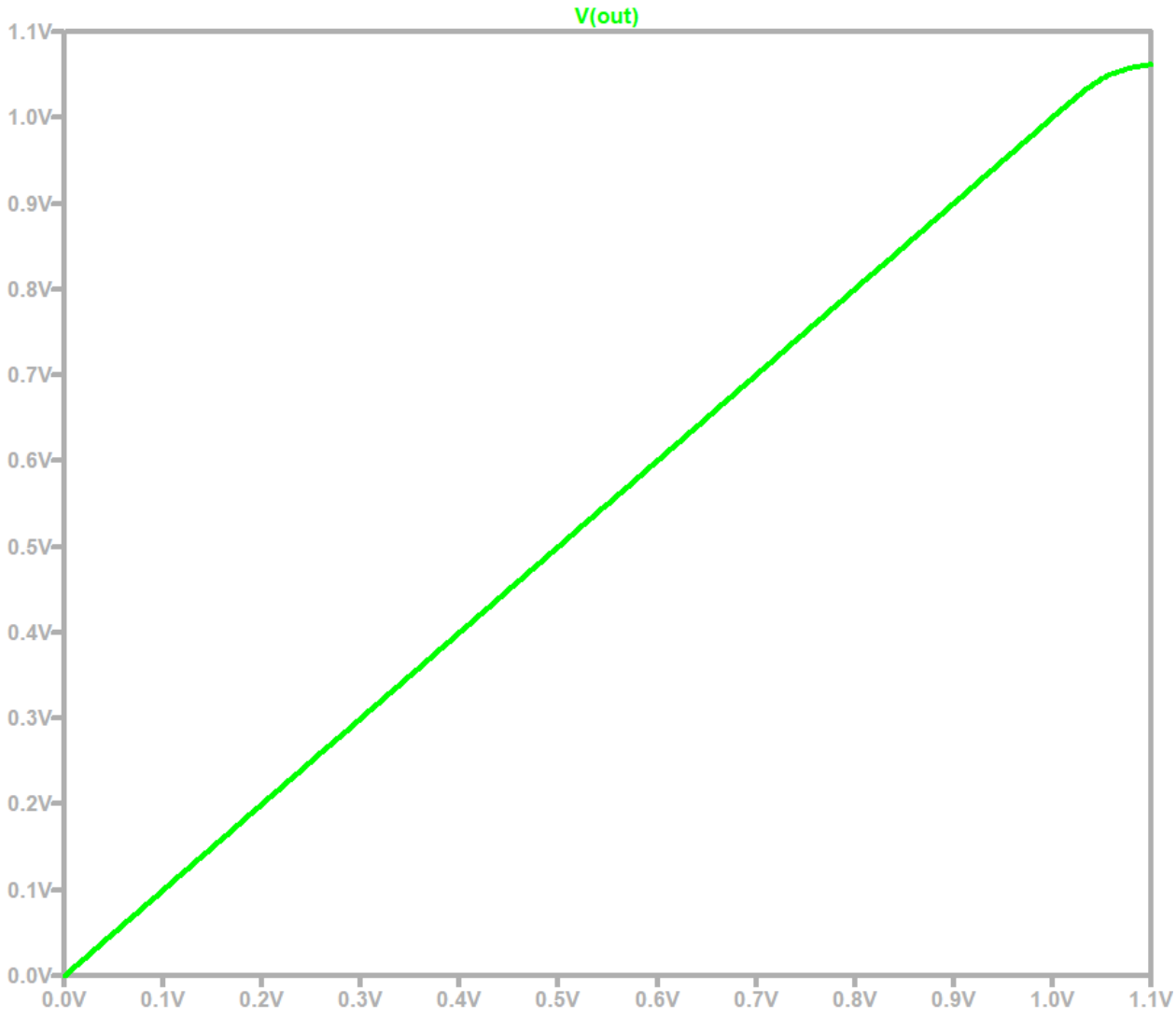
Negative Step



Negative Step Response

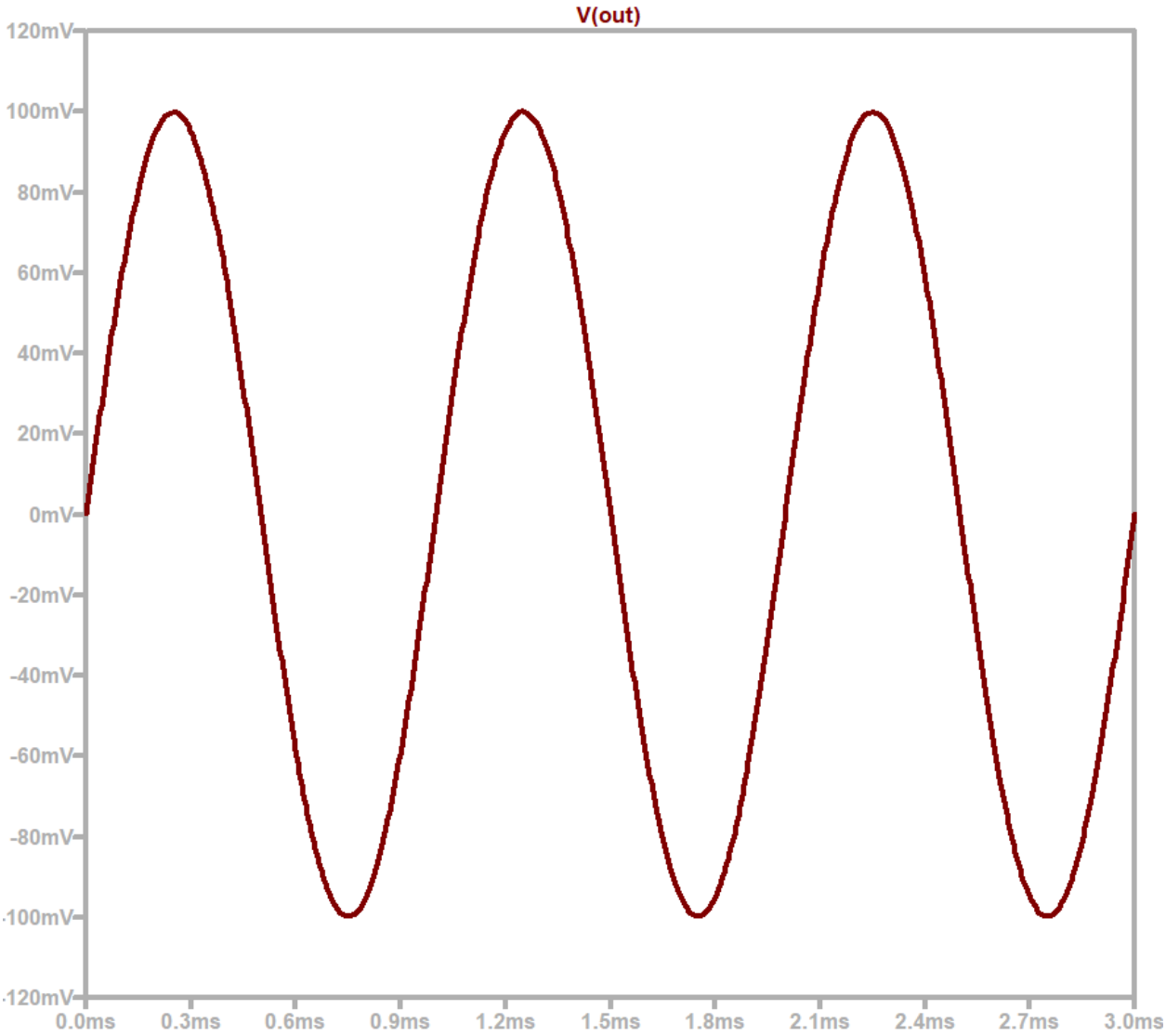
- Negative slew rate is -3.65 V/µs.

Input Dc sweep Response



Output

Output spectrum when V_{in} = (0.1 sin 2π1000t) V



Output

- The total harmonic distortion (THD) is 0.111232%.


thank
you