Analog Circuits(EE3300)
Simulation Exercise 1

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Contents

1 Problem statement

1. Design an amplifier with biasing to meet the following specifications:

   - Gain: 20 dB
   - Source resistance: 1 kΩ
   - Load resistance: 50 Ω
   - Frequency: 1kHz

(Given: One voltage source of 1.1V and current source of 10 μA.)(Given: One voltage source of 1.1V and current source of 10 μA.)

Objective is to meet the above specifications while maximizing the signal swing. You can cascade multiple stages if needed.

Submit the following:

- Hand calculation for choosing the device size and biasing elements. Use the square-law model extracted in the previous exercise. Final values can be changed based on simulation.
- Schematic screenshot and Final element values.
- Total harmonic distortion (THD) measures linearity of a system,

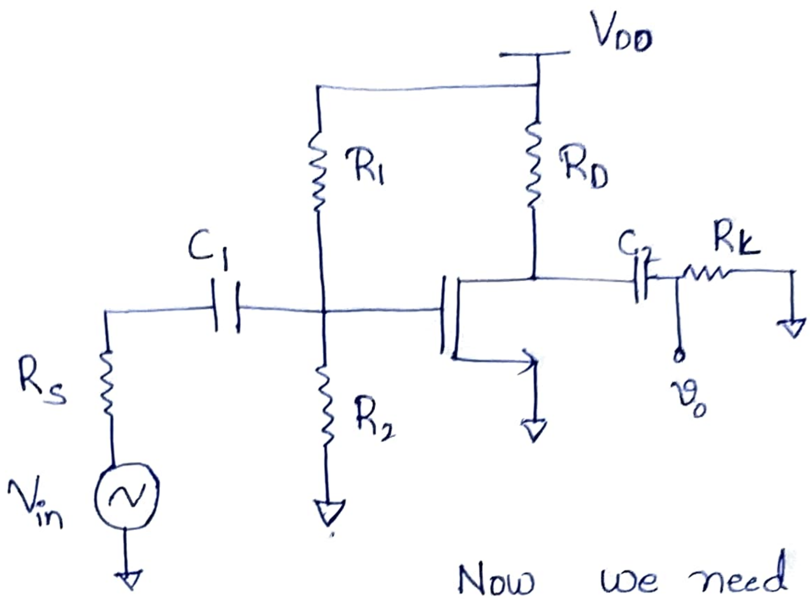
$$THD = \frac{\sqrt{V_2^2 + V_3^2 + ... + V_n^2}}{V_1} \quad (1)$$

  where, V_k is the rms value of kth harmonic.
  Calculate output voltage THD (in %) using LTspice for input amplitude of 1mV and 50 mV. Attach output FFT plots also.
- Frequency response from 10 Hz to 100 kHz.
- DC power consumed by the amplifier.
- Upload LTspice schematic as a separate file.

2 Hand Calculation

Hand Calculation

Single Cascade circuit Block:



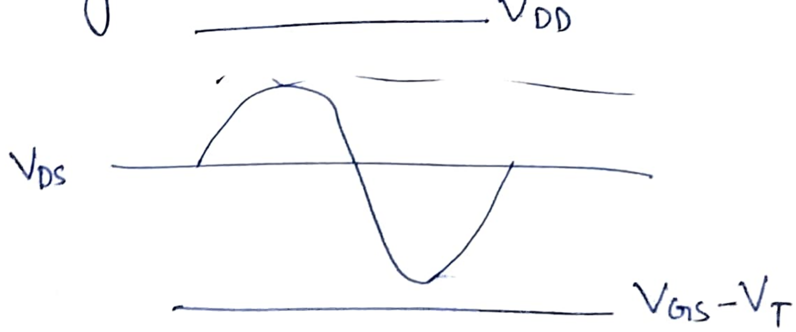
Now we need a total gain of 20dB

$\Rightarrow$ $\boxed{\dfrac{v_{final}}{V_{in}} = 10}$ Here we are cascading so

Let's say gain in first cascade is K_1

$$\Rightarrow \quad g_m (R_L // R_D) = K_1$$

Swing



To maximize swing V_{DS} should be mid value of V_{DD} and $V_{GS}-V_T$.

$$V_{DS} = \frac{V_{DD} + V_{GS} - V_T}{2}$$

$$V_{DS} = V_{DD} - I_{DS} R_D$$

$$I_{DS} = \frac{g_m}{2}(V_{GS} - V_T)$$

$$\Rightarrow V_{DD} - \frac{g_m R_D}{2}(V_{GS} - V_T) = \frac{V_{DD}}{2} + \frac{V_{GS} - V_T}{2}$$

$$\Rightarrow (1 + g_m R_D)(V_{GS} - V_T) = V_{DD}$$

$$\Rightarrow (V_{GS} - V_T) = V_x = \frac{V_{DD}}{1 + g_m R_D}$$

$$V_{DS} = \frac{V_{DD}\left\{\frac{2 + g_m R_D}{1 + g_m R_D}\right\}}{2}, \quad \text{But } g_m R_D \gg K_1$$

$$g_m R_D = 2 \times K_1 = 2$$
$$= 4$$

$$V_{DS} \approx \frac{V_{DD}}{2} \approx \frac{1.1}{2} = 0.55\,V$$

$$V_{GS} = V_T + \frac{V_{DD}}{1 + g_m R_D} \approx \text{around } 0.55$$

To calculate $\frac{W}{L}$, let's take $V_{GS} = 0.55$, $R_D = R_L = 50$

$\Rightarrow \quad g_m = \frac{1 \text{ to } 10}{(R_D // R_L)}$ = gain is in 1 to 10 because of cascade let's say 3.1

$\Rightarrow \quad g_m = \frac{3}{25}$

$\Rightarrow \quad \beta \frac{W}{L} (V_{GS} - V_T) = \frac{3}{25} \quad (\beta = 560\mu)$

$\Rightarrow \quad \frac{W}{L} (560) \times 10^{-6} \times 0.15 = \frac{3}{25}$

$\Rightarrow \quad \boxed{\frac{W}{L} \approx 1400}$

Now from these calculation ranges and simulation. Values we will eventually get a gain of 10 after using some cascade.

Note:

* I haven't used current source anywhere.

* To maximize swing the last Block of cascade should have highest gain.

Now capacitances

$\Rightarrow \dfrac{1}{WR} << C$

$\Rightarrow \quad C_1 >> \dfrac{1}{(2\pi \times 10^3) R}$

$\boxed{\omega = 2\pi \times 10^3}$

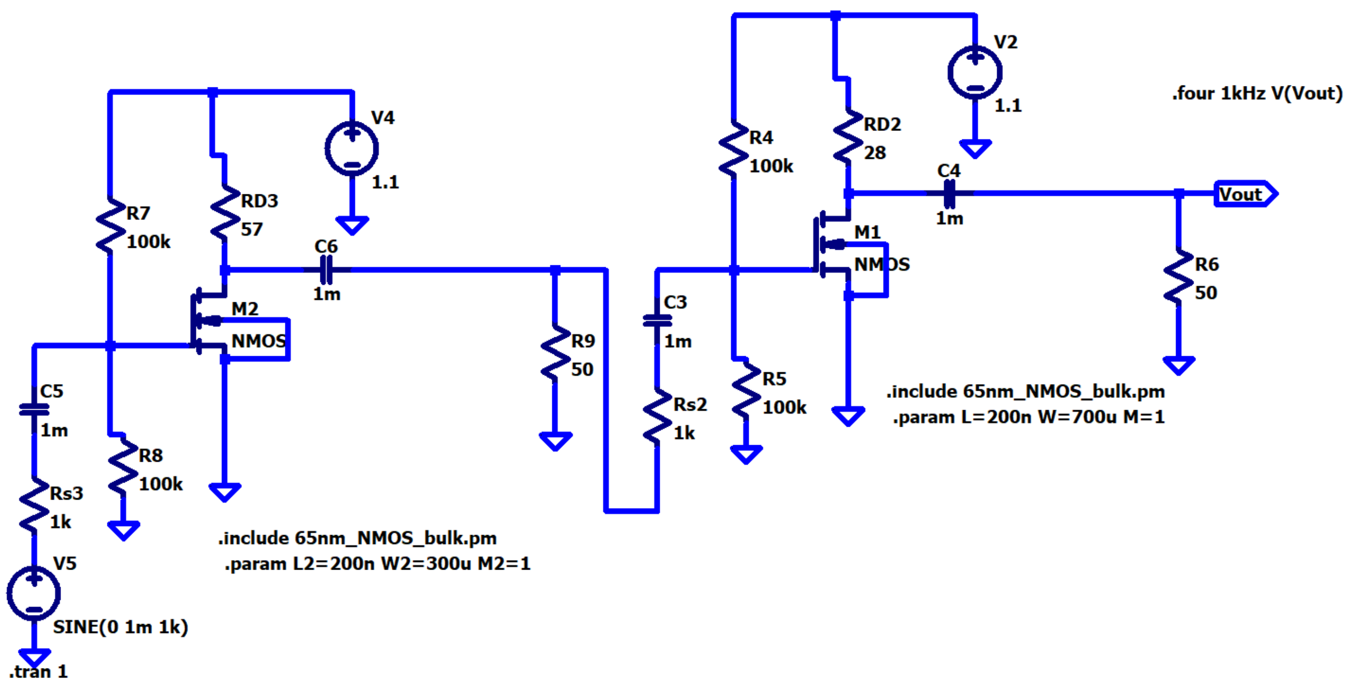
$\Rightarrow \quad C_1 >> \dfrac{1}{\omega (R_1 // R_2 + R_S)}$

$\Rightarrow \quad C_2 >> \dfrac{1}{\omega (R_D // R_L)}$

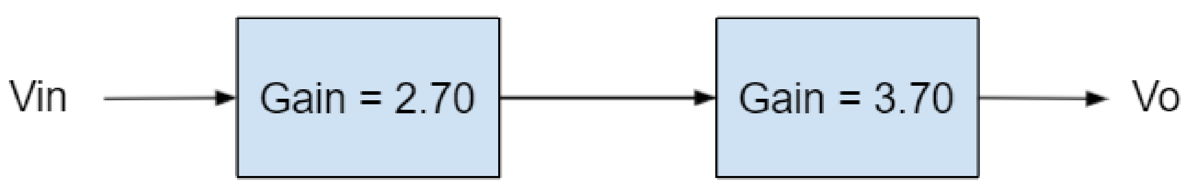
$R_1 // R_2 >> R_S$

Using this we can calculate and we capacitors.

3 Schematic



Amplifier Circuit Schematic



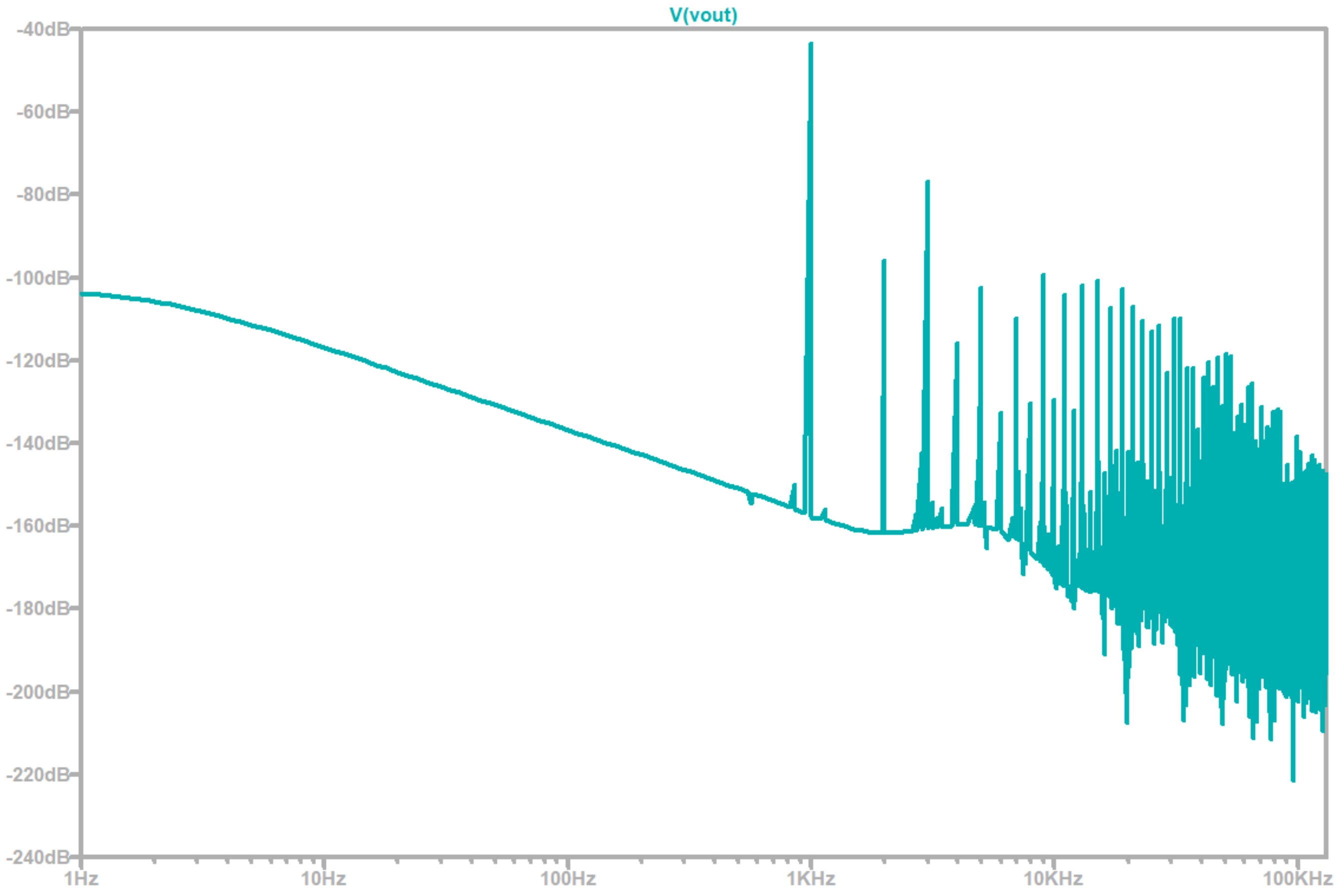
Cascade blocks

- The Gain of the first block is 2.7 and the second block is 3.7.
- The total gain is 10 i.e.

$$\frac{V_o}{V_{in}} = 10. \tag{2}$$

4 Output

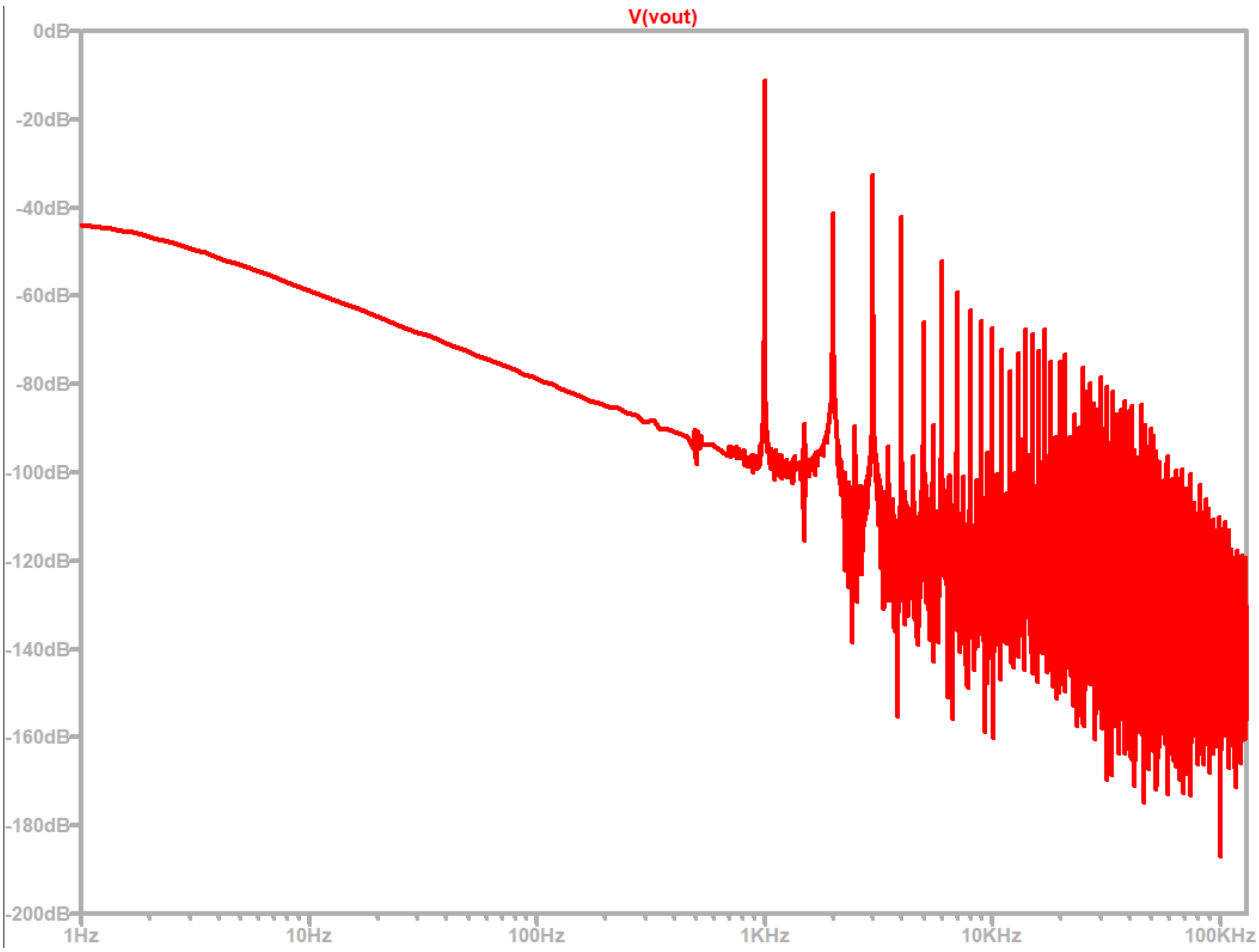
4.1 Output FFT For $V_{in} = 1$mV :



V_o FFT for $V_{in} = 1$mV

- Total Harmonic Distortion: 2.134221%.

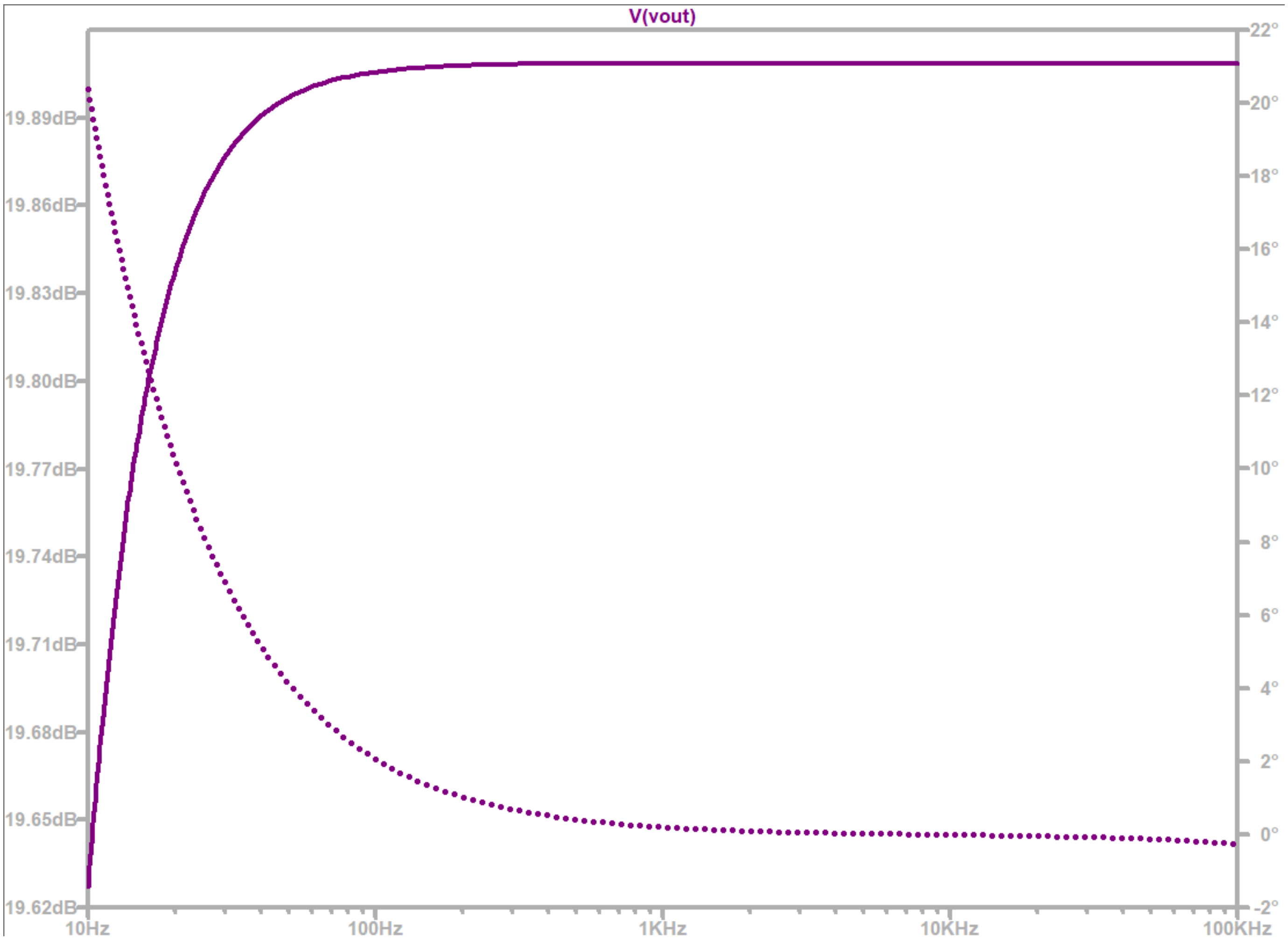
4.2 Output FFT For $V_{in} = 50\text{mV}$:



V_o **FFT for** $V_{in} = 50\text{mV}$

- Total Harmonic Distortion: 9.584068%.
- Here the Output gain was 7.2 because in simulation the swing limit was exceeded.

5 Frequency Response



Frequency Response

6 DC power consumed by the amplifier.

The power for source is the DC power.
Refer to the schematic for component labels.

$$P_{DC} = V_{DD}(I(Rd3) + I(Rd2) + I(R7) + I(R4)) \tag{3}$$

- Here I(Rd2) = 18.0271 mA, I(Rd3) = 8.98041 mA, I(R4) = 5.7543 μA, I(R7) = 5.62947 μA.

- DC power is 29.7 mWatt.


thank you