Analog Lab (EE2401)
Experiment 9: Double balanced mixer

EE19BTECH11041,
Srijith Reddy Pakala
Department of Electrical Engineering
IIT Hyderabad

April 22, 2021

1 Aim

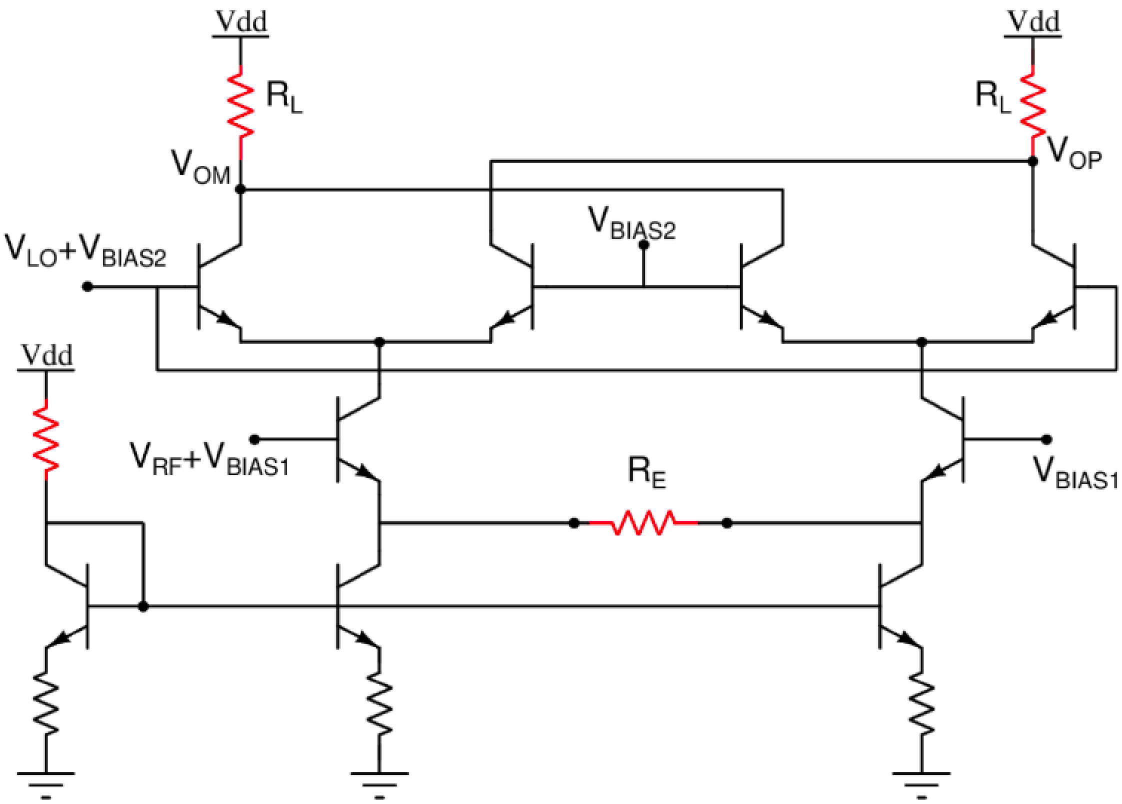
our aim here is to design a double balanced mixer.

Double balanced mixer

Both the LO and RF ports are balanced and all ports of the mixer are inherently isolated from each other and only multiplication component is present in output.

2 Problem statement

1. Below is the schematic of a double-balanced mixer present in MC1496 IC:



Components in RED are external to the IC.

- Input signal frequency (V_{RF}): 11 kHz
- V_{LO}: 10 kHz output from the oscillator designed in Exp. 5

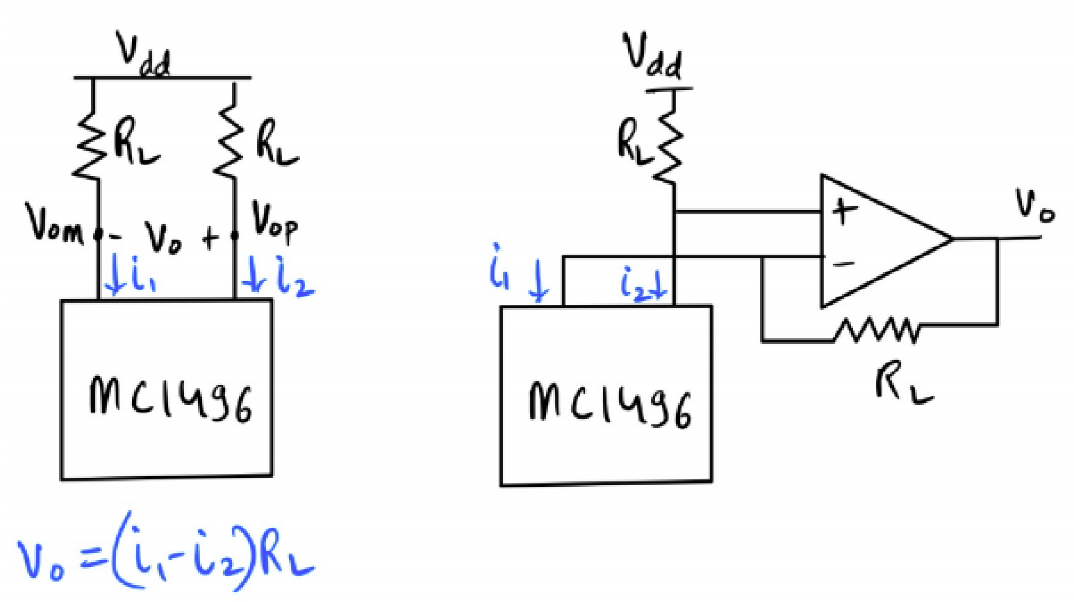
Plot transient simulation result and FFT of the output $V_O = V_{OP}V_{OM}$. Connect appropriate value of capacitors across R_L to filter out undesired components. Generate bias voltages from the supply. Connect bypass capacitors for the bias voltages.

2.Differential output of the mixer can be converted into single-ended by using the following circuit:

What is the expression for the single-ended output in terms of supply voltage, i_1, i_2 and R_L?

Use the signal specs given in the previous problem and perform the following

- Plot single-ended output. (Transient and FFT)

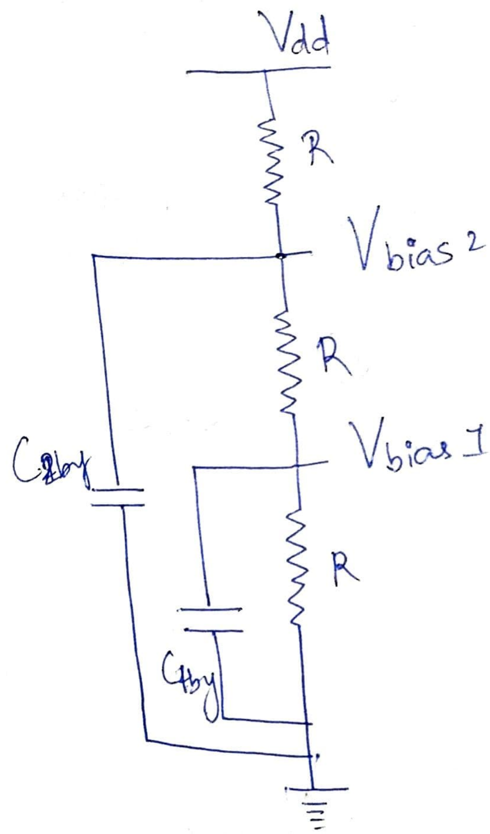


. • Apply only V_{RF} and V_{LO} one at a time and make your observation regarding the output.

In the Schematic.

$$V_{out} = V_{op} - V_{OM} = V_{RF} \frac{R_L}{R_E} \operatorname{Sgn}(V_{LO})$$

we need to choose R_E Such that gain is high but also such that current through npn is in proper region.



we have to use bypass capacitor to ensure that there is not current and it acts as voltage source.

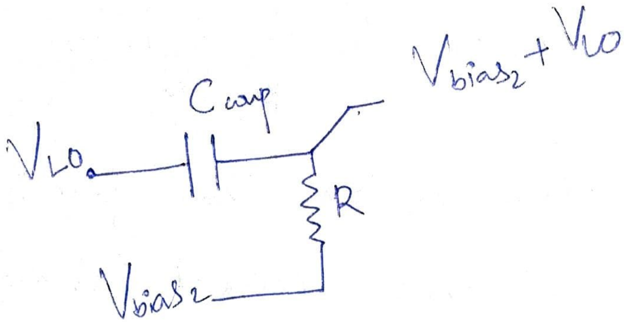
$$X_C = \frac{1}{2\pi f C} < \frac{R}{100}$$

X_C is should lower than R Such that we can shunt current.

$$\Rightarrow C = \frac{1}{2\pi f X_C}$$

$$\Rightarrow C > \frac{100}{2\pi f R}$$

using this we can find bias too.

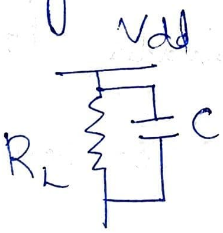


we now need to choose coupling capacitor. to remove any DC component present in V_{LO}

$$\frac{1}{2\pi f C} < \text{Some Resistance for given frequency}$$

& $C = 1\mu F$ for $f = 10KHz$
choose

Similarly for V_{RF}



Now to remove high frequency terms we are used cap across R_L

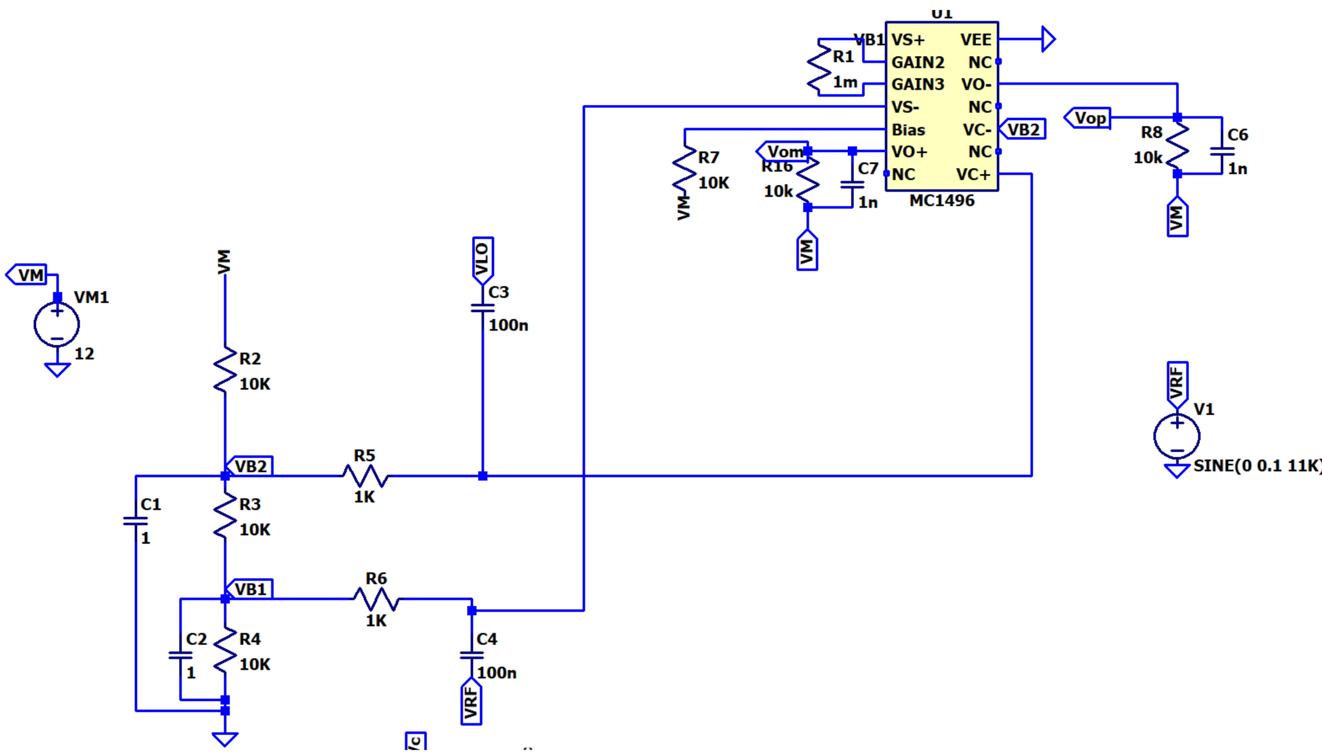
$$Z = \frac{R_L}{1 + j\omega R_L C} \qquad \omega_0 = \frac{1}{R_L C}$$

cutoff

$$\omega_0 > f_{LO} + f_{RF} \quad f_{RF} - f_{LO}$$

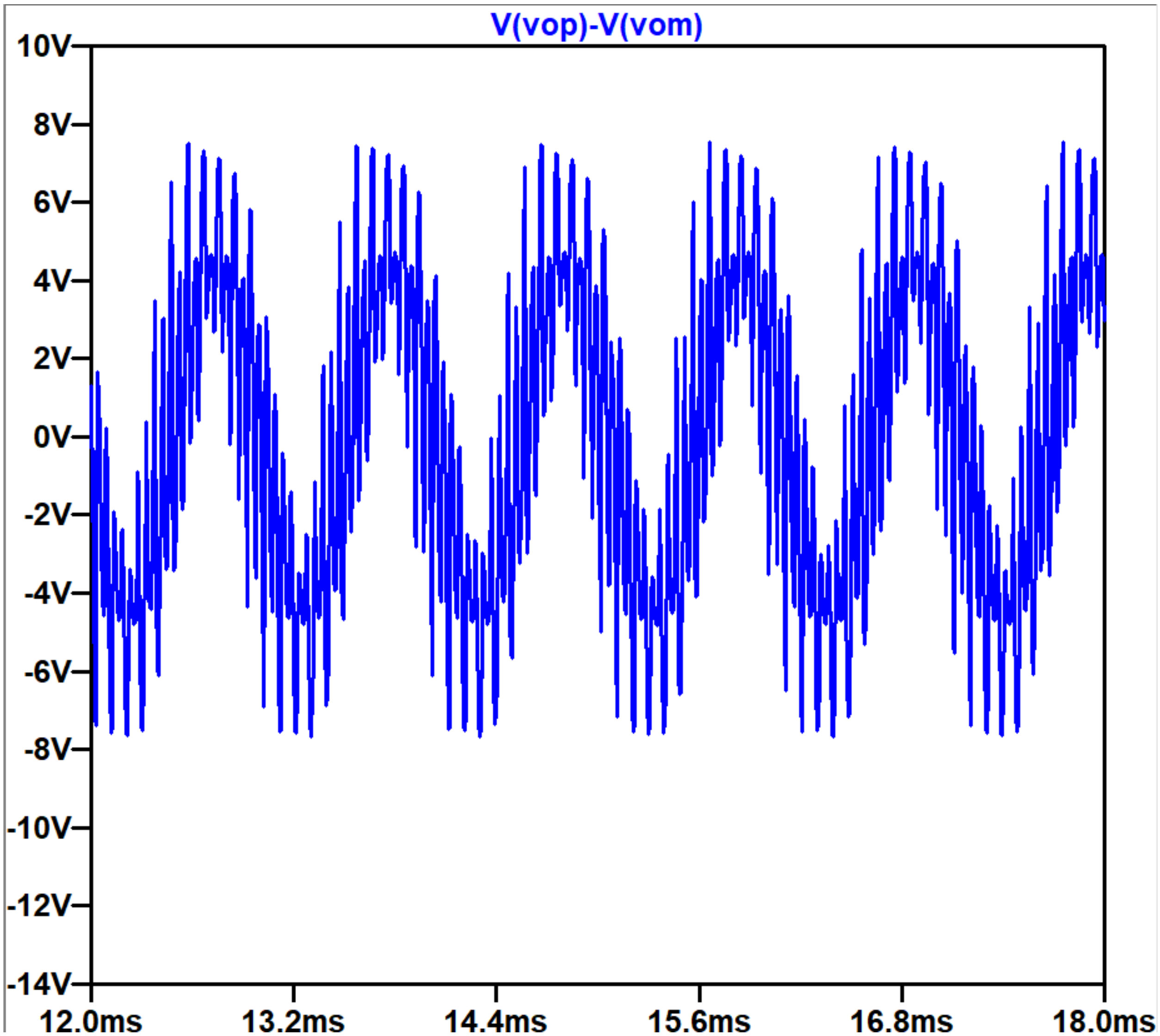
Question 1

Schematic of MC1496



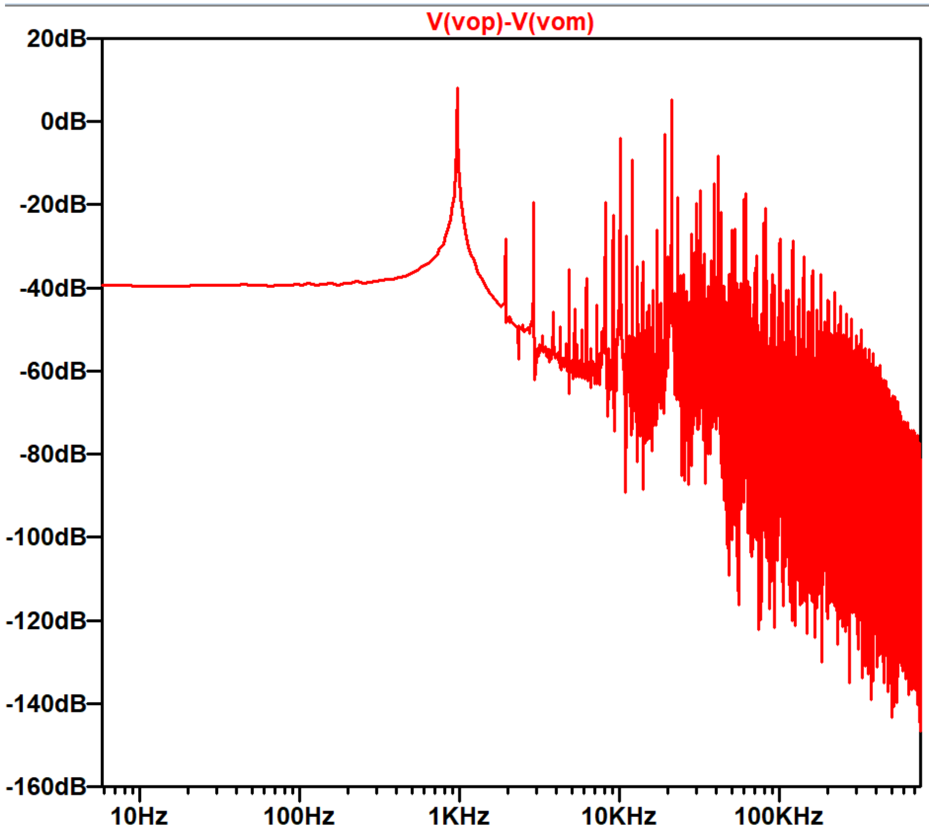
circuit schematic

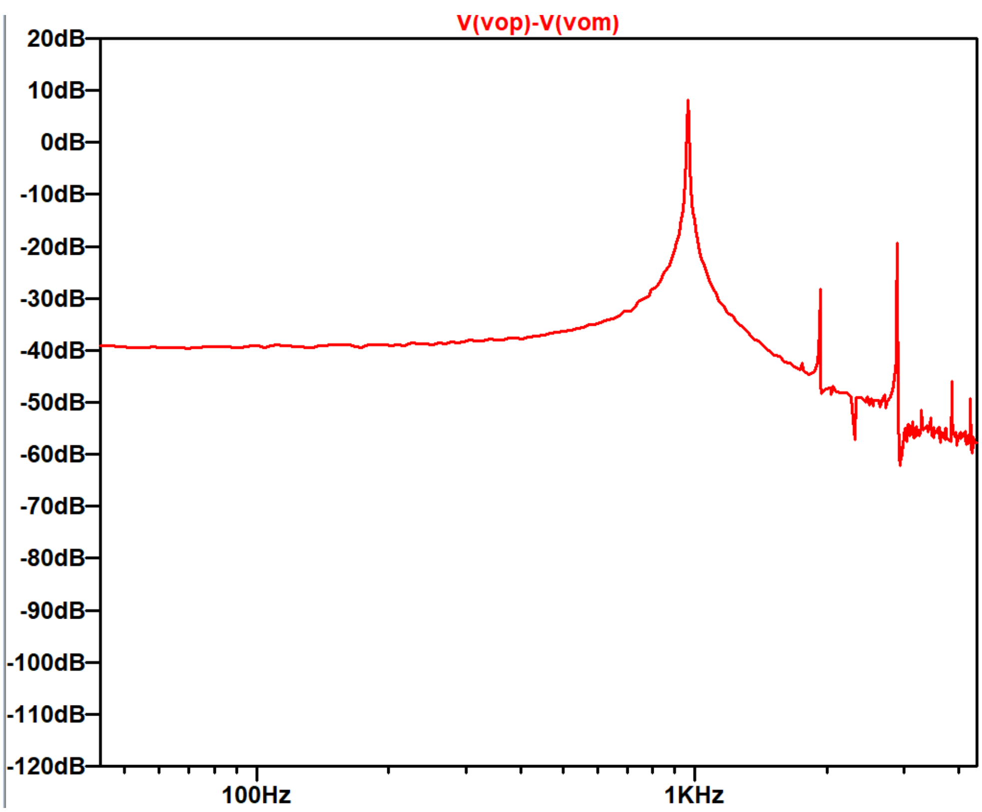
Output Vo transient plot

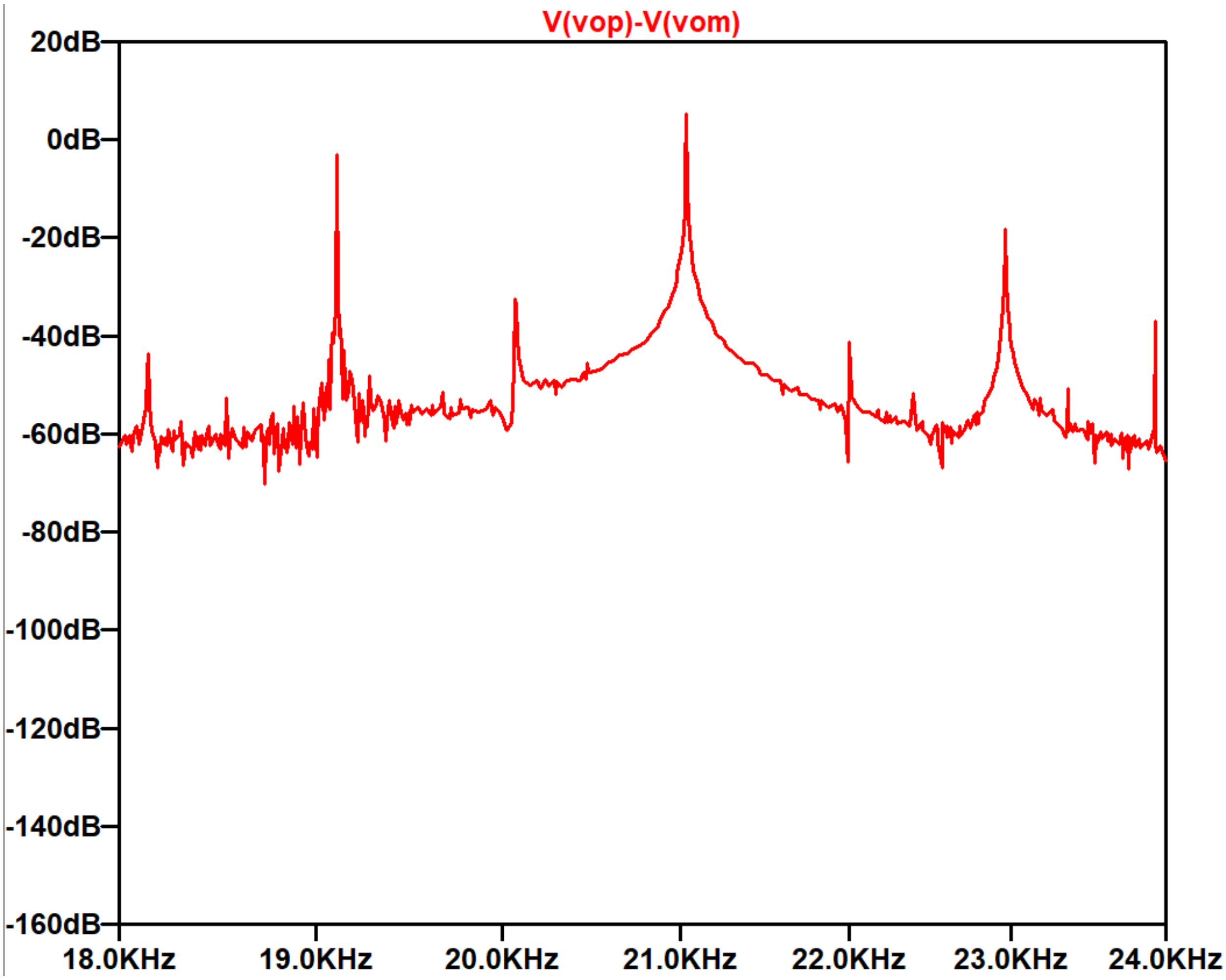


Output

Output FFT


V(vop)-V(vom)
20dB
0dB
-20dB
-40dB
-60dB
-80dB
-100dB
-120dB
-140dB
-160dB
10Hz
100Hz
1KHz
10KHz
100KHz

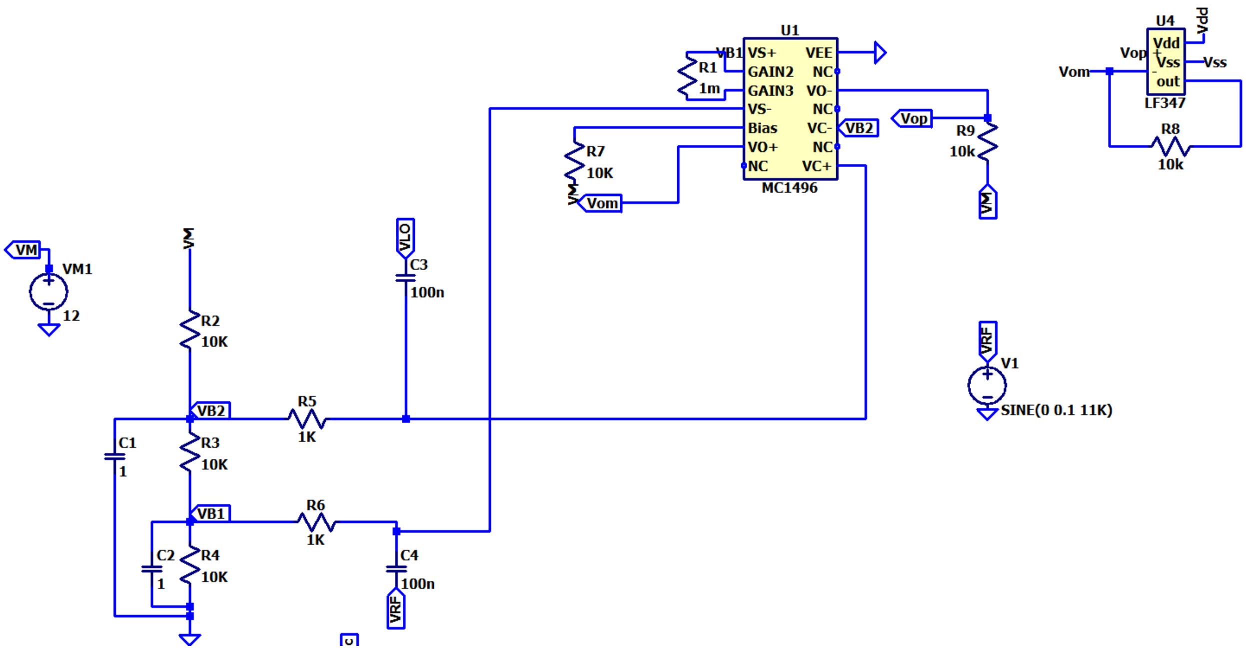

V(vop)-V(vom)
20dB
10dB
0dB
-10dB
-20dB
-30dB
-40dB
-50dB
-60dB
-70dB
-80dB
-90dB
-100dB
-110dB
-120dB
100Hz
1KHz



- We can see the peaks at 1KHz and 21KHz, But also at some other higher frequencies .

Question 2

Schematic

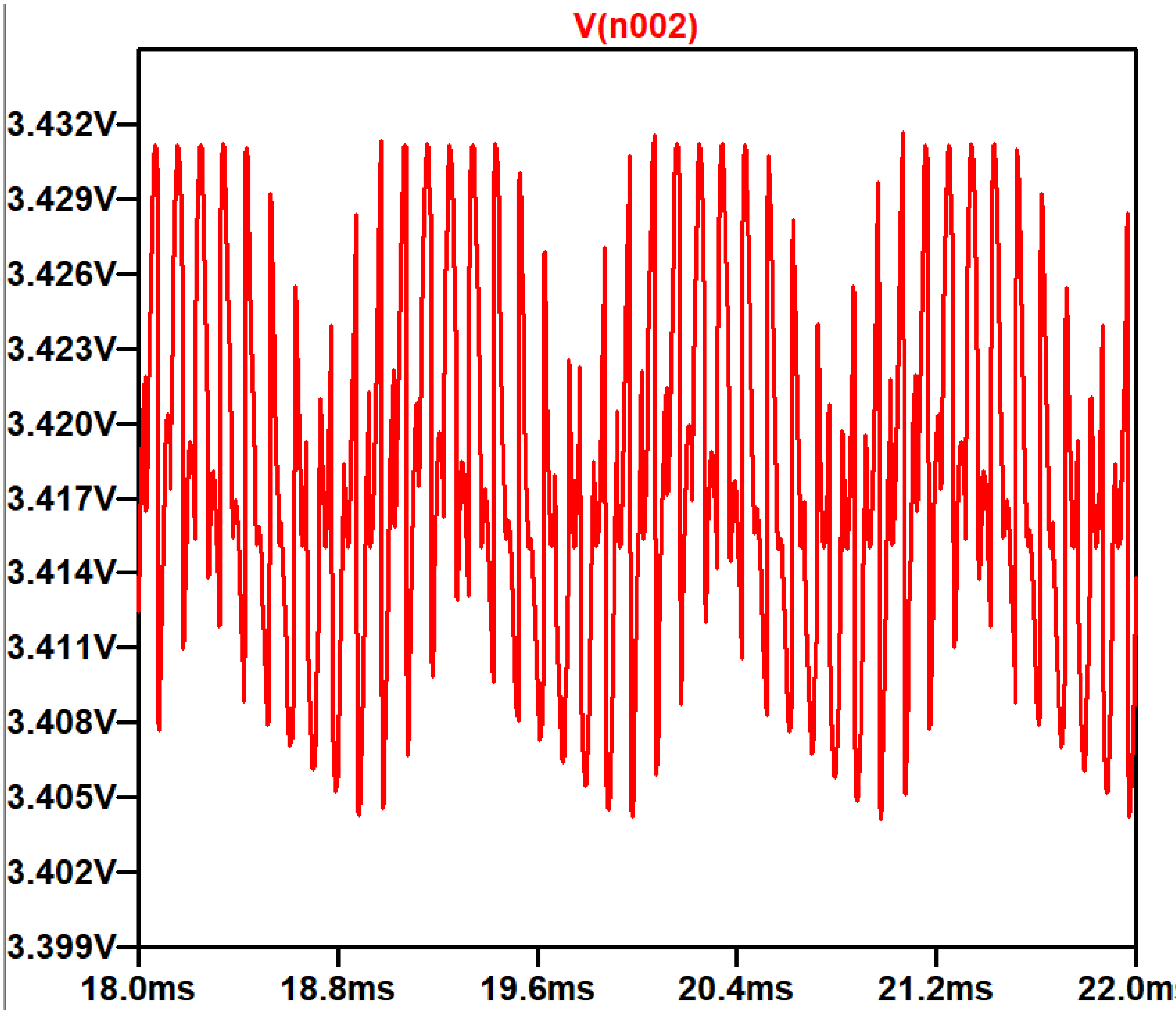


Schematic using MC1496 to obtain single-end output

From the circuit assuming virtual short we can find Vo.

$$Vo = (i_1 - i_2)R_L + V_{DD} \tag{1}$$

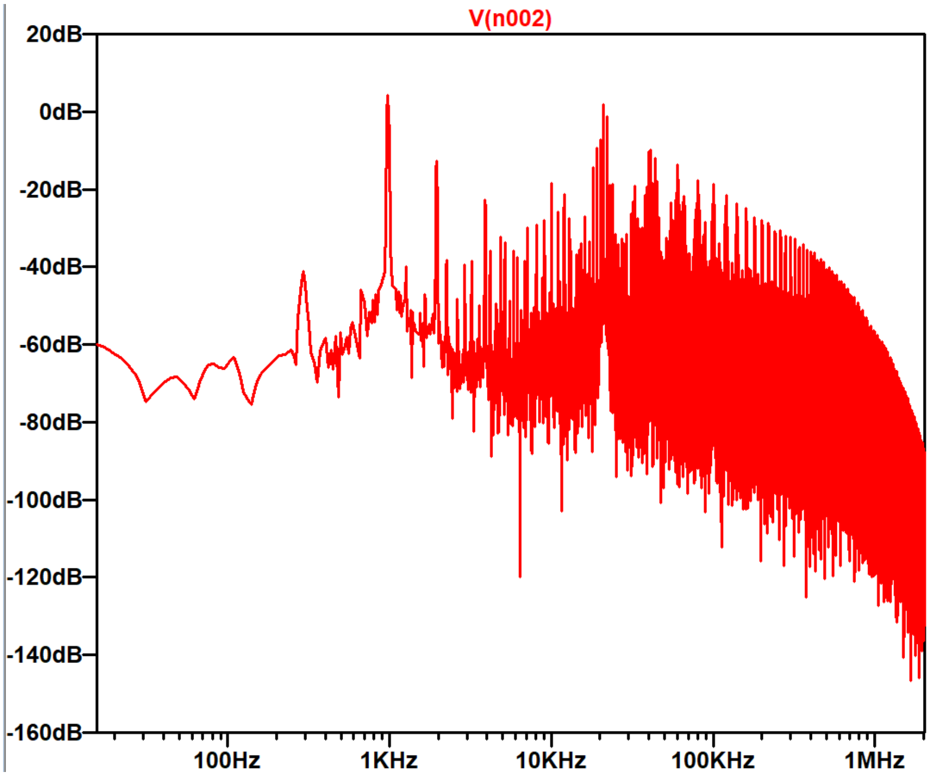
Output Vo transient plot

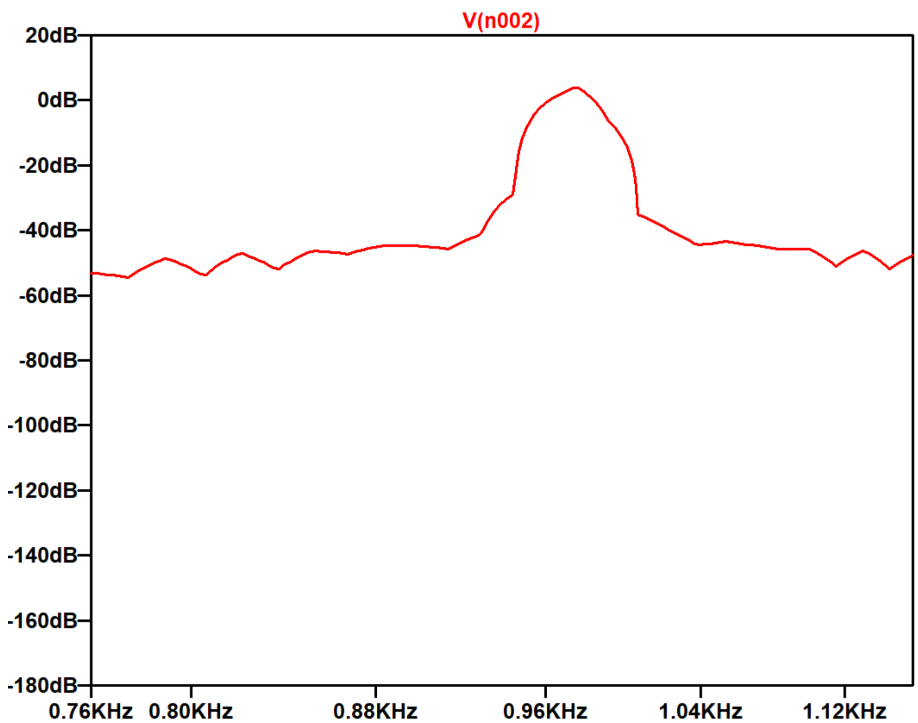


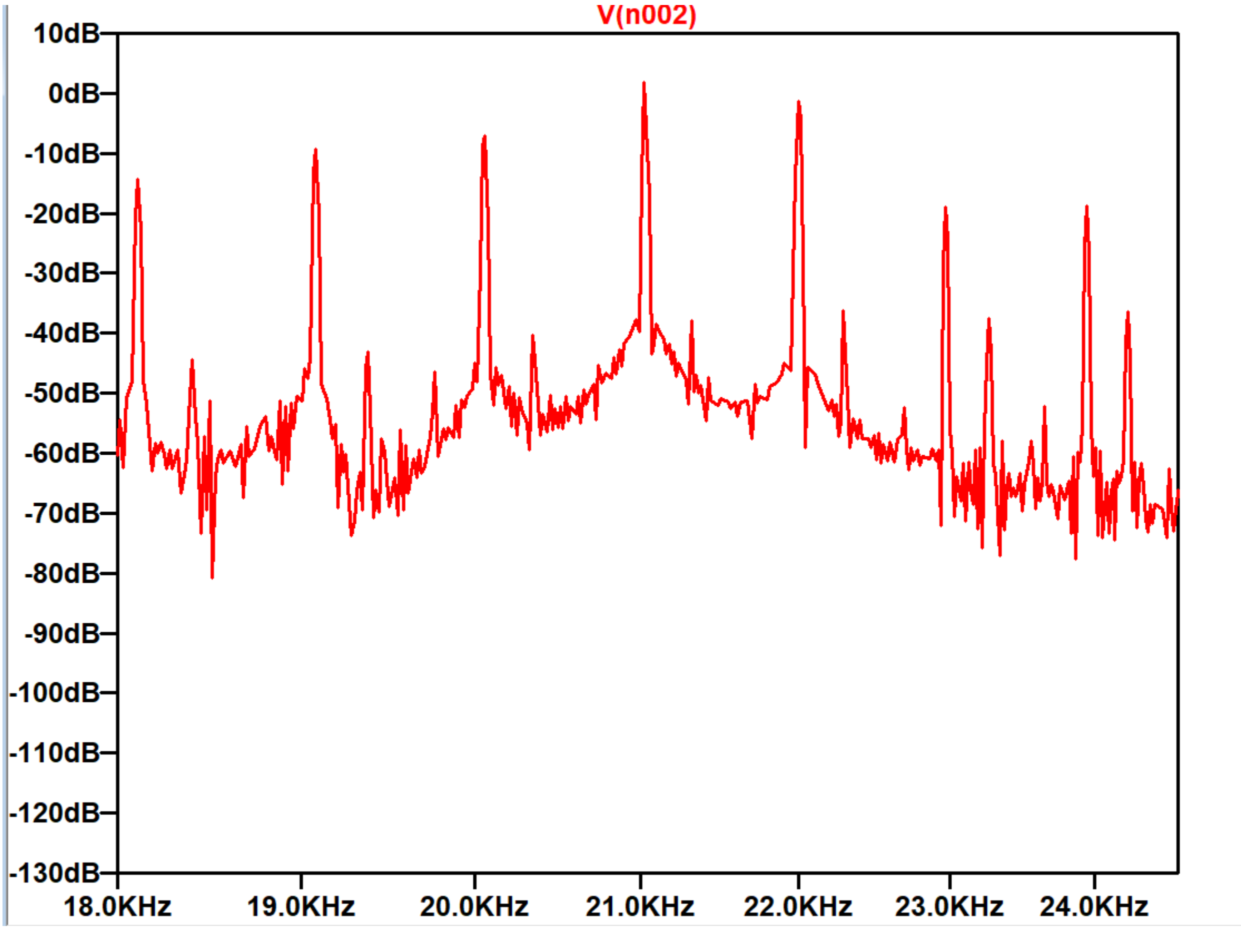
Output

- The output is not exactly same as previous question with bias of 3.5V .but similar although FFT is mostly same.

Output FFT

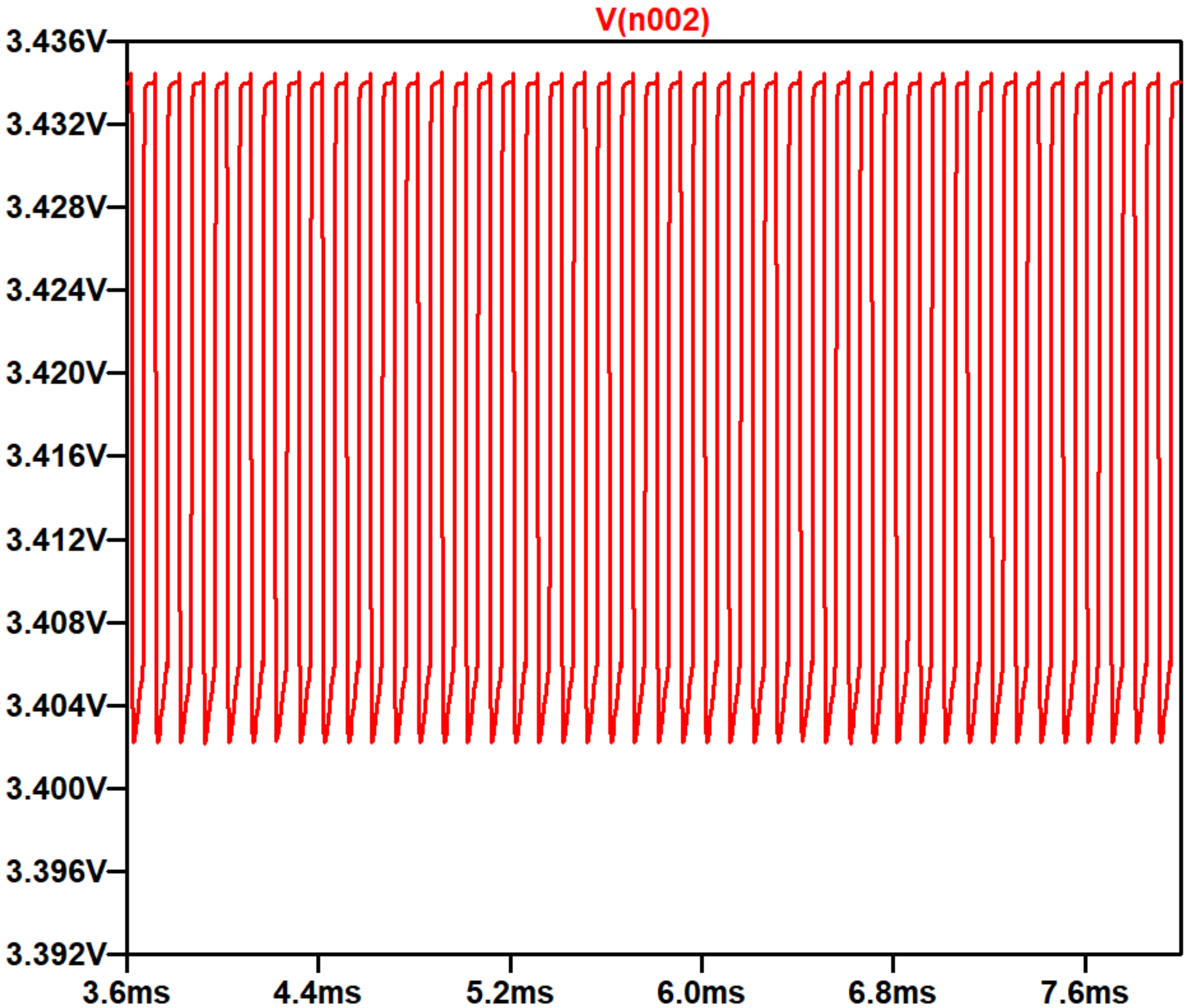

V(n002)
20dB
0dB
-20dB
-40dB
-60dB
-80dB
-100dB
-120dB
-140dB
-160dB
100Hz
1KHz
10KHz
100KHz
1MHz

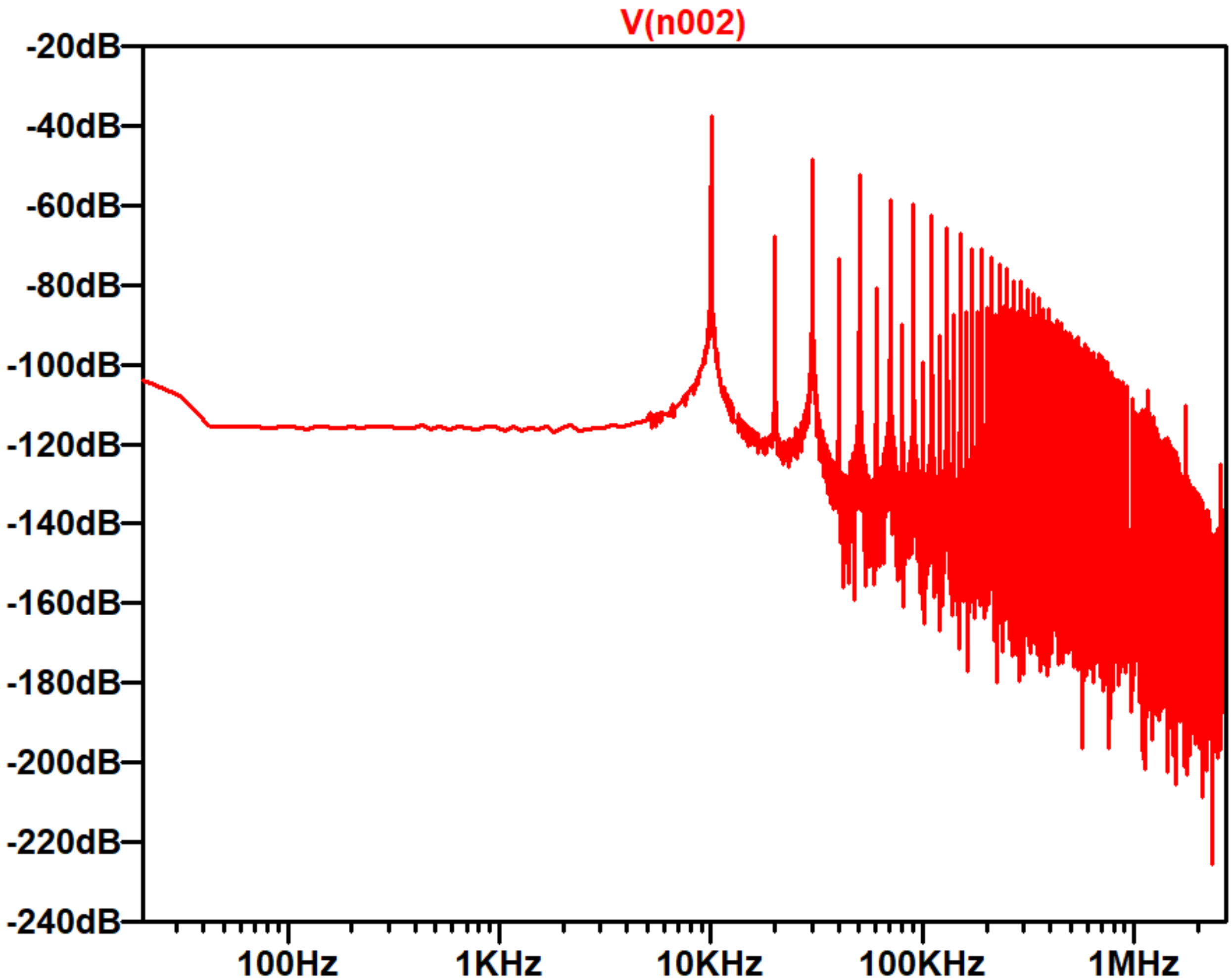

V(n002)
20dB
0dB
-20dB
-40dB
-60dB
-80dB
-100dB
-120dB
-140dB
-160dB
-180dB
0.76KHz
0.80KHz
0.88KHz
0.96KHz
1.04KHz
1.12KHz



- The FFT are similar to previous question plots.

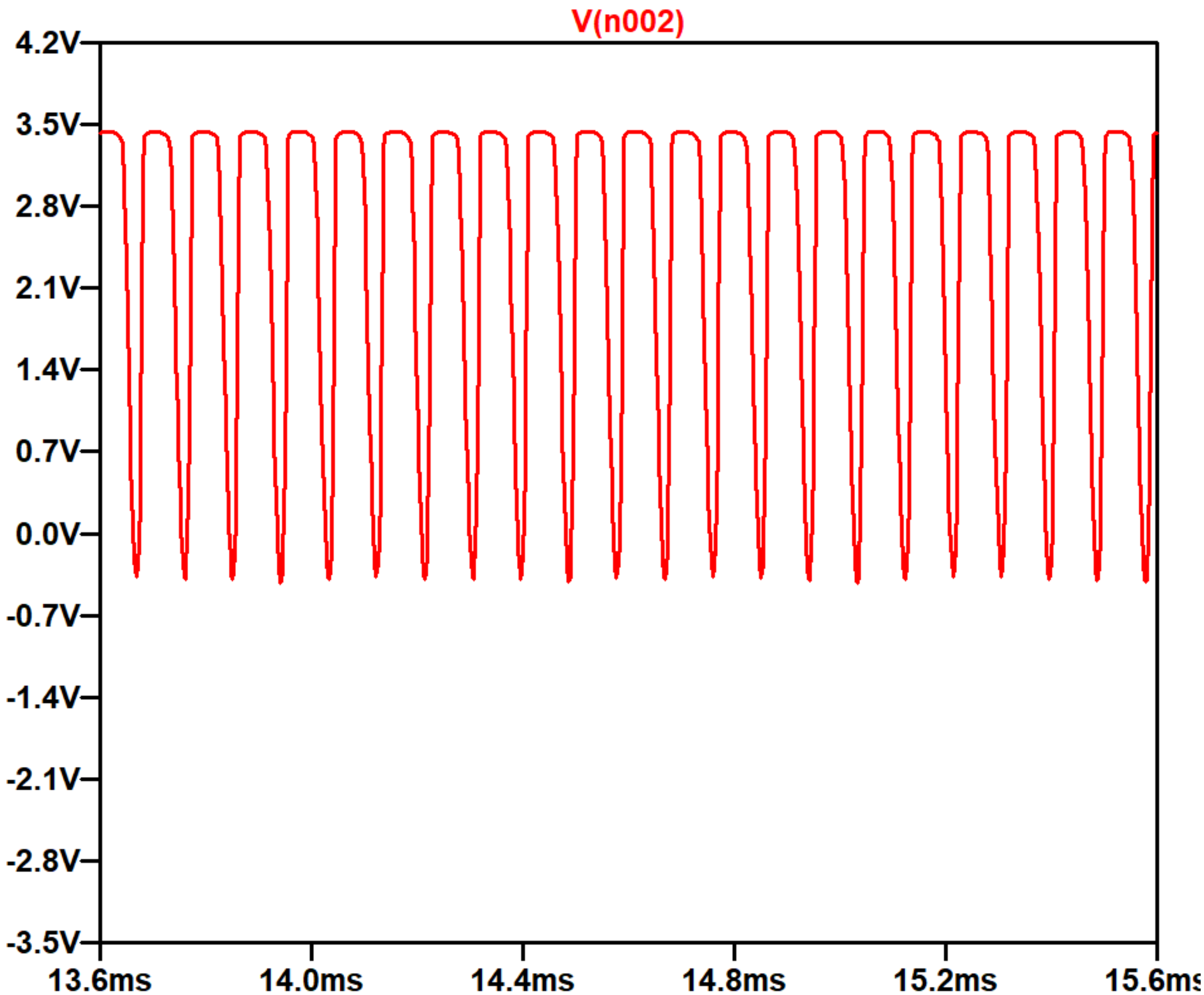
Output only for V_{LO}

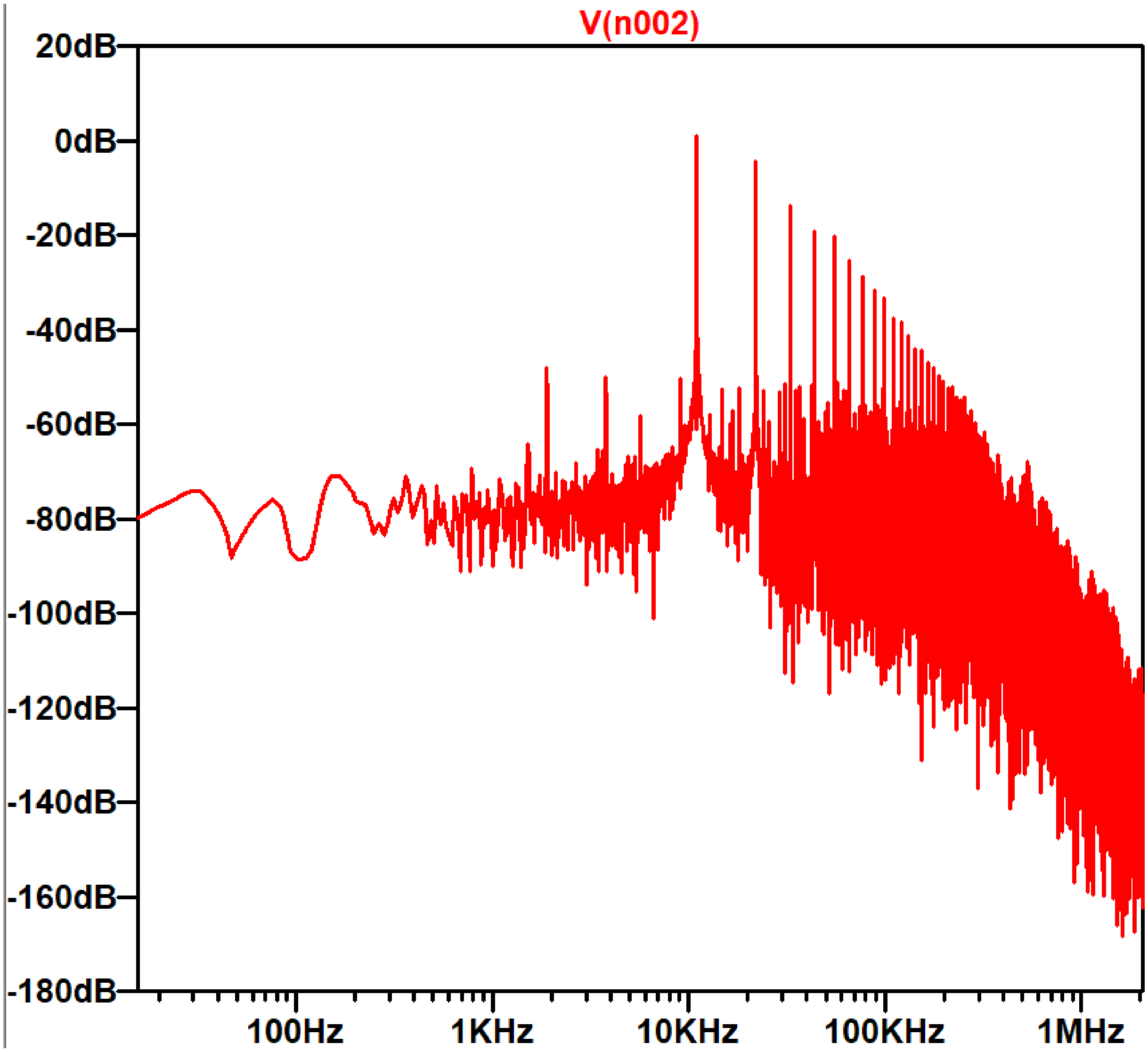




- The FFT has peak at 10KHz.

Output only for V_{RF}





- The FFT has peak at 11KHz.


thank you