Analog Lab (EE2401)
Experiment 5 : Voltage controlled oscillator

EE19BTECH11041,
Srijith Reddy Pakala
Department of Electrical Engineering
IIT Hyderabad

March 4, 2021

1 Aim

Understand the operation of a schmitt trigger based oscillator.

Design a variable frequency oscillator controlled by voltage.

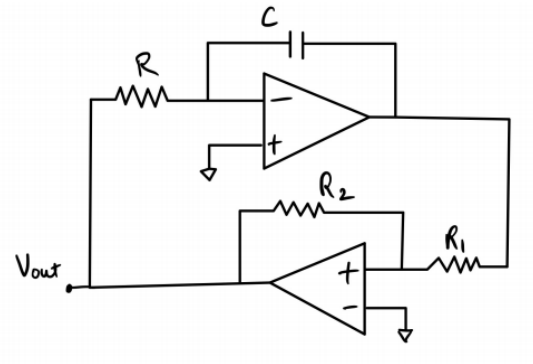
Schmitt trigger

A Schmitt trigger is a comparator circuit with hysteresis implemented by applying positive feedback to the noninverting input of a comparator or differential amplifier.

2 Problem statement

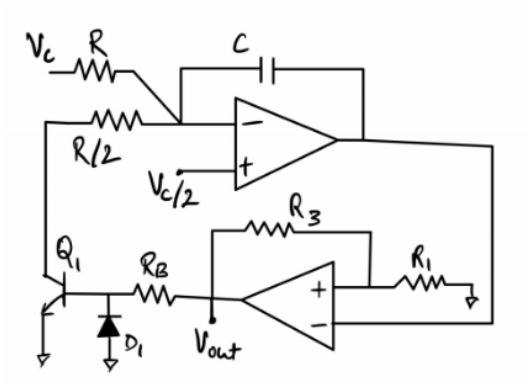
1. Design a schmitt trigger based oscillator with the following specifications:

. • Oscillation frequency: 10 kHz.
. • Hysterisis width for schmitt trigger: Around 20 % of the opamp peak-to-peak output swing.
. • LF347 opamp with +5V/-5V dual supply.



2. Below is a modified oscillator with a control voltage (V_C) input to vary the oscillation frequency. Here, V_C decides the rate of integration and hence controls the output frequency. Transistor Q_1 introduces an inversion, therefore the schmitt trigger is also inverting. RB is for controlling the base current of Q_1 and D_1 protects the transistor from breakdown during negative swing. :

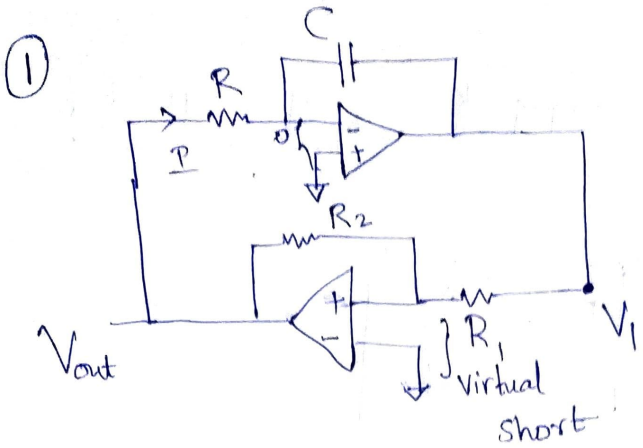
. • Analyze and calculate component values assuming Q_1 to act like an ideal switch.
. •frequency 10-15 kHz for V_C ranging from 4-6 V.
. • Generate $V_C/2$ from V_C using a voltage divider.
. • Q_1: 2N3904, D_1: 1N4148
. • Plot frequency vs V_C characteristics. Is it expected?



3. Change R or C to obtain new frequency range of 100-150 kHz for the same V_C range as above. Plot frequency vs V_C. Is it linear? Explain. In reality Q_1 doesn't act like an ideal switch. It has a saturation voltage of around 0.2 V. This can cause deviation in the expected duty cycle. Modify the circuit in Problem 2 to compensate this effect. You can assume a matched transistor is available.

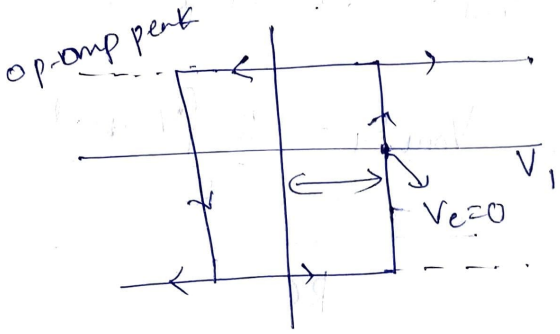
3 Analysis and simulation

Question1



Given hysterisis width is 20 % of peak to peak opamp.

$$\Rightarrow \quad V_e = \frac{V_{out} R_1 + V_1 R_2}{R_1 + R_2}.$$



At $V_e = 0$, $2V_1$ is hysterisis width

$$\Rightarrow \quad V_e = 0 = \frac{V_{out} R_1 + V_1 R_2}{R_1 + R_2}$$

$$\Rightarrow \quad V_1 = -\frac{V_{out} R_1}{R_2}$$

(1)

$$\Rightarrow V_1 = \frac{\text{op-amp peak}}{5} = \frac{\text{op-amp peak}\, R_1}{R_2}$$

$$\Rightarrow \boxed{R_1 = \frac{R_2}{5}}$$

$$V_1 = -\frac{\int V_{out}\, dt}{RC}$$

Let us suppose $V_e > 0$ at $t = 0$ and therefore $V_{out} = 3.5 = V_{peak} = V_p$.

then.

$$V_e = \frac{V_{out} R_1 - \frac{R_2 \int V_{out}\, dt}{RC}}{RC}$$

As the capacitor charges V_e will become zero at $t = t_1$

$$\Rightarrow t_1 = \frac{R_1 RC}{R_2}$$

(1) Now the actual cycle starts.

when $t > t_1$ $V_e < 0 \Rightarrow V_{out} = -V_p$

$$\Rightarrow V_e = \frac{-V_p R_1 + \frac{R_2 \int_{t_1}^{t_2} V_p dt}{RC} + \frac{R_2 \int_{0}^{t_1} -V_p dt}{RC}}{R_1 + R_2}$$

$$\Rightarrow V_e = 0 \Big|_{t=t_2}$$

$$\Rightarrow \frac{R_2 V_p (t_2 - t_1)}{RC} = 2 V_p R_1$$

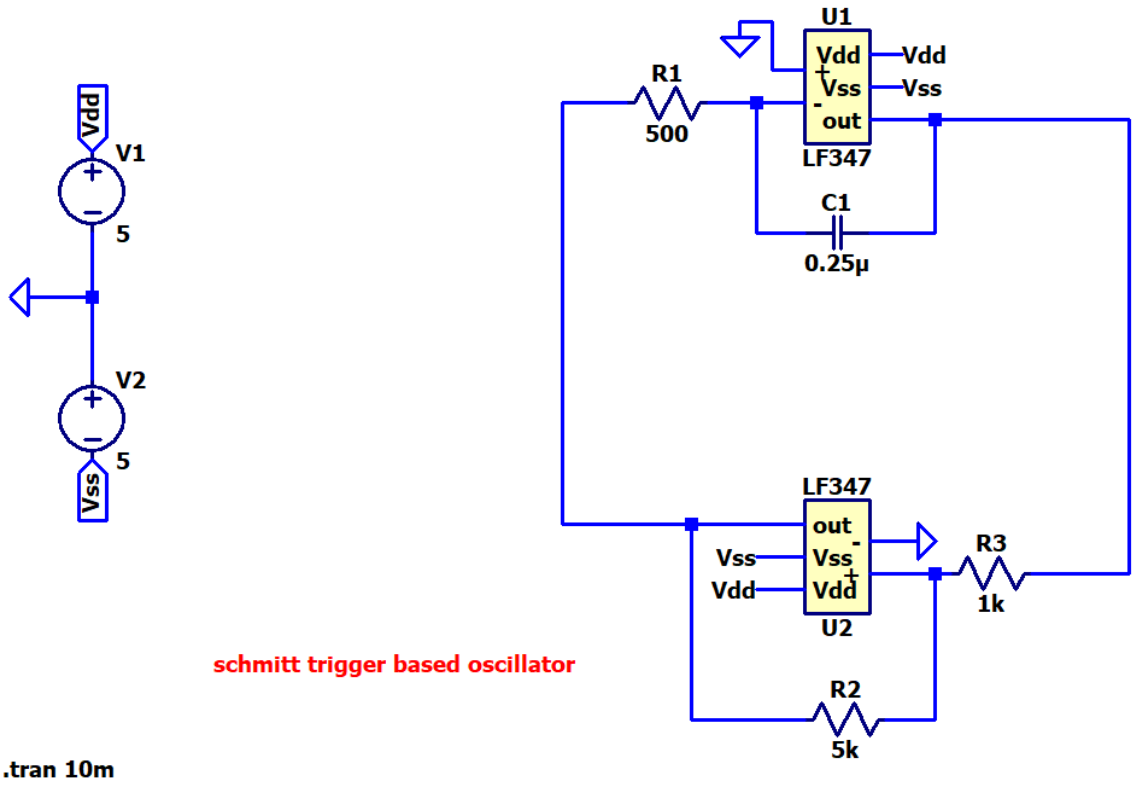
$$\Rightarrow \Delta t = t_2 - t_1 = \frac{2RCR_1}{R_2}$$

Here Δt is half the Time period.

$$\Rightarrow T = 2\Delta t = \frac{4RCR_1}{R_2} = \frac{4RC}{5}$$

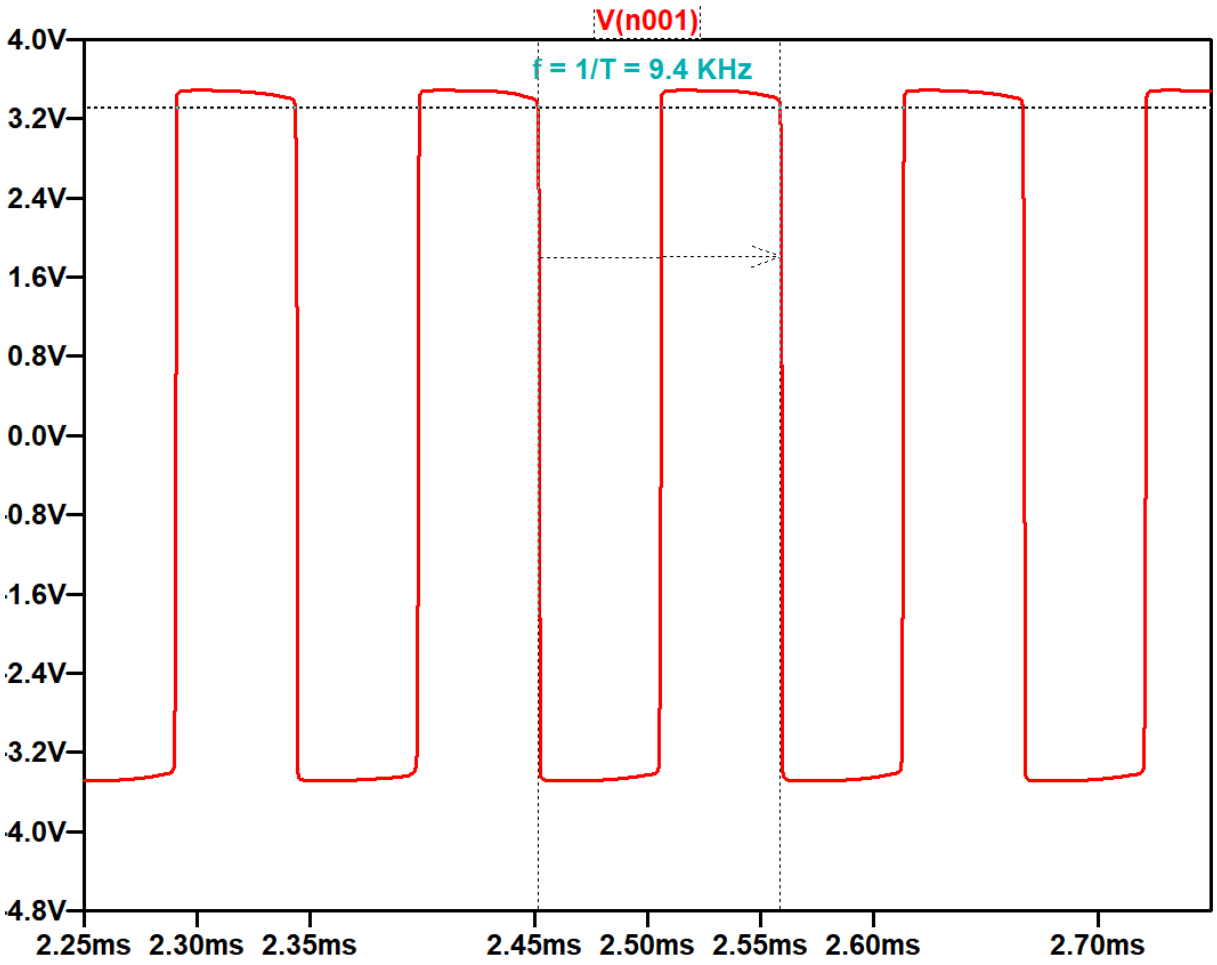
$$\boxed{f = \frac{5}{4RC}}$$

Schematic



Circuit schematic

Output



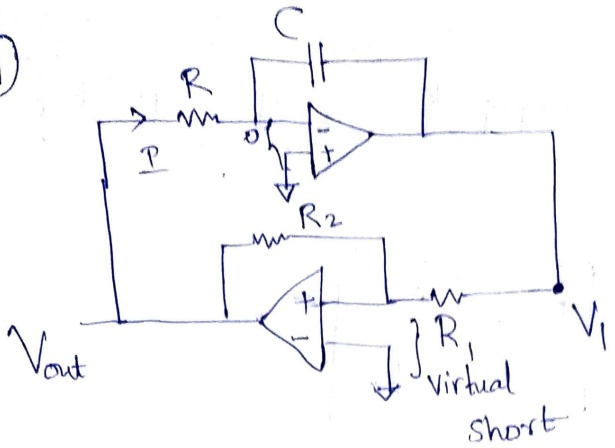
V_{out}

• As we can see the frequency is 9.4KHz which is deviated from the expected value 10KHz and duty cycle here is 50.0157%.

• The may be accounted by the non ideal characteristics of opamp we used .

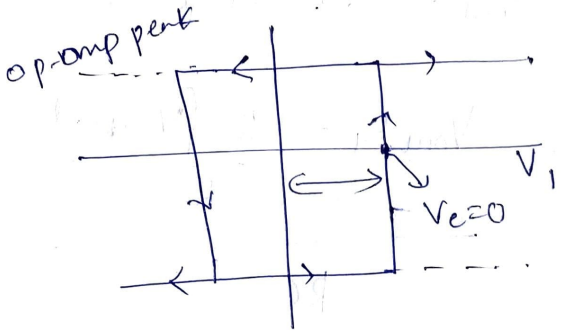
Question2

(1)



Given hysterisis width is 20 % of peak to peak opamp.

$$\Rightarrow \quad V_e = \frac{V_{out} R_1 + V_1 R_2}{R_1 + R_2}.$$



At $V_e = 0$, $2V_1$ is hysterisis width

$$\Rightarrow \quad V_e = 0 = \frac{V_{out} R_1 + V_1 R_2}{R_1 + R_2}$$

$$\Rightarrow \quad V_1 = -\frac{V_{out} R_1}{R_2}$$

(2)

$$V_e = \frac{V_{out} R_1}{R_1 + R_3} - V_1$$

Similarly using 20% peak hysteresis

$$\frac{R_1}{R_1 + R_3} = \frac{1}{5}$$

$$\Rightarrow \quad R_3 = 4R_1$$

$$V_1 = \frac{V_c}{2} - \int \frac{V_c}{2RC}\, dt \quad , \quad V_e > 0 \quad , \quad V_{out} > 0$$

$$V_1 = \frac{V_c}{2} + \int \frac{V_c}{2RC}\, dt \quad , \quad V_e < 0 \quad , \quad V_{out} < 0$$

Now let's say at $t=0$ $V_e > 0$ and cap is uncharged. $\Rightarrow V_{out} = V_p$

$$V_e = \frac{V_{out} R_1}{R_1 + R_3} + \int_0^t \frac{V_c}{2RC}\, dt - \frac{V_c}{2}$$

As cap charges $V_e \downarrow$ and at $t = t_1$, $V_e = 0$

$$\Rightarrow \quad 0 = \frac{V_c}{2}\left(\frac{t_1}{RC} - 1\right) + \frac{V_{out} R_1}{R_1 + R_3}$$

(2)

$$t_1 = RC - \left(RC \frac{2 V_{out} R_1}{V_c (R_1 + R_3)} \right)$$

Now. At $t > t_1$, $V_e < 0 \Rightarrow V_{out} = -V_p$

Now the actual cycles will start.

let t_2 be tat which $V_e = 0$ when $V_{out} = -V_p$

$$\Rightarrow V_e = \frac{-V_p R_1}{R_1 + R_3} - \int_{t_1}^{t_2} \frac{V_c}{2RC} dt$$

$$\frac{-V_p R_1}{R_1 + R_3}$$

$$\Rightarrow V_e|_{t=t_2} = 0$$

$$\Rightarrow (t_2 - t_1) V_c = \frac{4RC V_p R_1}{R_1 + R_3}$$

$$\Rightarrow \Delta t = \frac{T}{2} = \frac{4RC V_p R_1}{V_c (R_1 + R_3)}$$

$$\boxed{T = \frac{8RC R_1}{(R_1 + R_3)} \frac{V_p}{V_c}} = \frac{8RC.V_p}{5 V_c}$$

(2) $f = \frac{5V_c}{8RCV_p}$

Now from simulation $V_p \approx 3.5V$

we need $f = 10KHz\big|_{V_c=4V}$

$$\Rightarrow \frac{5\times 4}{8RC(3.5)} = 10KHz$$

$$\Rightarrow R = 1K,\ C = 35.714nF$$

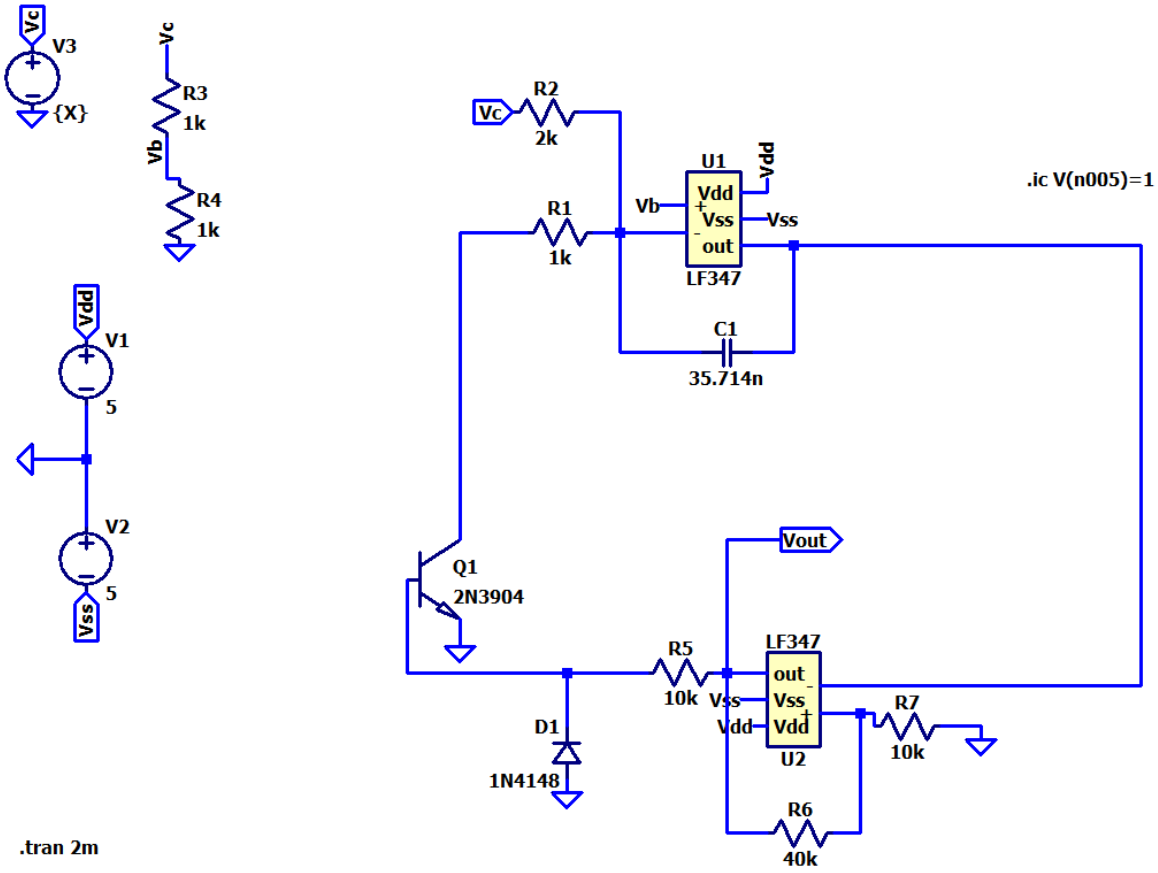
Now coming to R_B. R_B controlls I_B at Q_1 and maintain D_1 from breakdown.

R_B should be higher such that D_1 is safe and lower enough such that Q is in saturation i.e $I_B > \frac{I_C}{\beta}$

$$\frac{V_{out}-0.7}{R_B} > \frac{V_c}{2R\beta}$$, Typically $R_B < 100K$

we choose $R_B = 10K$.

Schematic



Circuit schematic

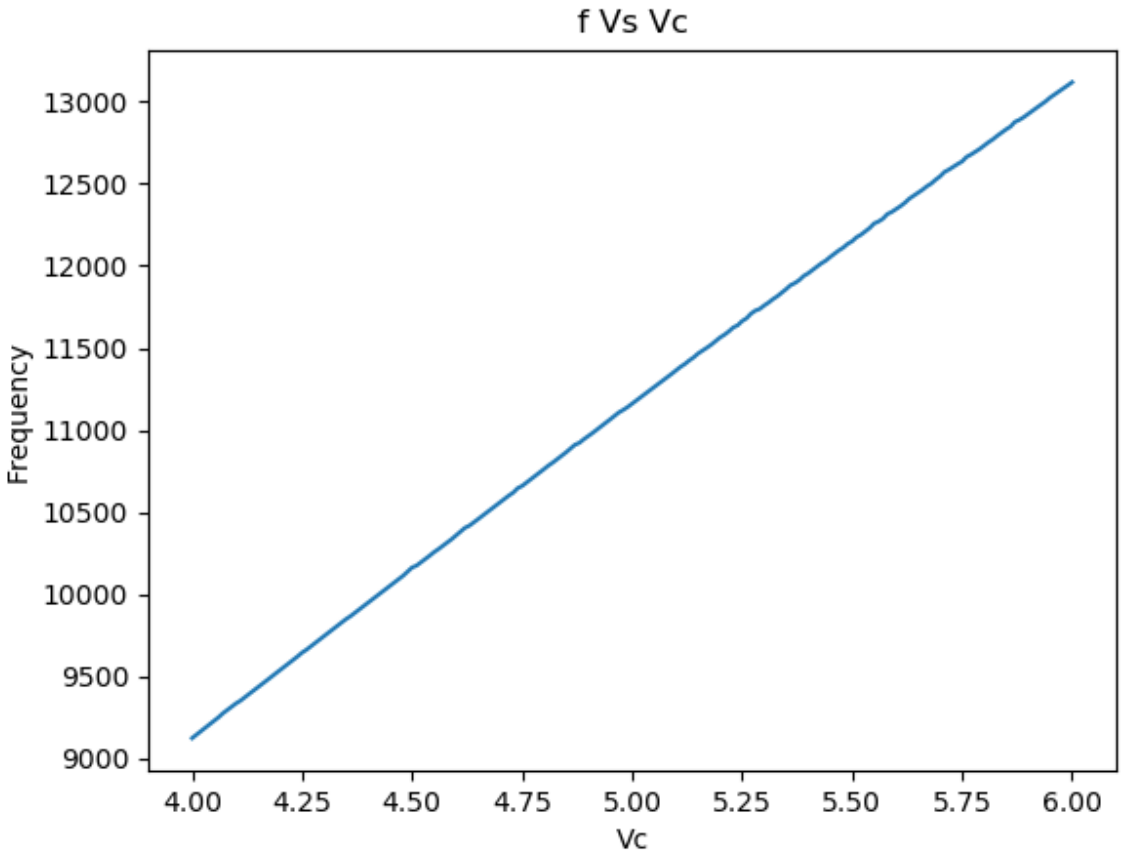
```
.step param X 4 6 0.01

.meas tran T3 find time when V(vout)=0 fall 10
.meas tran T1 find time when V(vout)=0 rise 10
.meas tran T2 find time when V(vout)=0 rise 11
.meas tran  Frequency param 1/(T2-T1)

.meas tran duty PARAM (T3-T1)/(T2-T1)
```

- To find frequency as V_C varies we have used above statements and also for duty cycle.

f as V_C varies



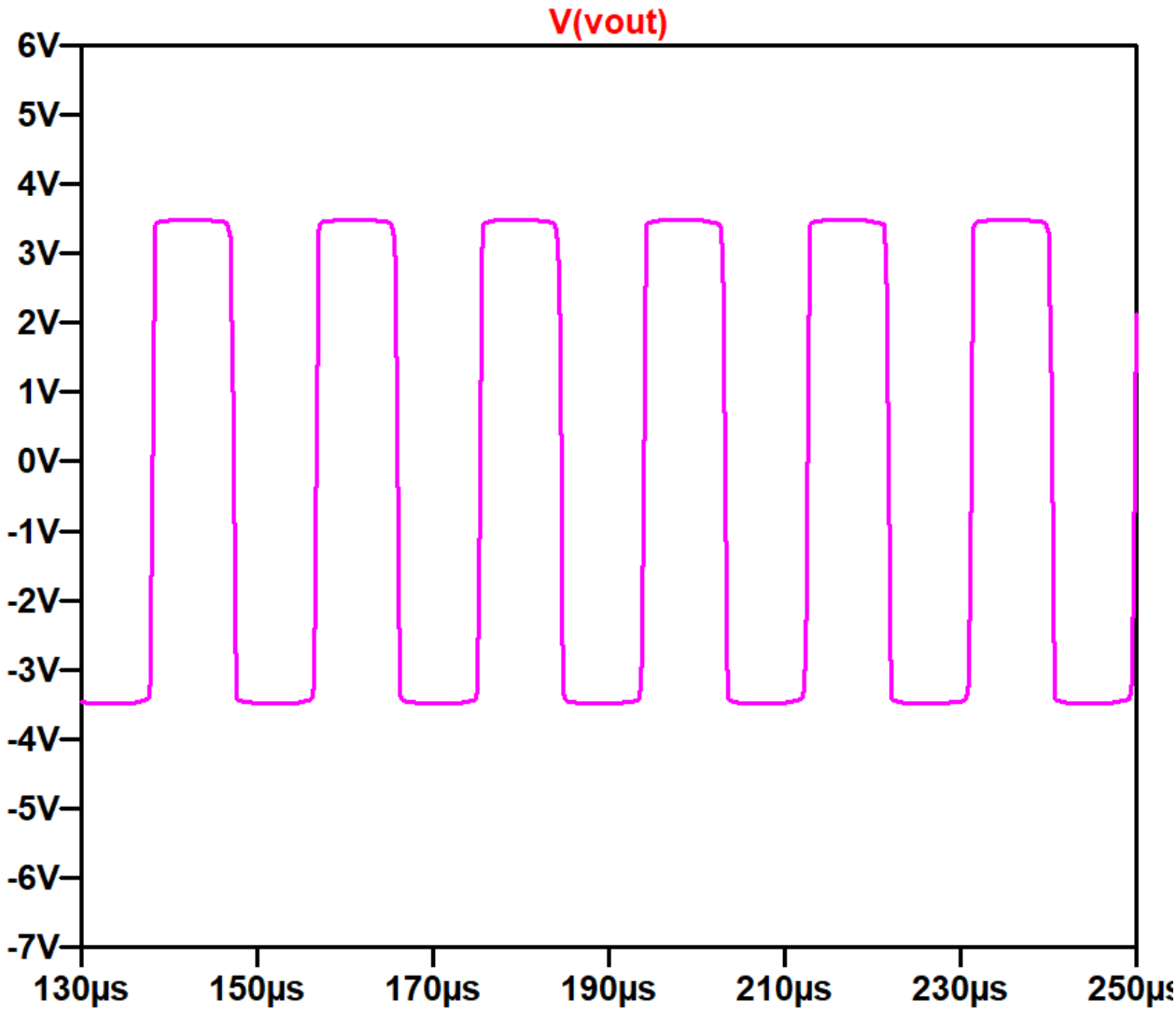
f **Vs** V_C

• We can see that the frequency is increasing linearly w.r.t to V_C .

• But similar from the first question the frequency here is also deviated from the expected values.

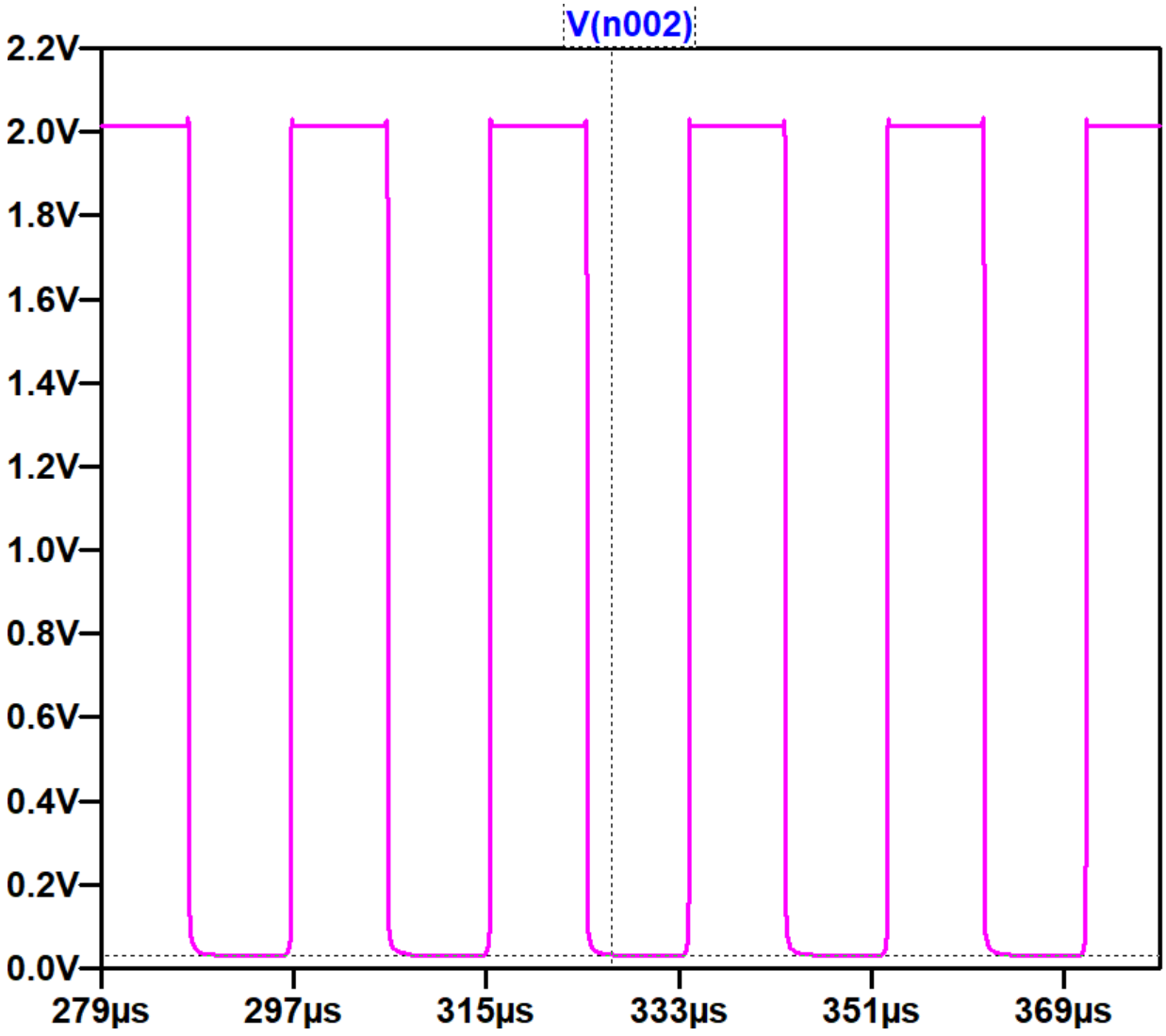
• The duty cycle here is 50.3009%.

V_{out} **at** V_C**=5V**



V_{out} **Vs time(ms)**

Voltage at collector of Q_1

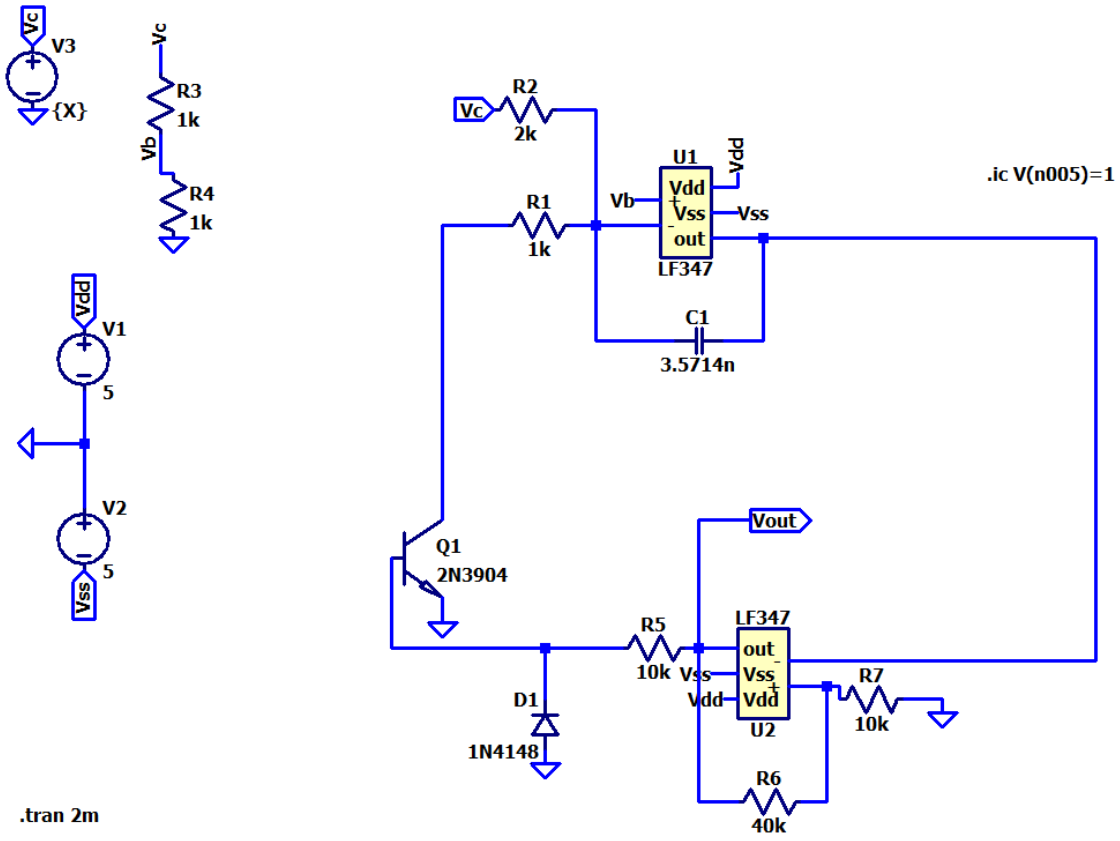


$V_{Collector}$ **Vs time(ms)**

• From the above plot the saturation voltage is 30mV which is quite low and good for the circuit.

Question3

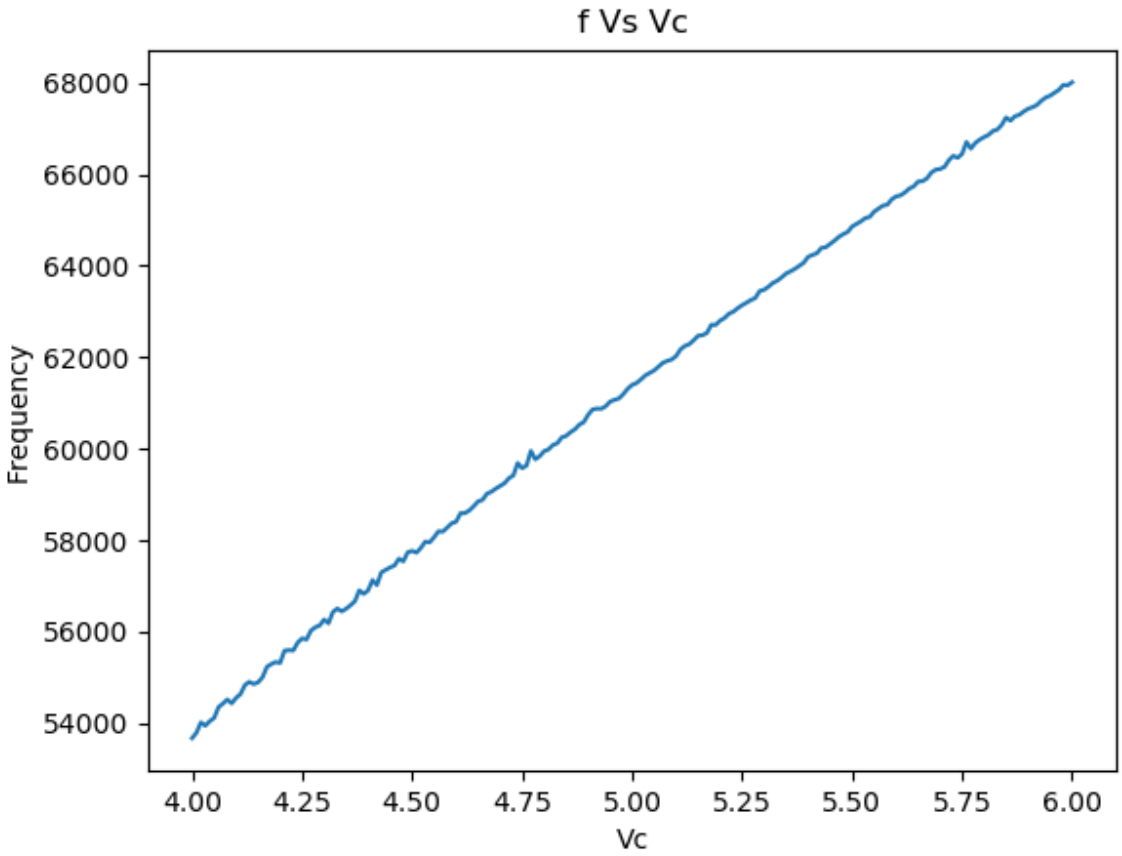
Schematic



Circuit schematic

- We have changed R and C such that frequency range is 100KHz to 150KHz.

f as V_C varies



f **Vs** V_C

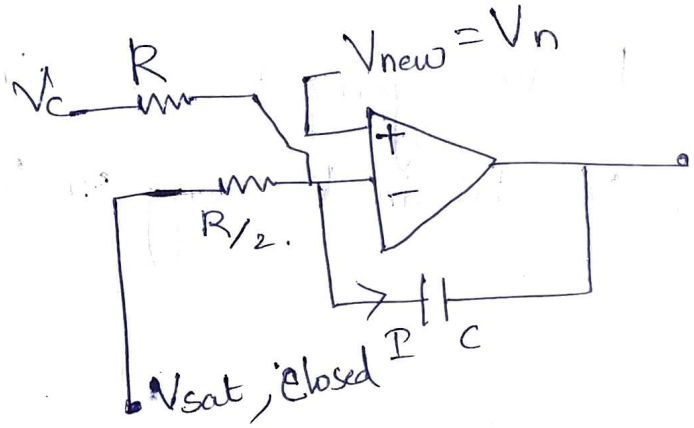
- We can see that the frequency is increasing w.r.t to V_C but non-linear.

- The frequencies observed is very much deviated from the expected value,the reason is that opamp output cannot change faster than slew rate.

- The duty cycle here is 0.511321% at V_C=6V.

(3) In reality Q_1 is not an ideal Switch so, to we need to compensate it's saturation effect.

we can change non-inverting input of integrator such that current through capacitor has same magnitude.



closed

$$-I_p = \frac{V_c - V_n}{R} - \frac{(V_n - V_{sat})}{R/2}$$

open

$$+I_p = \frac{V_c - V_n}{R}$$

(3)

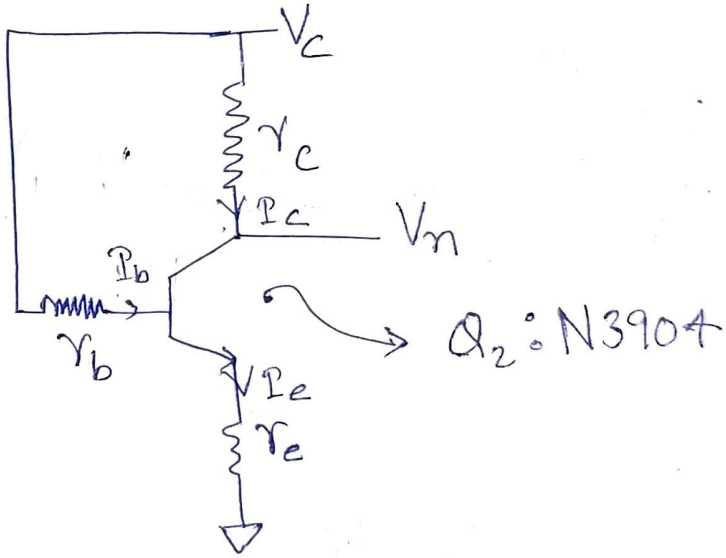
$$\Rightarrow \quad \frac{V_C - V_n}{R} = \frac{2(V_n - V_{sat})}{R} - \left(\frac{V_C - V_n}{R}\right)$$

$$\Rightarrow \quad V_C - V_n = V_n - V_{sat}$$

$$\Rightarrow \quad \boxed{V_n = \frac{V_C}{2} + \frac{V_{sat}}{2}}$$

Now we need to generate a circuit such that V_n is obtained using matched transistor.

Method 1:



(3) Now let's write equations.

$$V_{CE} = V_C - I_C r_c - I_e r_e \quad -(1)$$

$$(V_c - I_b r_b - 0.7) = I_e r_e \quad -(2)$$

$$I_b = \frac{I_c}{\beta} \quad -(3)$$

$$I_e = (\beta+1) I_b = I_b + I_c \quad -(4)$$

$$\Rightarrow V_n = \frac{\beta r_c V_{sat} + (\beta+1) r_e V_c}{\beta r_c + (\beta+1) r_e}$$

By comparing $V_n = \frac{V_c}{2} + \frac{V_{sat}}{2}$

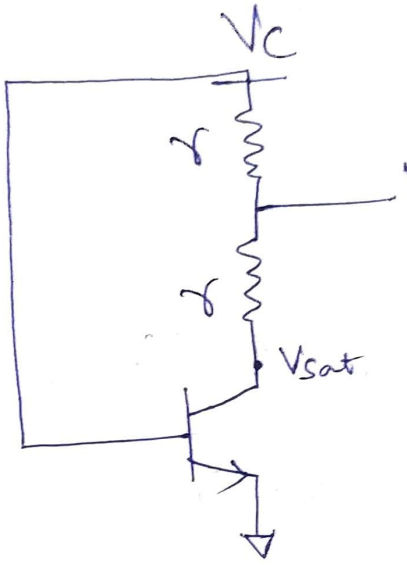
$$\beta r_c = (\beta+1) r_e$$

Assuming $\beta >> 1$

$$\Rightarrow r_c \approx r_e, \quad r_B \approx \beta r_c$$

(3) Method 2

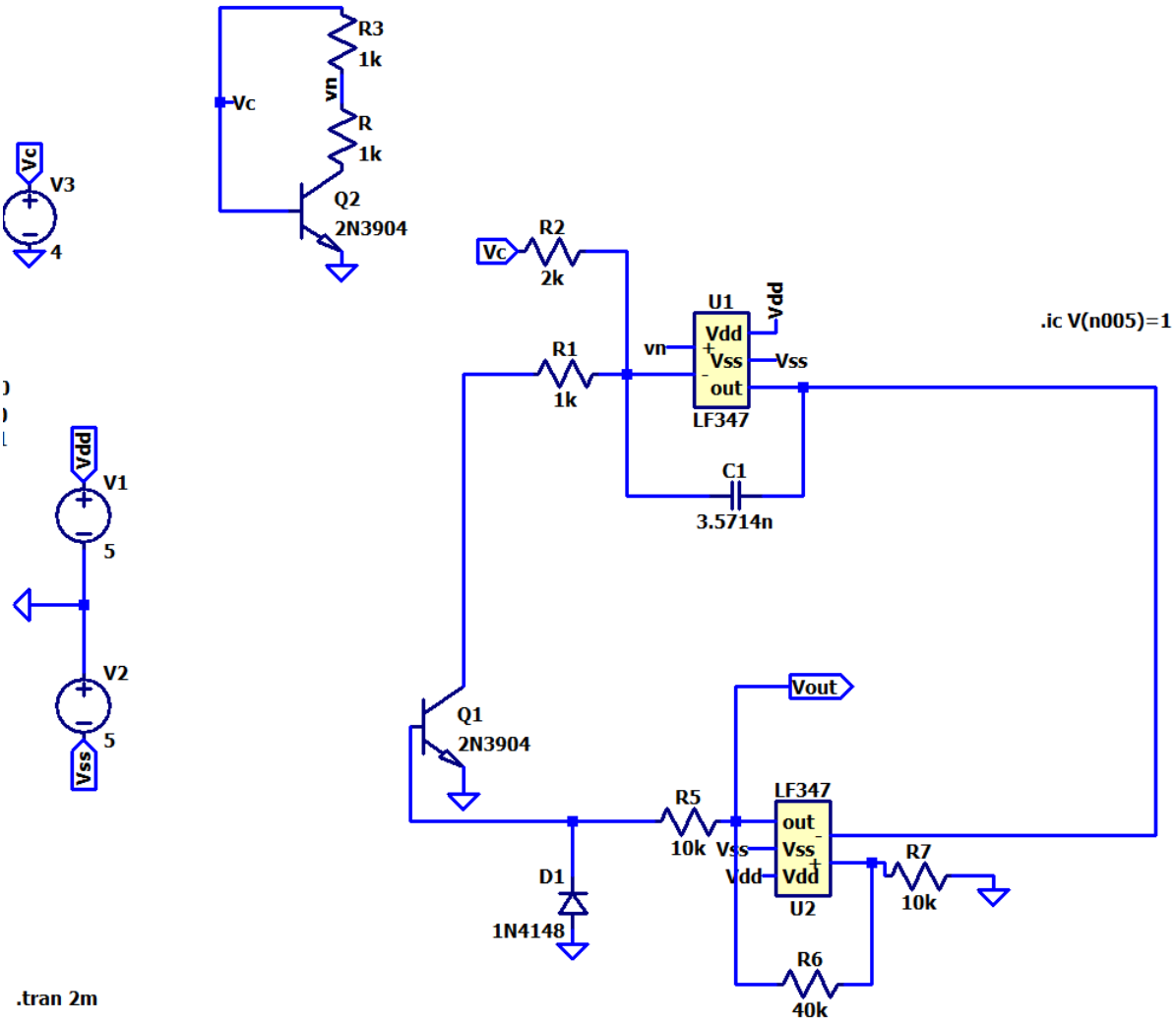
Since we donot know we can use this method.



$$V_n = \frac{V_c}{2} + \frac{V_{sat}}{2}$$

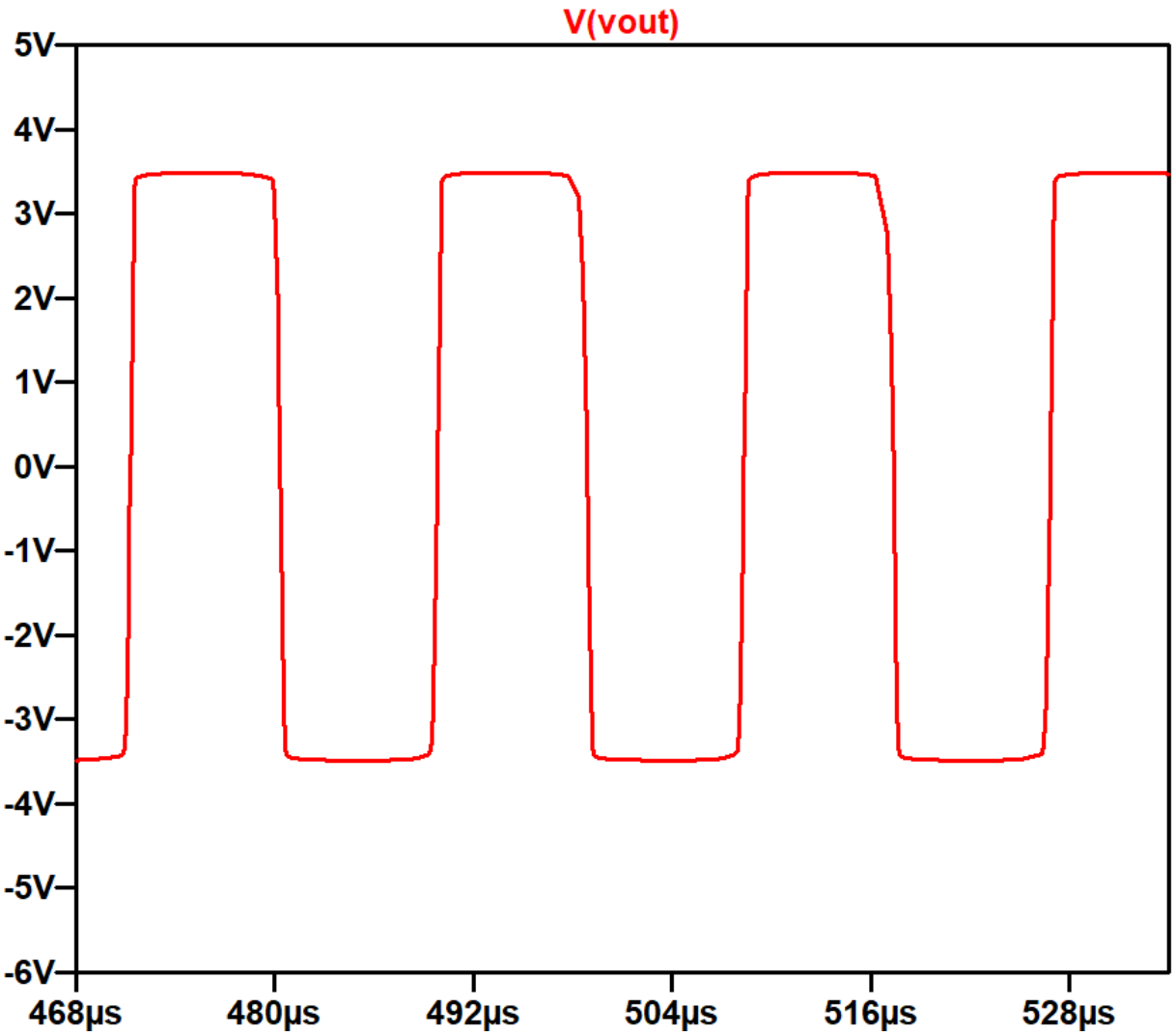
we can use r in the range of 1K.

Schematic



Circuit schematic with compensation

V_{out} **at** V_C**=4V**



V_{out} **Vs time(ms)**

• Duty cycle observed here is 0.513224%.

• There is not much of a difference in duty cycle here because of low saturation voltage i.e 30mV.It could be helpful if our saturation would have high.


thank
you