Analog Lab (EE2401)
Experiment 4 : Charge pump

EE19BTECH11041,
Srijith Reddy Pakala
Department of Electrical Engineering
IIT Hyderabad

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1 Aim

Design a negative voltage generator from a positive supply.

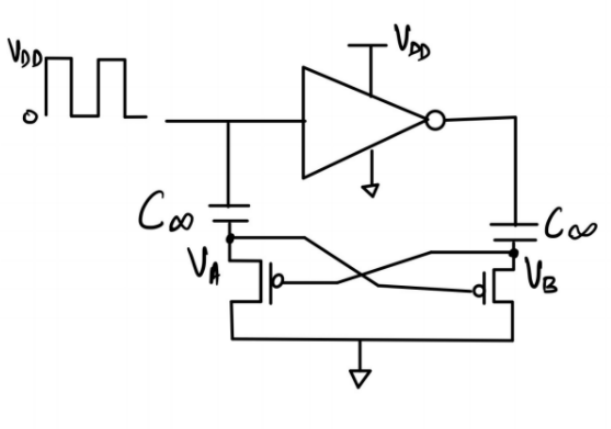
Design a circuit to get a higher voltage than the available supply

Charge pump

A charge pump is a kind of DC-to-DC converter that uses capacitors for energetic charge storage to raise or lower voltage. Charge-pump circuits are capable of high efficiencies, sometimes as high as 90–95%, while being electrically simple circuits.

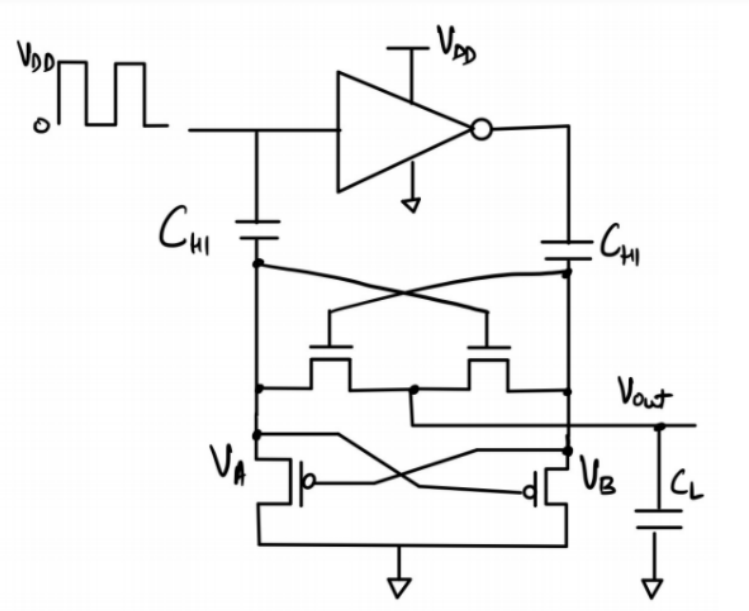
2 Problem statement

1. Determine the voltage waveforms of V_A and V_B in steady state in the figure below. Analyze by hand taking into account region of operation for the transistors.



2. NMOS transistors are added to multiplex V_A and V_B resulting in V_{out} as shown in figure below. Use CD4069 ICs to implement this circuit. Use the following values:

- Clock frequency: 10 kHz.
- Supply voltage: 5 V.
- C_{HI} : 10 nF.



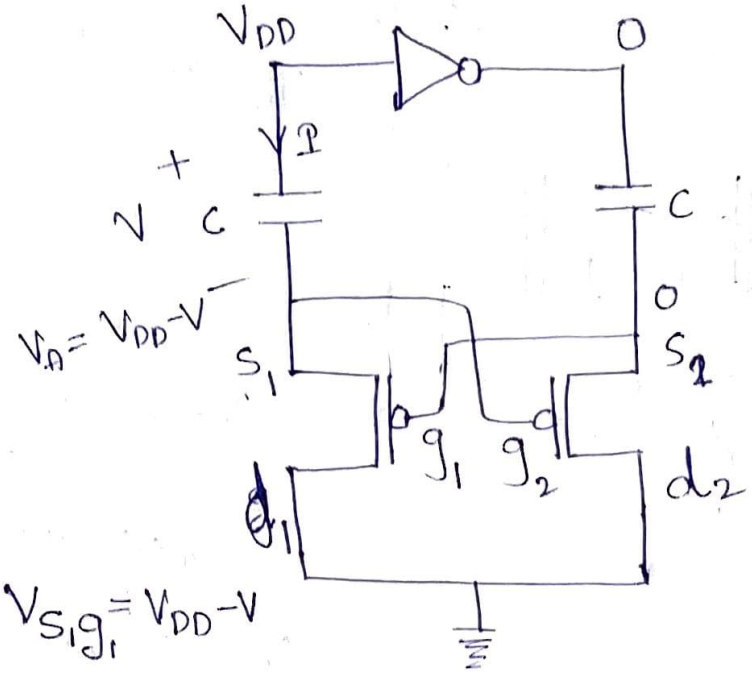
3. Design and simulate a circuit that gives positive output of close to twice the supply voltage w.r.t. ground.

3 Analysis and simulation

Question 1

At $t=0$ Both capacitors will be unchanged and have no voltage drop across them.

First half cycle : $(V_{in} = V_{DD})$



$V_{S_1 g_1} = V_{DD} - V$

$V_{S_1 d_1} = V_{DD} - V$.

$V_{S_1 d_1} > V_{S_1 g_1} - |V_T|$

PMOS$_1$

Saturation.

$V_{S_2 g_2} = -(V_{DD} - V)$

$V_{S_2 d_2} = 0$

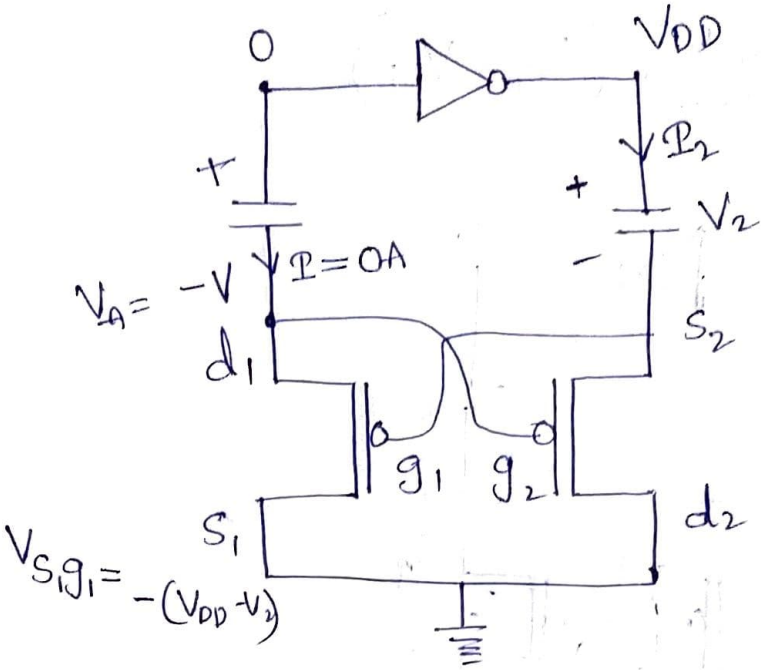
$V_{S_2 g_2} < |V_T|$

PMOS$_2$

cutoff.

The left capacitor will charge to some voltage 'V' in first half cycle. and right capacitor will stay unchanged.

Second half cycle ($V_{in}=0$)



PMOS$_1$

Cutoff

PMOS$_2$

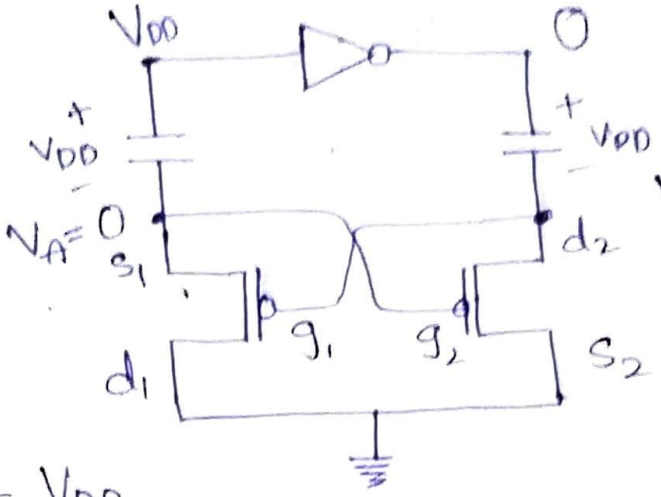
Linear.

Since Pmos$_1$ is in cutoff left cap will stay at same voltage and right capacitor will Charge to some 'V_2' at end of second half cycle.

* After some cycles Both capacitors will eventually charge to V_{DD}.

N^{th} half cycle after full capacitor charging:

($V_{in} = V_{DD}$) (steady state)



$V_{S_1 g_1} = V_{DD}$

$V_{S_1 d_1} = 0$

$I = 0$

PMOS$_1$

Cutoff

$V_{S_2 g_2} = 0$

$V_{S_2 d_2} = V_{DD}$

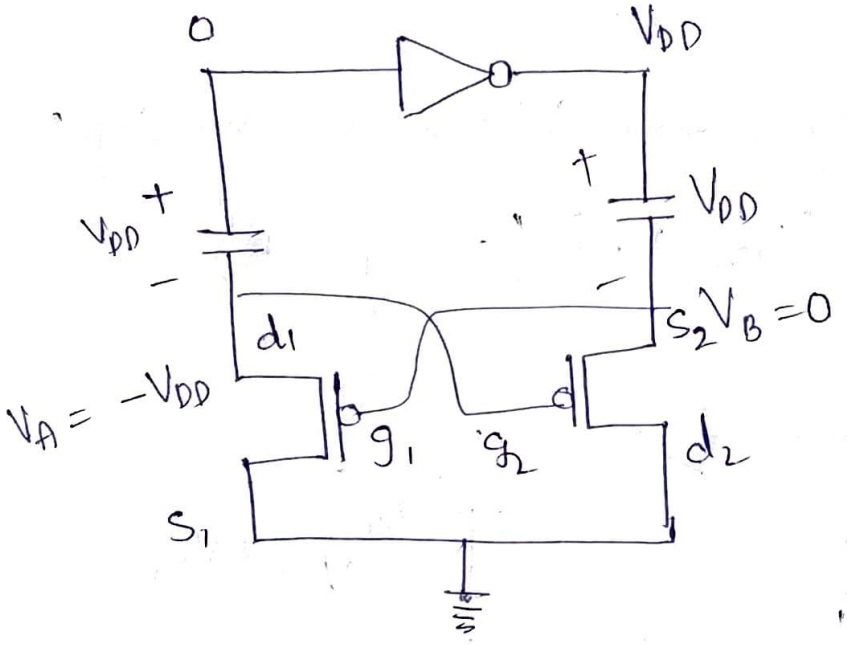
$I_2 = 0$

PMOS$_2$

cutoff

Therefore both mosfet will be in cutoff and capacitors will stay at V_{DD} voltage across them. i.e, there is no charging or discharging.

$(N+1)^{th}$ half cycle ($V_{in}=0$) (steady state)



$V_{s_1 g_1} = 0$

$V_{s_1 d_1} = V_{DD}$

$I = 0$

PMOS$_1$

cutoff

$V_{s_2 g_2} = V_{DD}$

$V_{s_2 d_2} = 0$

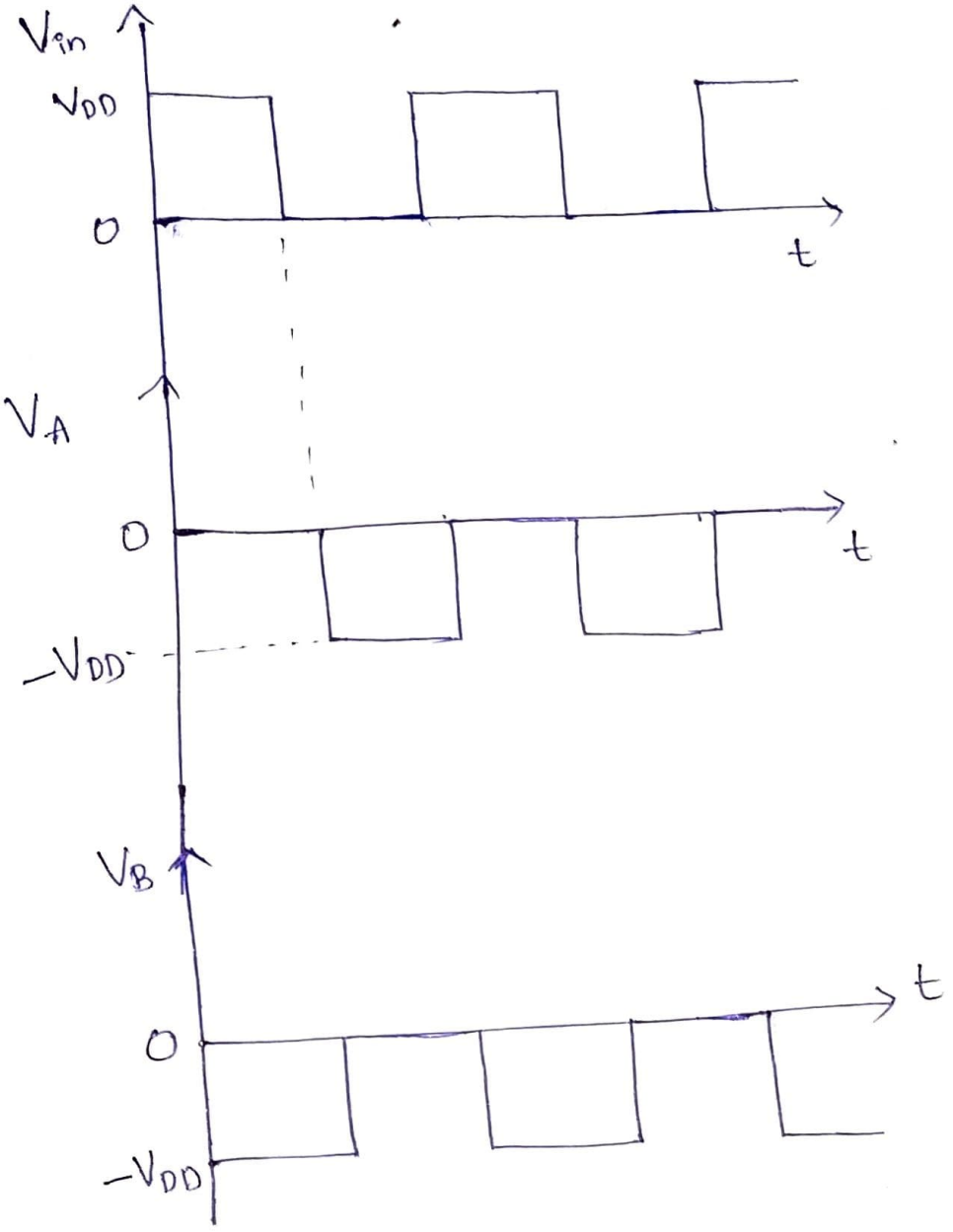
$I_2 = 0$

PMOS$_2$

cutoff

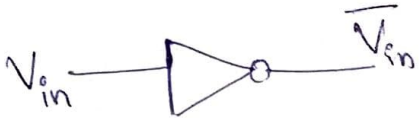
Similarly as in previous cycle. Both mosfet are in cutoff. and there is no charging or discharging.

At Steady state.:



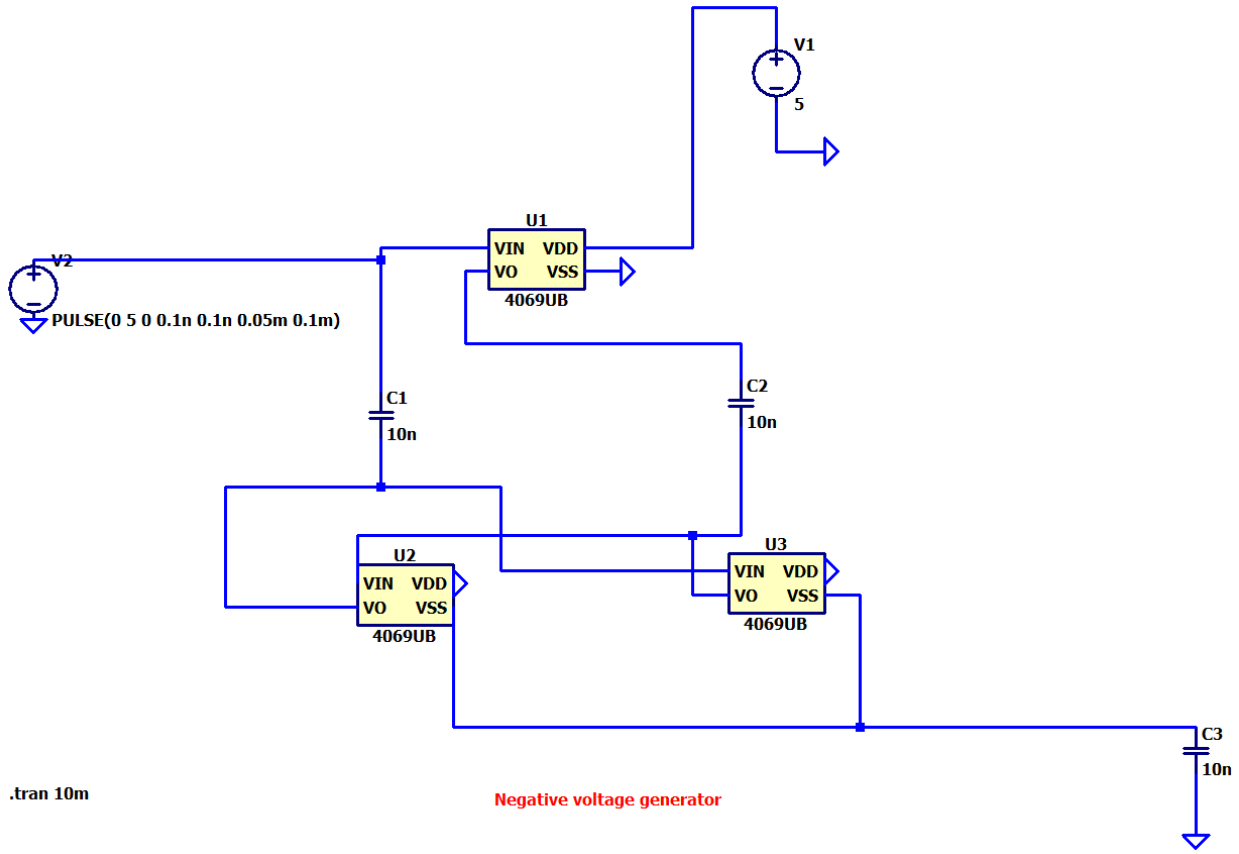
We can say at steady state.

$$V_A = V_{in} - V_{DD} \quad , \quad V_B = \overline{V_{in}} - V_{DD}$$



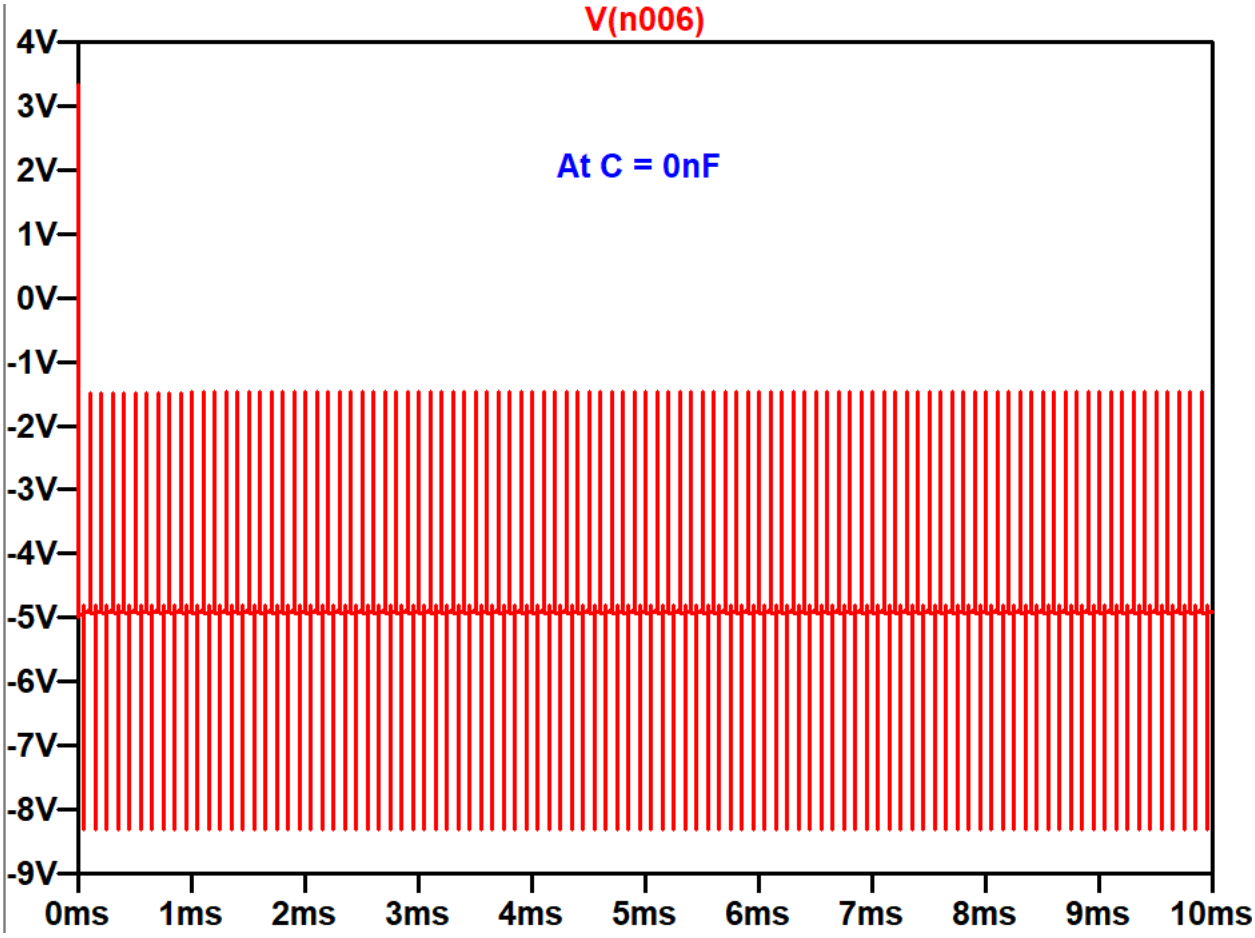
Question 2

Schematic



Circuit schematic

Output at C = 0nF



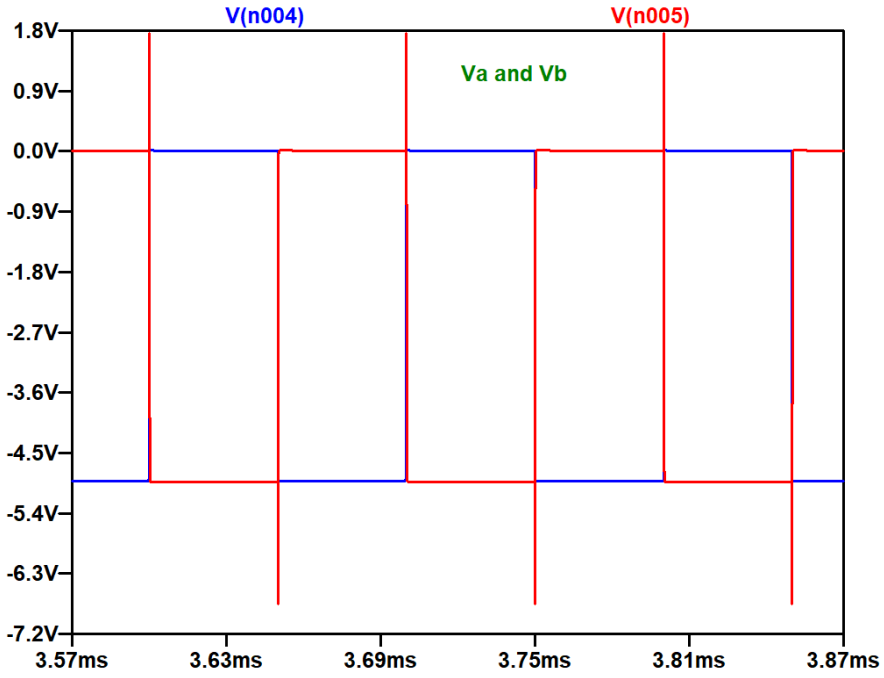
V_{out} **at C = 0F**

• We can see that the output is -5V with some spikes in transition period.

• From the previous analysis we just added 2 Nmoses to earlier circuit which just act as switches i.e when V_{in} is 5V left nmos will be cutoff therefor making right nmos source and drain as same voltage to have no current,similarly when V_{in} is 0V left nmos acts as short and right nmos acts as open, therefore maintaing constant voltage -5V.

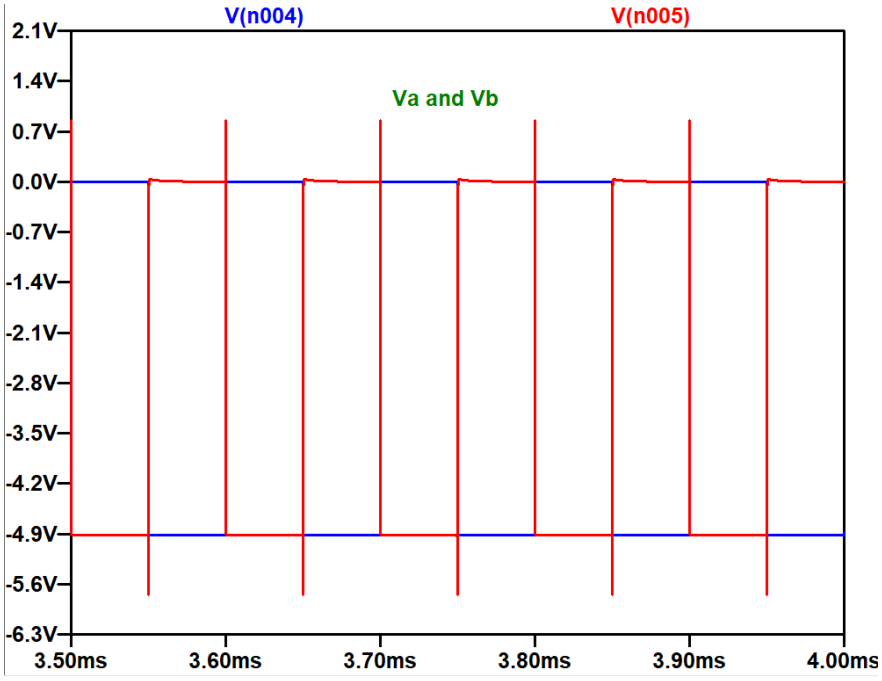
• Here capacitance 0 F signifies that it's essentially open circuit at capacitor. and therefore causes spikes in the output at transition of input from 0V to 5V and 5V to 0V.

V_a and V_b at C = 0nF



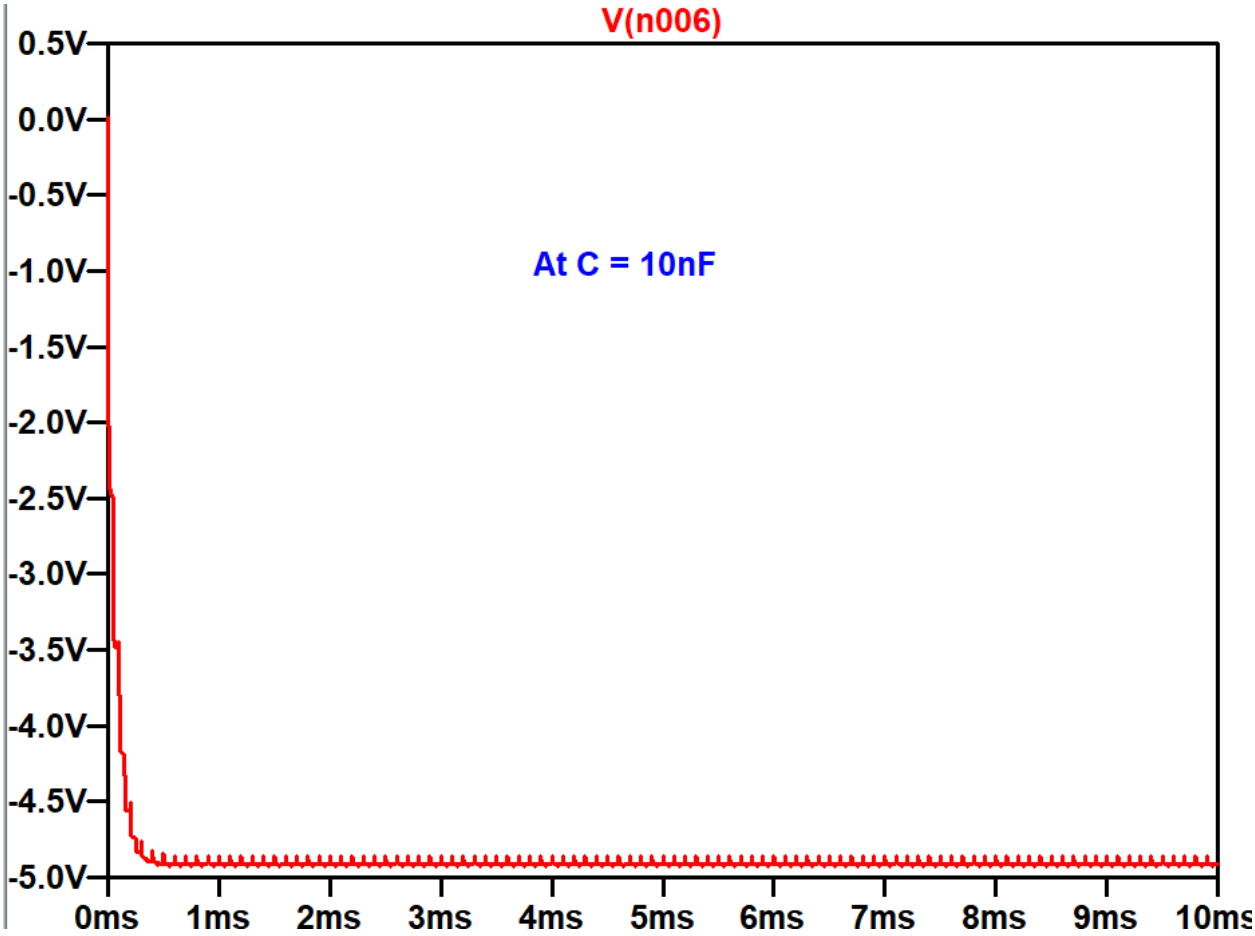
V_a and V_b at C = 0nF

V_a and V_b at C = 10nF



V_a and V_b at C = 10nF

Output at C = 10nF

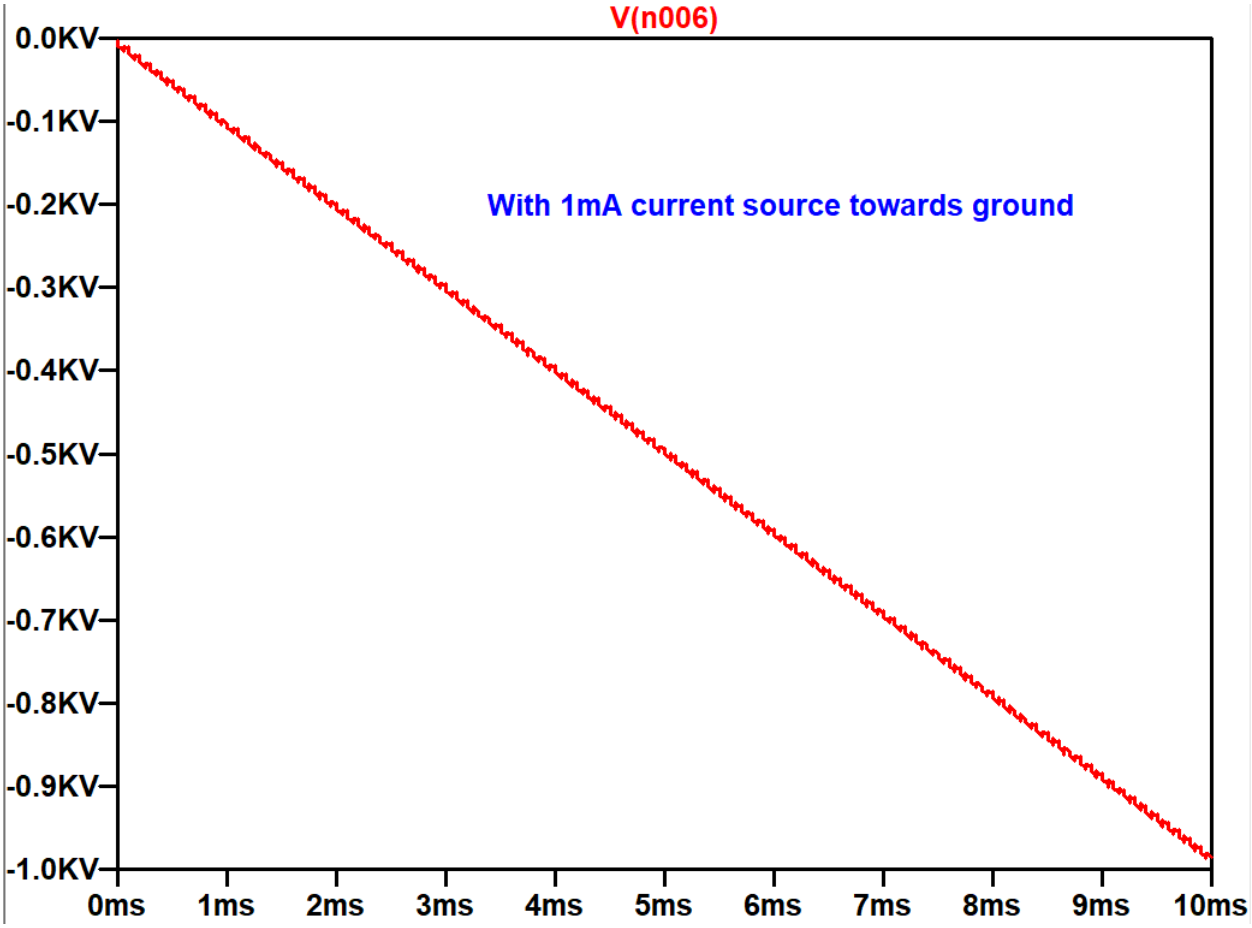


V_{out} **at C = 10nF**

• We can see that the output is -5V with very low variation.

• Here capacitance 10nF is the reason for removing spikes when compared to at C=0 because of charging of capacitor.

Output with 1mA current source

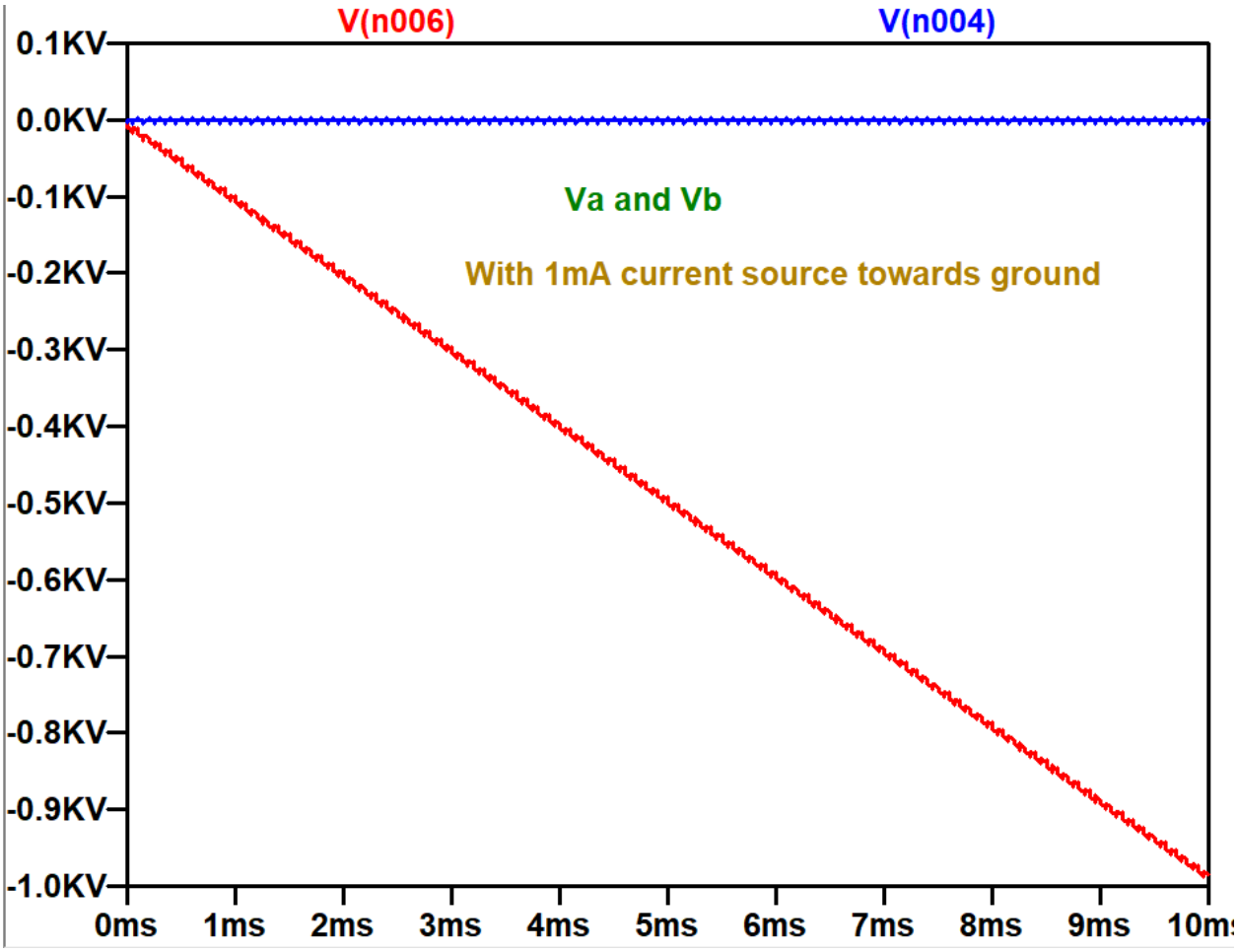


V_{out} at 1mA current source

• We can see that the output decreases as the time increases in essentially a straight line manner .

• This behaviour can be attributed to charging of one the capacitor due to current source as time progresses. and the other capacitor stays at same voltage because one of the nmos will always be in cutoff.

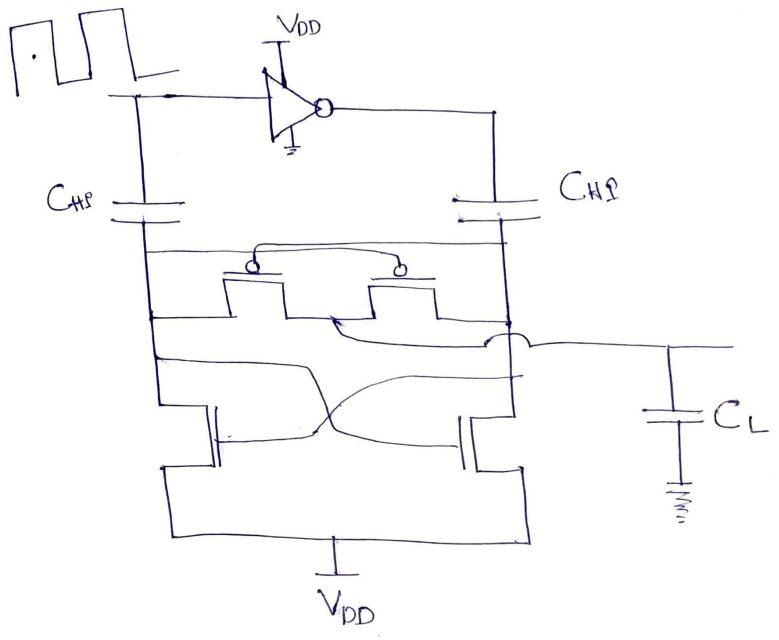
V_a and V_b with 1mA current source.



V_a and V_b with 1mA current source.

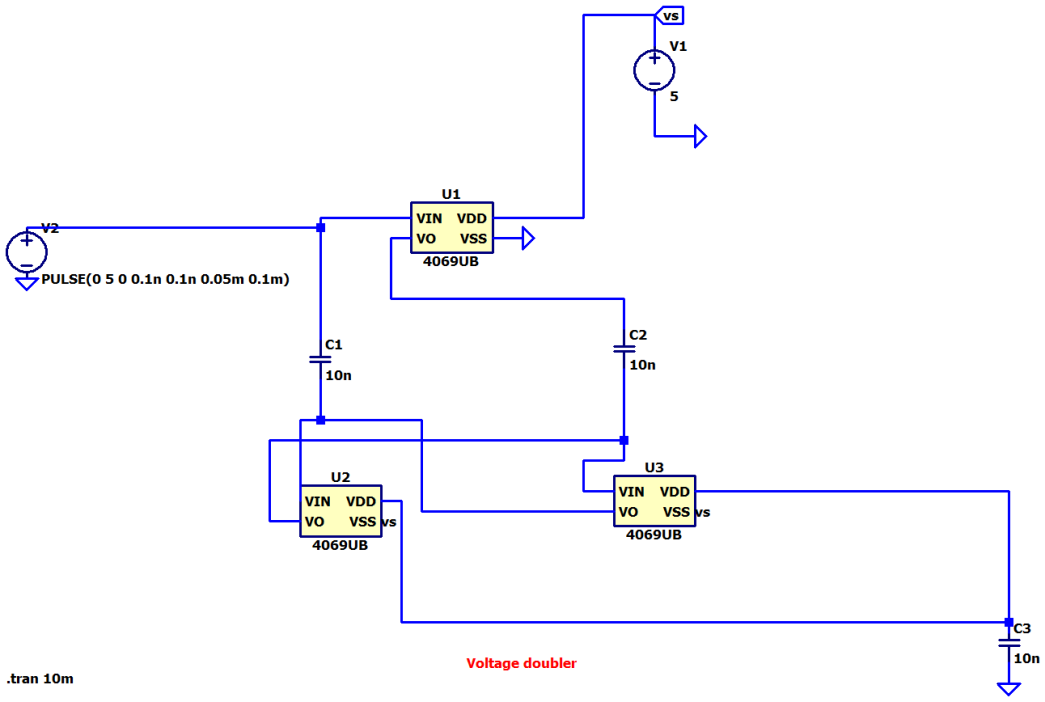
Question 3

Design



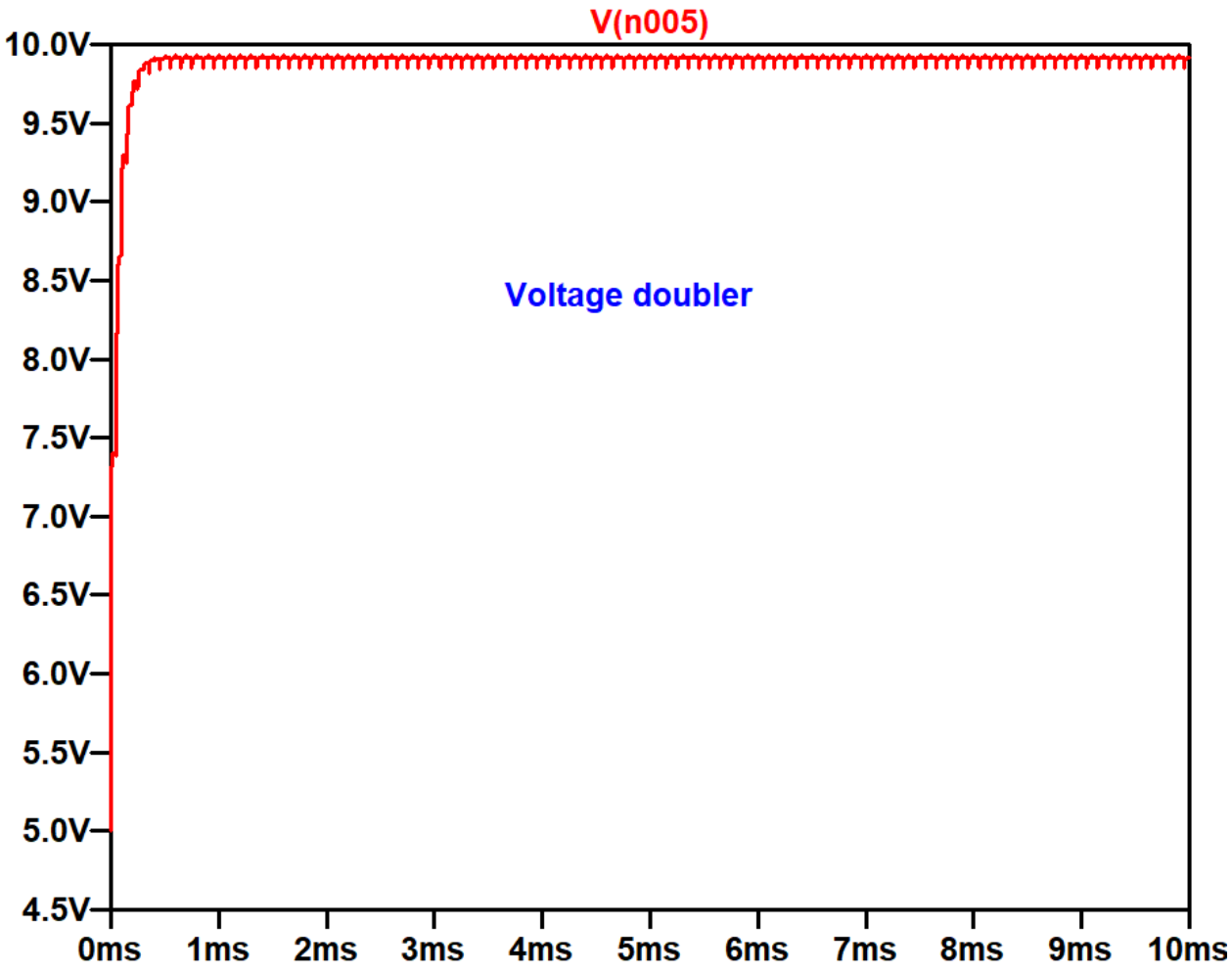
Voltage doubler design

Schematic



Voltage doubler schematic

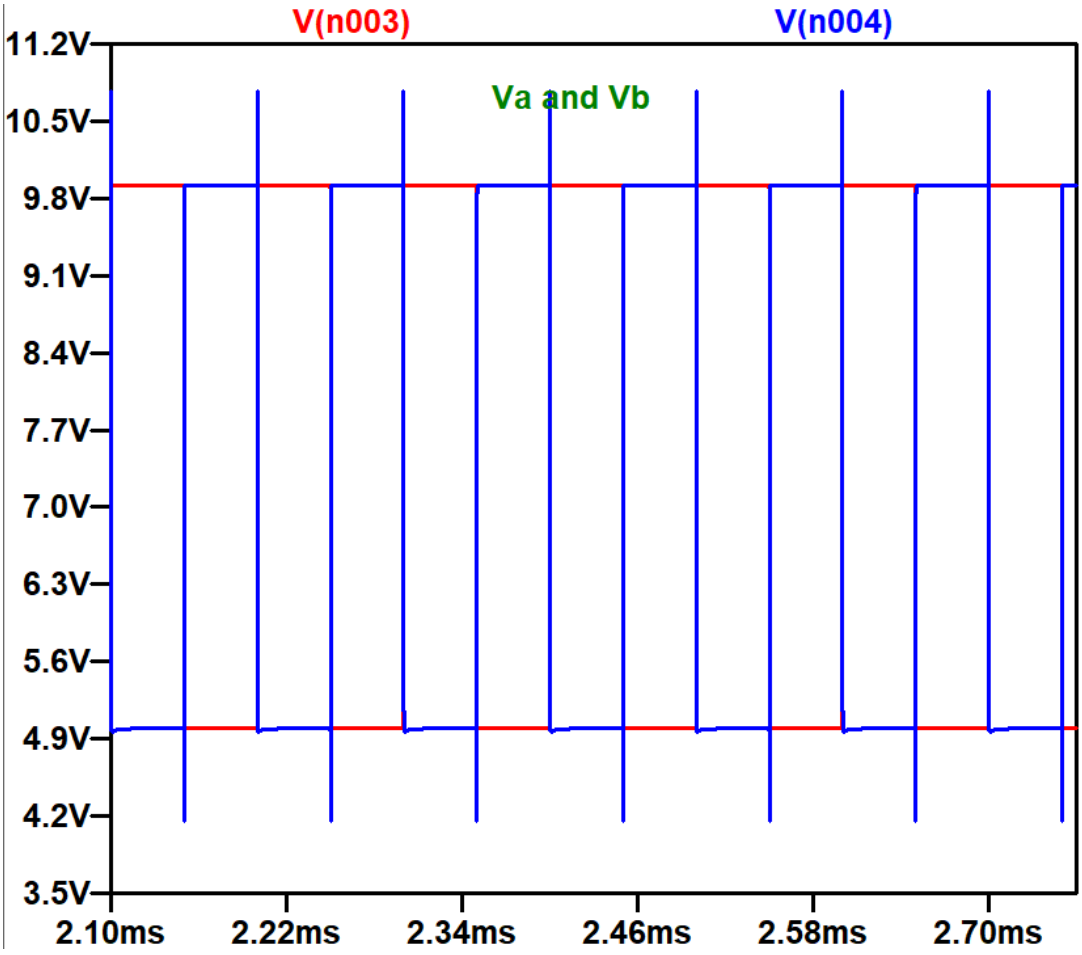
Output



V_{out} **Vs time**

• We have essentially use nmos in place of pmos in Question2 and vice versa and also replaced ground with VDD making the polarity of Capacitor opposite and so V_a will be square wave with 5V and 10V as maximum and minimum, V_b out of phase with V_a and so the pmos acting as switches maintaining constant 10V here.

V_a **and** V_b



V_a **and** V_b

Comments :

• No unusual observations have be observed here.

• Here we have completed our aim by designing a circuit with output twice the supply voltage.

• The main element here capacitor charging is the reason for higher voltage than supply and these circuits are used when a small portion of the IC needs a higher supply voltage, but multiple power supplies can't be used.


thank
you