

Analog Lab (EE2401)

Experiment 6 : PCB Design

EE19BTECH11041,
Srijith Reddy Pakala
Department of Electrical Engineering
IIT Hyderabad

March 11, 2021

1 Aim

our aim here is to design PCB boards for the voltage controlled oscillator using Kicad.

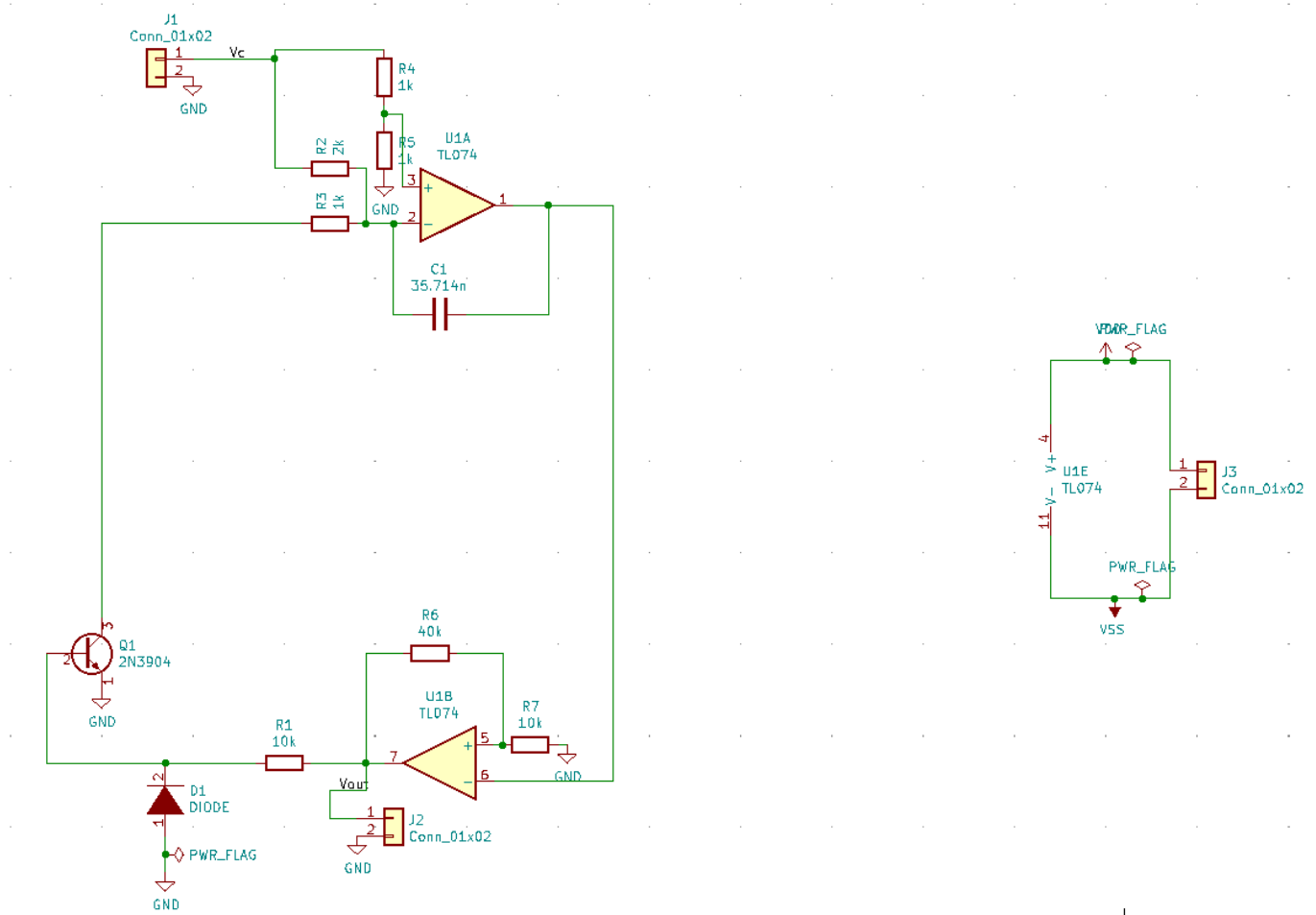
2 Problem statement

1. Design a PCB for the voltage-controlled oscillator implemented in Experiment 5.

- . • Two layer PCB.
- . • 2-pin connectors for supply, input and output.
- . • Use only one TL074 (same symbol and footprint as LF347) IC with four opamps.
- . • Through-hole package for all the components.
- . • DRC rule: Minimum track width and spacing - 10 mils, minimum via hole - 10 mils.

3 Design schematics and layout

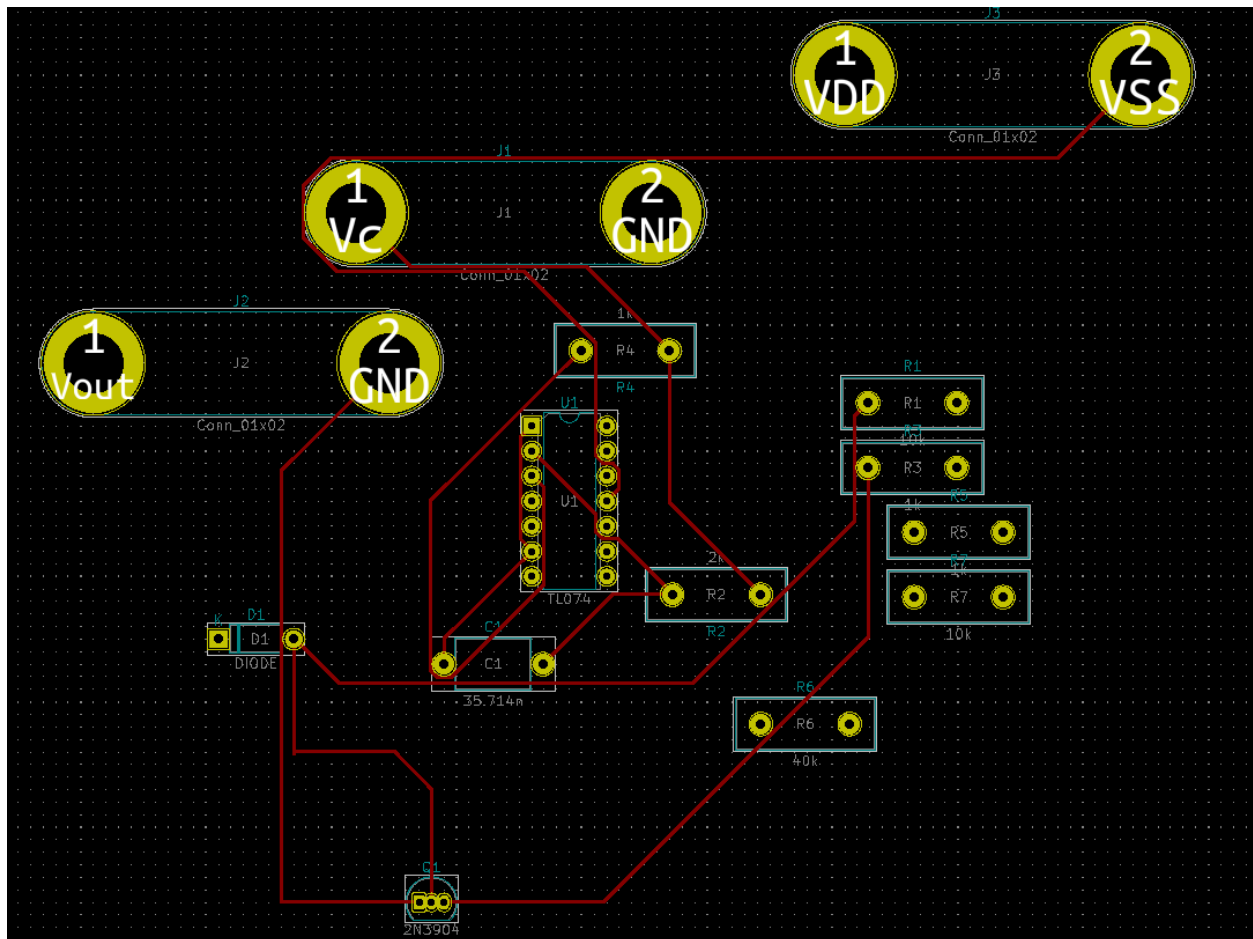
Schematic of the Voltage controlled oscillator



Circuit schematic

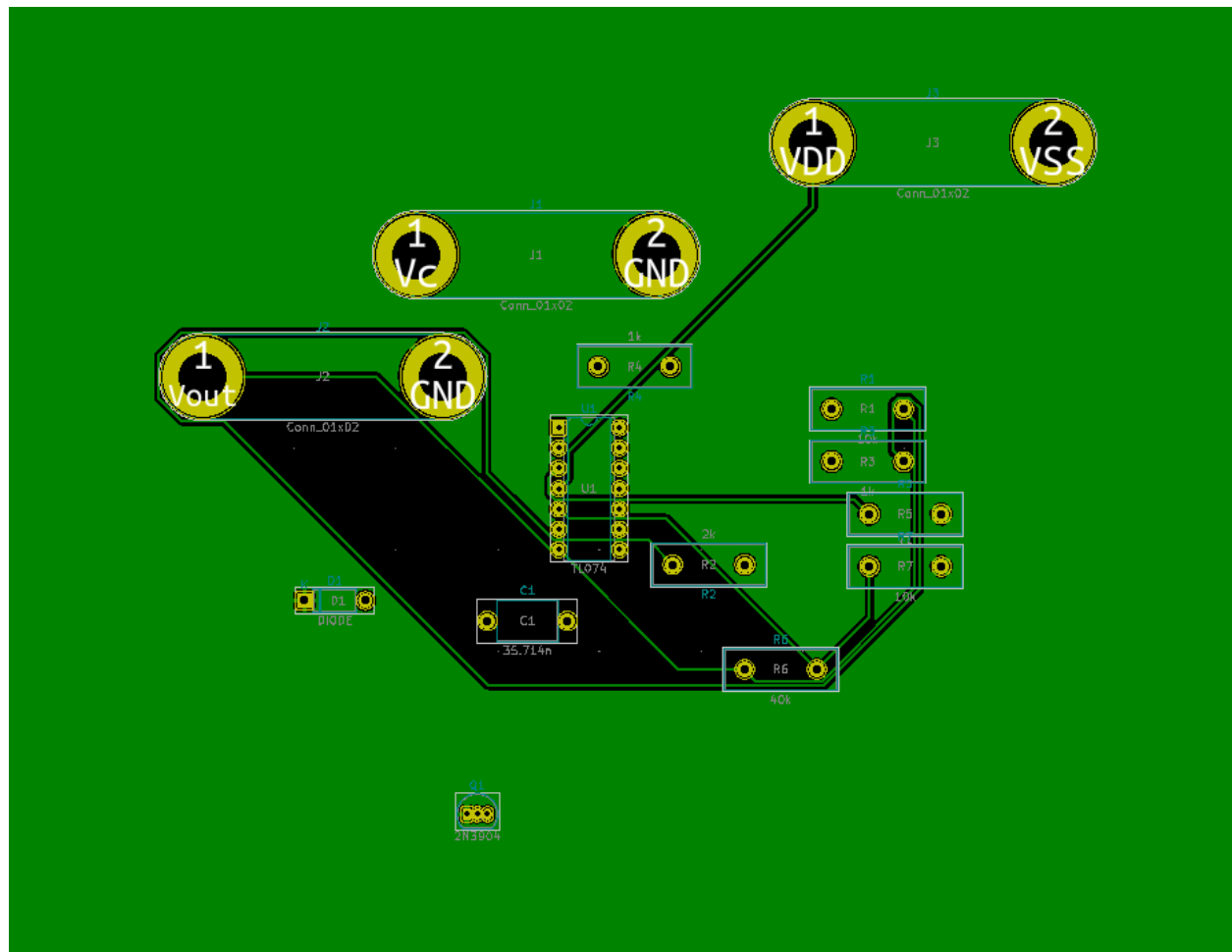
- Using the schematic I have generated a netlist to start PCB after checking for errors.

Layout of PCB Top layer



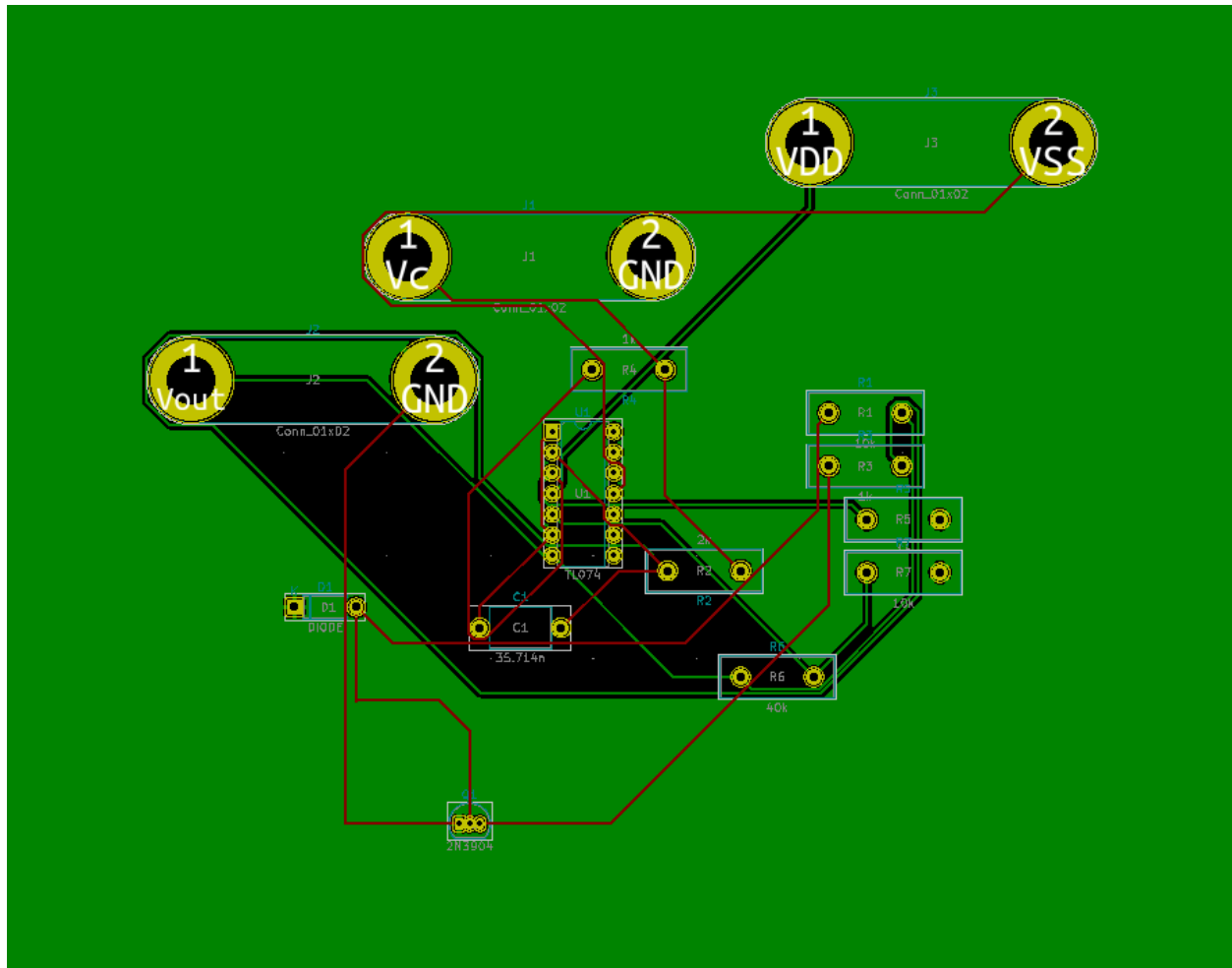
PCB layout Top layer

Layout of PCB Bottom layer



PCB layout Bottom layer

Layout of PCB Both layer



PCB layout Both layer

PCB minimum parameters for error checking

DRC Control ✕

Clearance: by Netclass

Minimum track width: mm

Minimum via size: mm

Minimum uVia size: mm

☐ Refill all zones before performing DRC

☐ Report all errors for tracks (slower)

☐ Test tracks against filled copper areas (very slow)

☐ Create report file: 📁

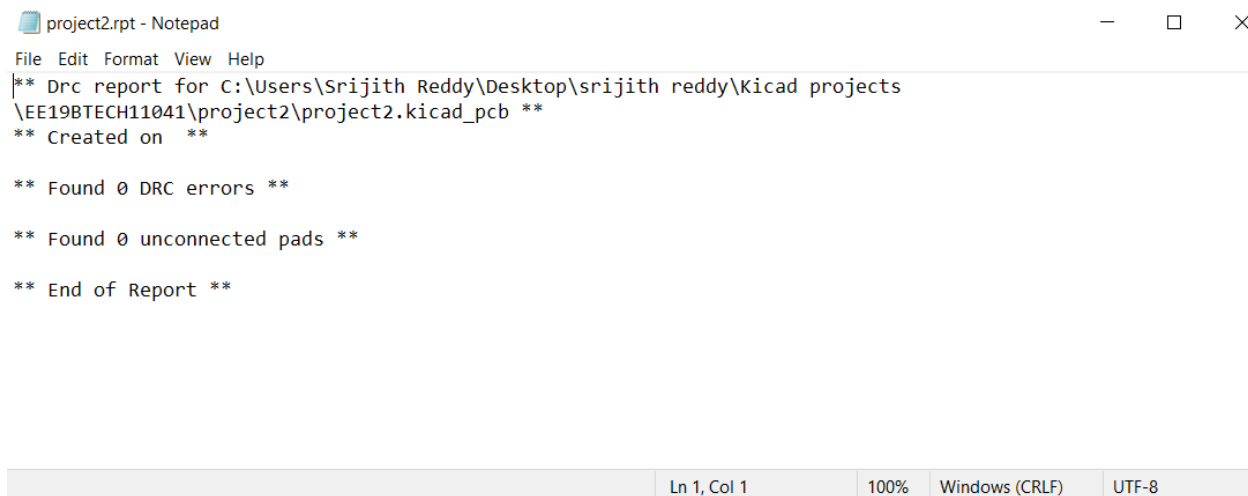
Messages

- Track clearances...
- Zone to zone clearances...
- Unconnected pads...
- Keepout areas ...
- Test texts...
- Courtyard areas...
- Items on disabled layers...
- Finished

Problems / Markers (0) Unconnected Items (0)

Delete Marker Delete All Markers Run DRC Close List Unconnected

PCB DRC Report



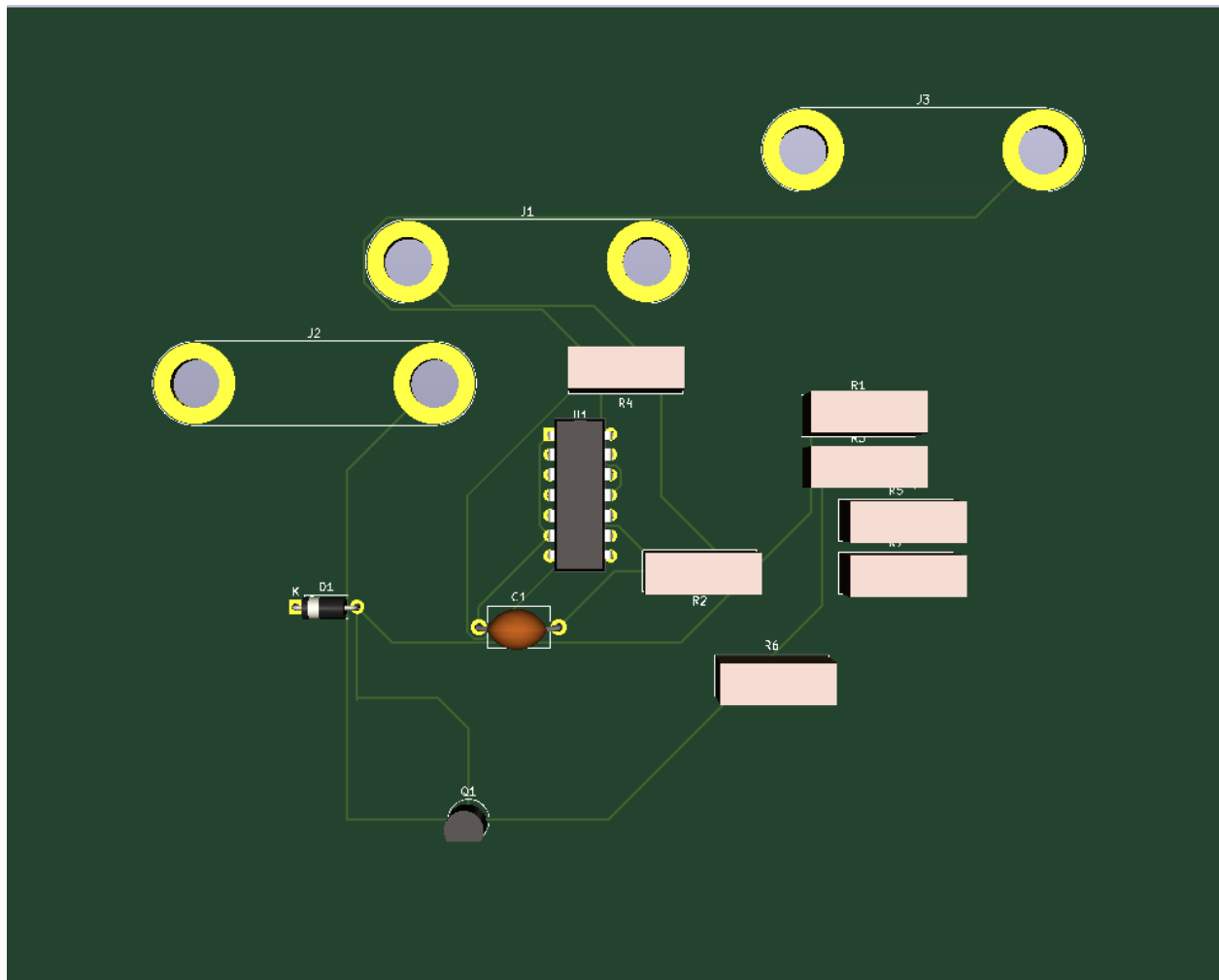
The screenshot shows a Notepad window titled "project2.rpt - Notepad". The menu bar includes "File", "Edit", "Format", "View", and "Help". The text content of the report is as follows:

```
** Drc report for C:\Users\Srijith Reddy\Desktop\srijith reddy\Kicad projects  
\EE19BTECH11041\project2\project2.kicad_pcb **  
** Created on **  
  
** Found 0 DRC errors **  
  
** Found 0 unconnected pads **  
  
** End of Report **
```

The status bar at the bottom indicates "Ln 1, Col 1", "100%", "Windows (CRLF)", and "UTF-8".

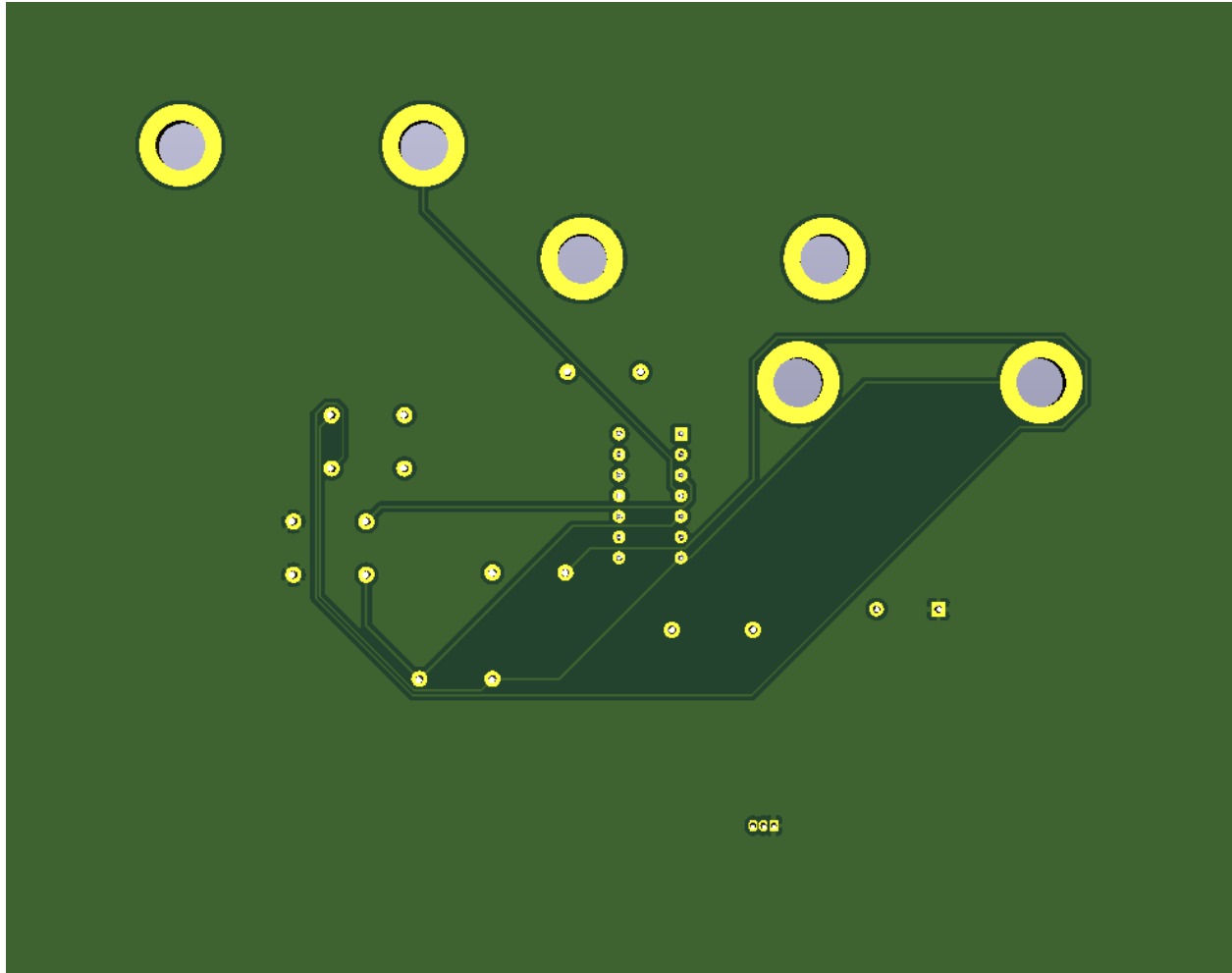
PCB DRC Report

3D view of PCB Top layer



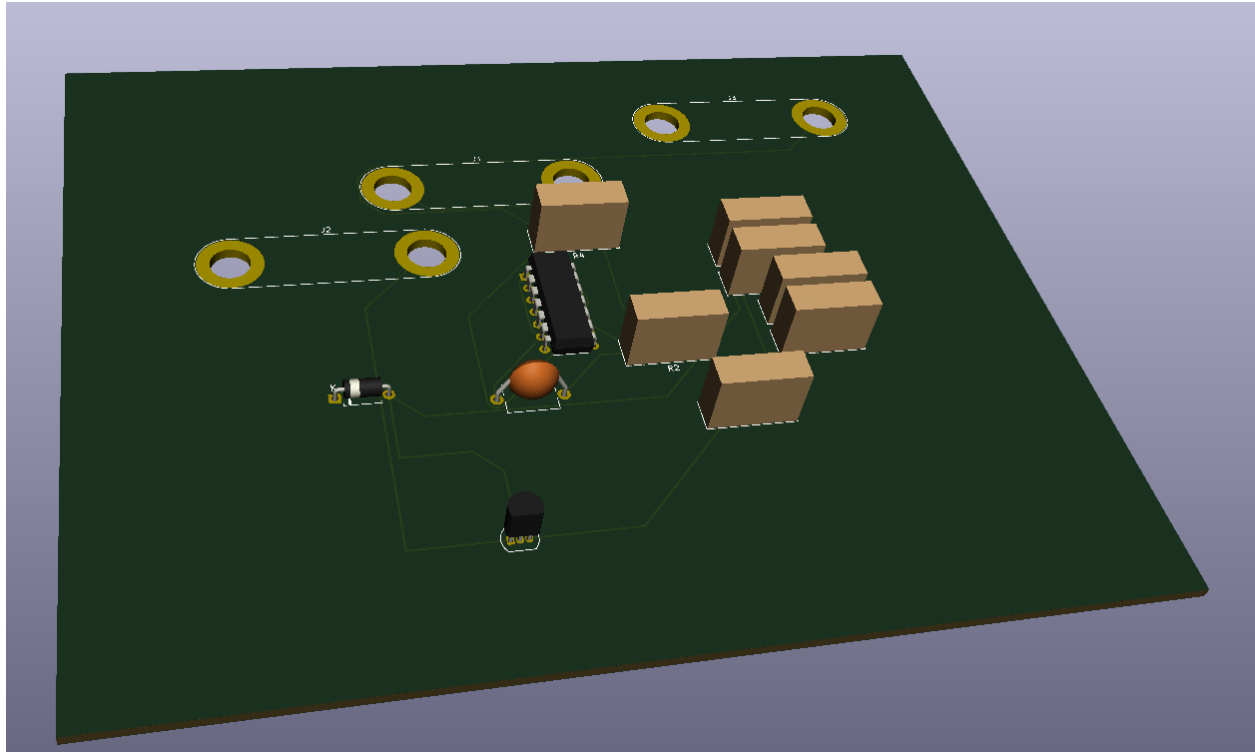
PCB 3d view Top layer

3D view of PCB Bottom layer



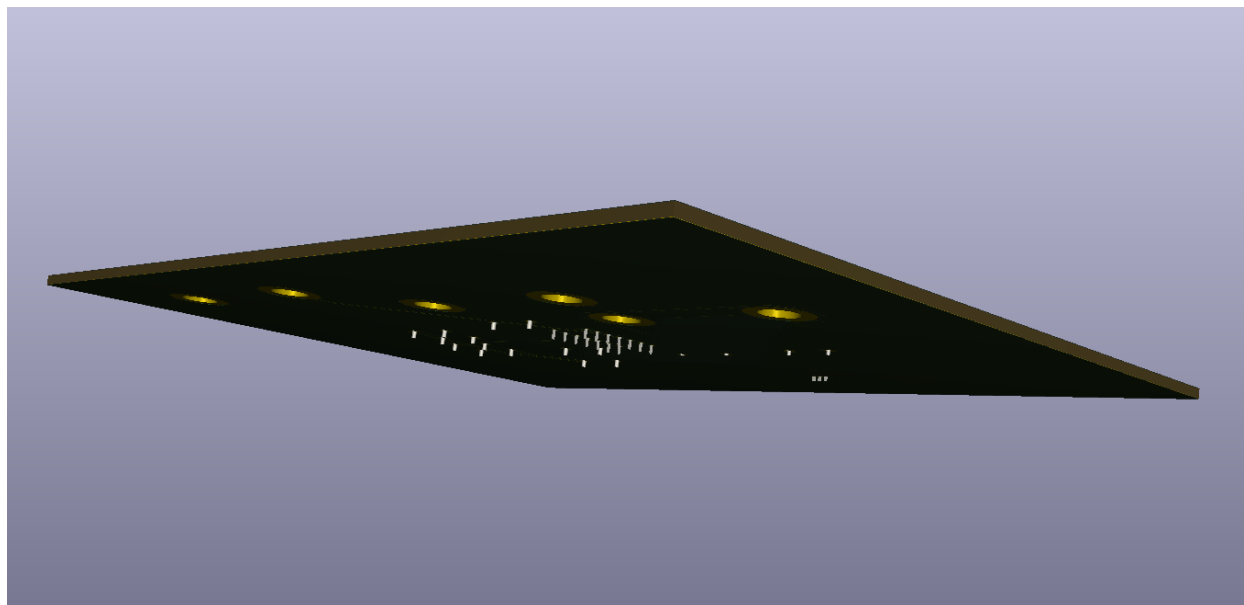
PCB 3d view Bottom layer

3D side view of PCB



PCB 3d view

3D side view of PCB



PCB 3d view

Thank
you