EE1025-Independent Project
XOR and XNOR GATES IMPLEMENTATION

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Abstract

This report exploits the importance of XOR,XNOR gates and their behavioral study(i/o).

AIM

Understanding explicitly about the inputs and outputs of XOR and XNOR gates and the implementation using basic gates.

INTRODUCTION

The XOR,XNOR function is frequently used in digital circuits to manipulate signals that represent binary numbers.XOR output is asserted whenever an odd number of inputs are asserted. The XNOR function is the inverse of the XOR function,the XNOR an even detector. These are very useful property will be exploited in data error detection circuits.Any odd number of input inversion changes the function output between the XOR and XNOR functions; any even number of input signal inversions does not change function outputs.

APPARTUS

These experiments are conducted on an open-source LT-spice.Voltage sources within the range 0-5V and symmetric pulse of frequency within the range 1Hz to 5KHz.

THEORETICAL BACKGROUND

The table used to represent the Boolean expression of a logic gate function called a truth table. A logic gate is an electronic circuit that operates on one or more input signals to produce an output signal. The switch contains two states which are ON or OFF. The ON

means the logic 1 and the OFF means the logic 0.

XOR gate

XOR represents the inequality function, i.e., the output is true if the inputs are not alike otherwise the output is false. A common way that resembles the XOR is must have one or the other, but not both.
An XOR gate is normally two inputs logic gate where, output is only logical 1 when only one input is logical 1. When both inputs are equal, that is either both are 1 or both are 0, the output will be logical 0.
This gate is generally called the inequality detector. And odd no.of ones lead to 1 orelse 0.

The logical(BOOLEAN) expression of the gate is :-

$$A \oplus B = A\overline{B} + \overline{A}B$$

In first case consider, A = 0 and B = 0.

$$\therefore A \oplus B = 0 \oplus 0 = 0.\overline{0} + \overline{0}.0 = 0.1 + 1.0 = 0$$

In second case consider, A = 0 and B = 1.

$$\therefore A \oplus B = 0 \oplus 1 = 0.\overline{1} + \overline{0}.1 = 0.0 + 1.1 = 1$$

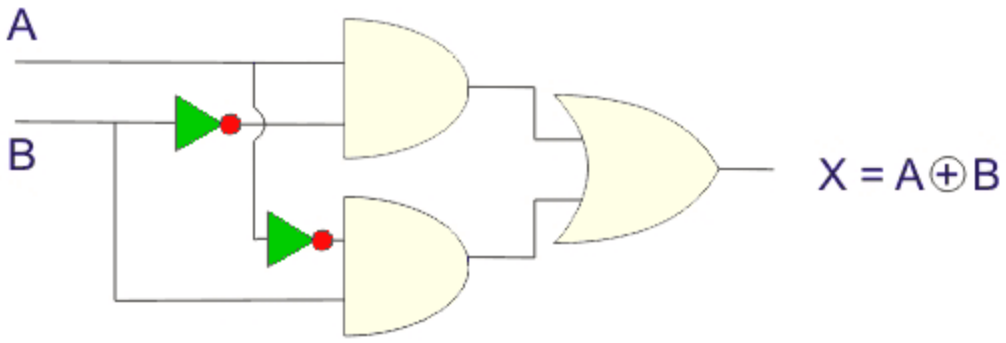
In third case consider, A = 1 and B = 0.

$$\therefore A \oplus B = 1 \oplus 0 = 1.\overline{0} + \overline{1}.0 = 1.1 + 0.0 = 1$$

In fourth case consider, A = 1 and B = 1.

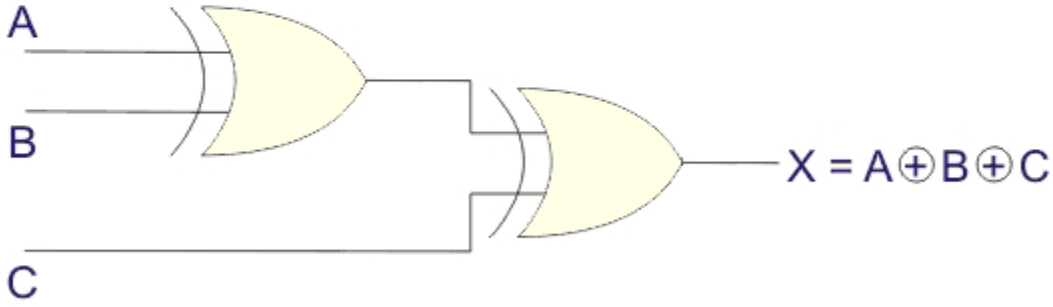
$$\therefore A \oplus B = 1 \oplus 1 = 1.\overline{1} + \overline{1}.1 = 1.0 + 0.1 = 0$$

The gate can be made up of AND and OR gates as logically verified and satisfying it's input and output properties. The circuit shown below explains it behavioral structure:-



Concatenating Two XOR gates gives three input XOR gate.

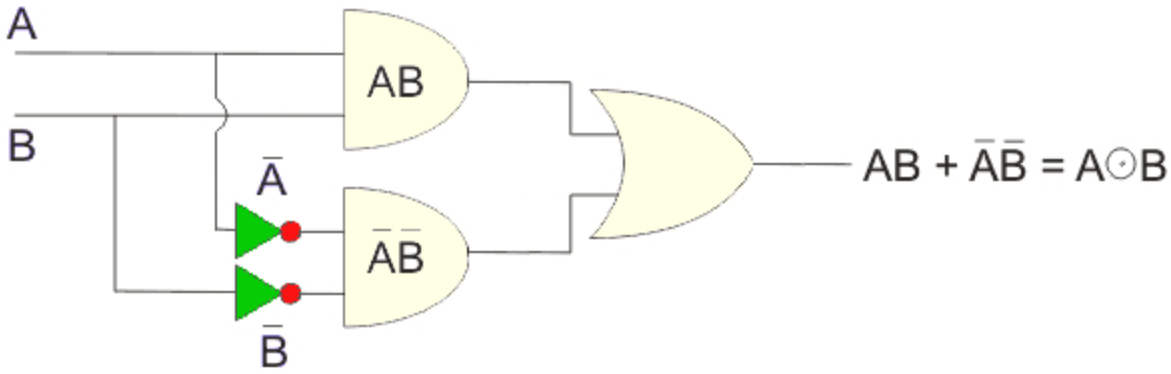
$$A \oplus B \oplus C = (A \oplus B) \oplus C$$



The main application of the Exclusive OR gate is in the operation of half and full adder.Pseudo-random number generation to model a linear feedback shift register XOR gates are used and they generate random sequence of bits.Xor gate can also be used as a controlled inverter.

XNOR gate

The XNOR gate is very similar in design just with inverters change positions as compared to XOR gate. XNOr represents the equality function. XNOR exhibits an inverse of XOR gate. In the case of XNOR gate, the output is 0 when only one input is 0 and the output is 1 when both inputs are same that is either both of them are 0 or 1. This gate is logically expressed as:-



The expression of XNOR operation can be realized by using two NOT gates, two AND gates and one OR gate as follows

$\therefore A \odot B = AB + \bar{A}\bar{B}$.

The XNOR logic gates are used in error detecting circuits which are to detect Odd parity or even parity bits in digital data transmission circuit and in arithmetic and encryption circuits.

EXPERIMENTATION

Task-1-XOR USING BASIC GATES:-

Step 1:-Connecting the two input AND gates and OR gate with inverters as shown below.

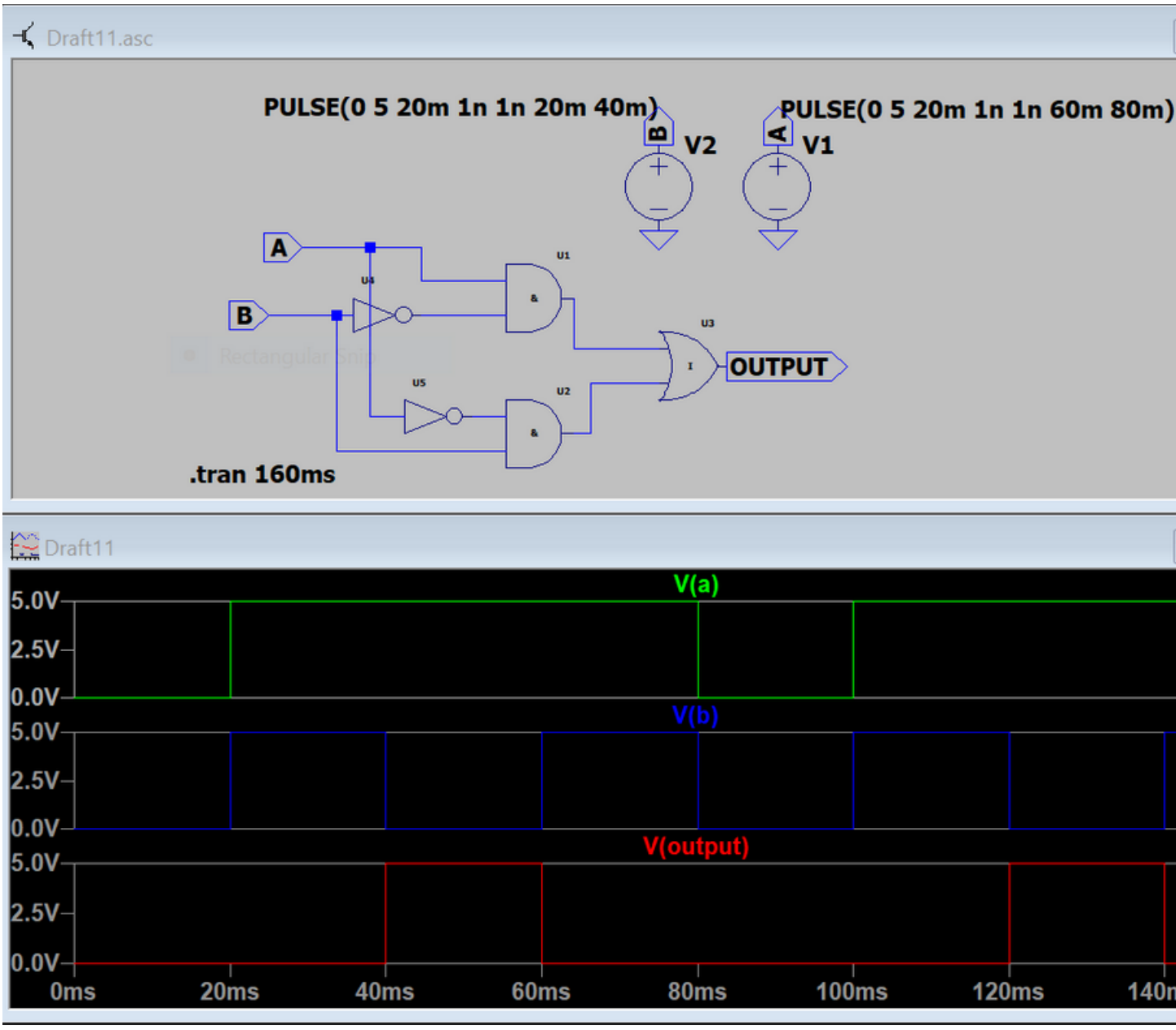
Step 2:-Considering 1st Voltage input(A) as a symmetric pulse of time period of 80m and duty cycle of 75 percent (A duty cycle or power cycle is the fraction of one period in which a signal or system is active.) And ON -voltage as 5 and OFF- voltage as 0.

Step 3:- Considering 1st Voltage input(A) as a symmetric pulse of time period of 40m and duty cycle of 50 percent.And ON -voltage as 5 and OFF- voltage as 0.

Step 4:- Simulating the system for 160ms in transient analysis.

Outcomes:-

XOR gate characteristics are verified i.e, output signal is high when both inputs aren't same and low when they are.

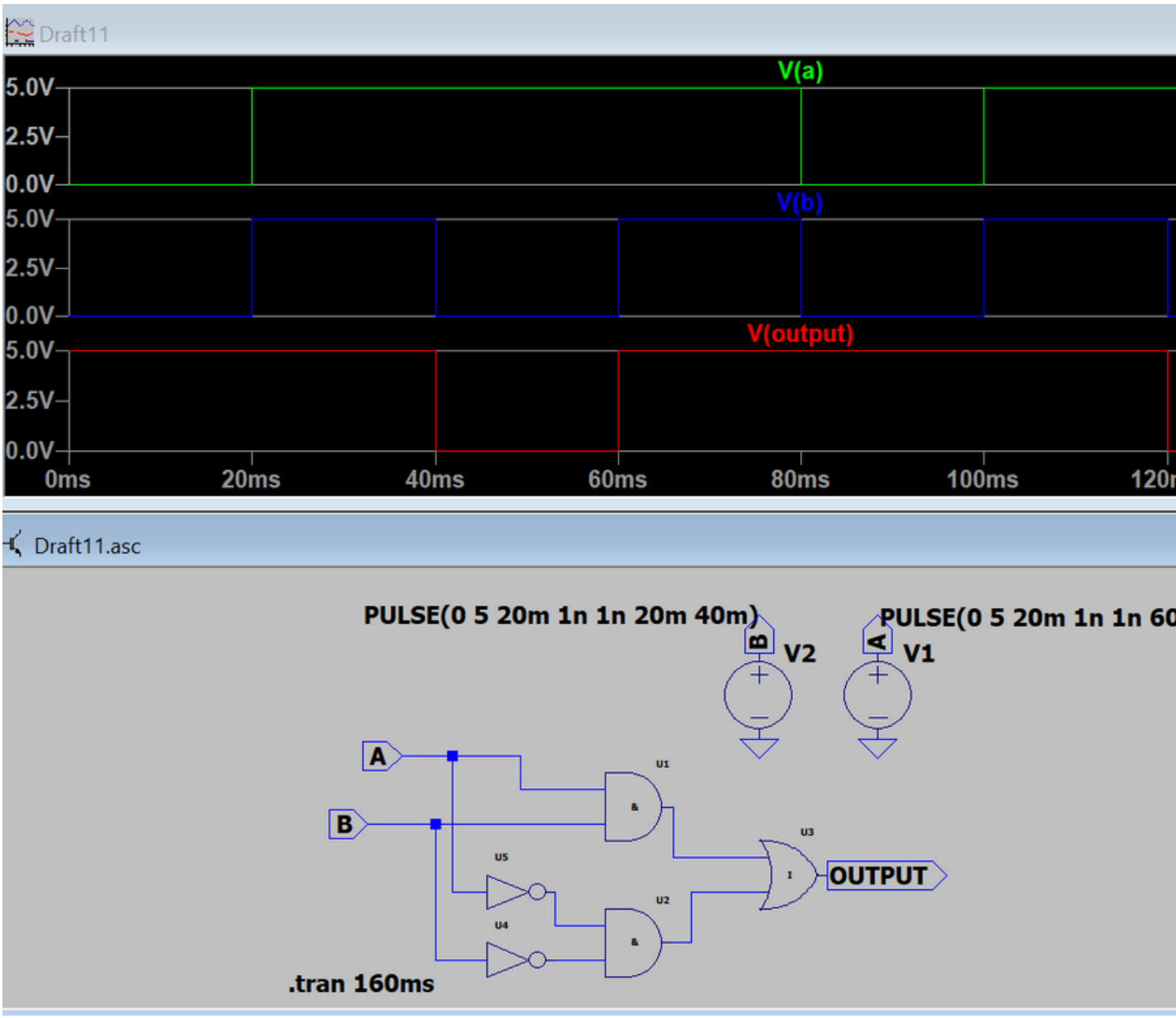


Task-2-XNOR USING BASIC GATES:-

The same steps are followed as Task -1

Outcomes:-

XNOR gate characteristics are verified i.e, output signal is high when both inputs are same and low when they aren't.



Task-3-SIMULATING THREE INPUT XOR AND XNOR:-

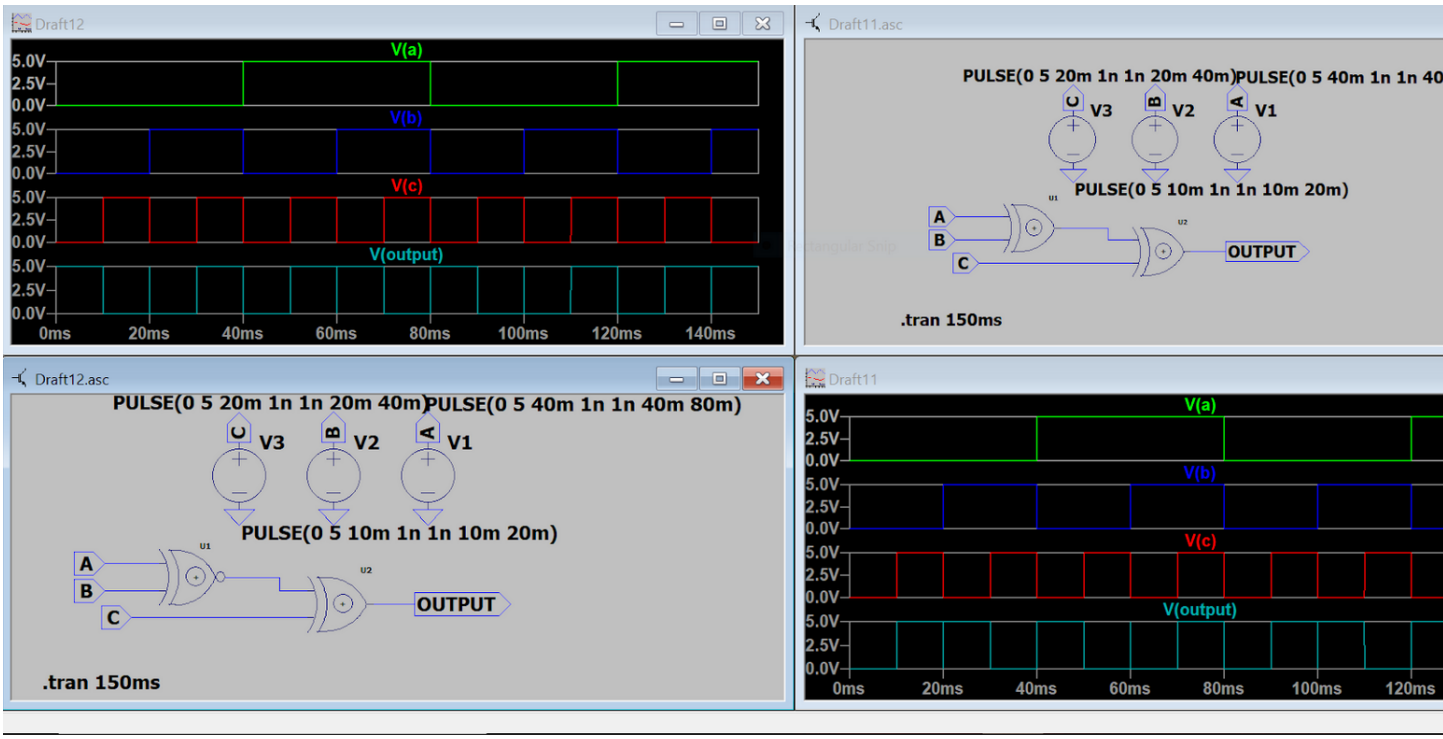
Step 1-Concatenating two XOR gates as shown below gives us the three input XOR gate.(output of one xor gate is connected to other).Similarly,for three input XNOR gate concatenating one XNOR with XOR gate.

Step 2-Exciting the system with voltage sources :-V(A) with time period 80m which twice of V(B) and V(B)'s time period is twice of V(C).All are of with duty cycle-50 percent.

Step 3-Simulating the system for 150ms in transient analysis.

Outcomes:-

The important observation is that the xor and xnor gates are complement everywhere.And the output of XOR gate is high if and only if odd of gates inputs are high.Conversly , XNOR gate is high if and only if even of gates inputs are high.



CONCLUSIONS

The XOR output is asserted whenever an odd number of inputs are asserted, and the XNOR is asserted whenever an even number of inputs are asserted: the XOR is an odd detector, and the XNOR, an even detector.