Electronic Devices and Circuits Lab (EE2301)
Experiment 8 : Logic Gates

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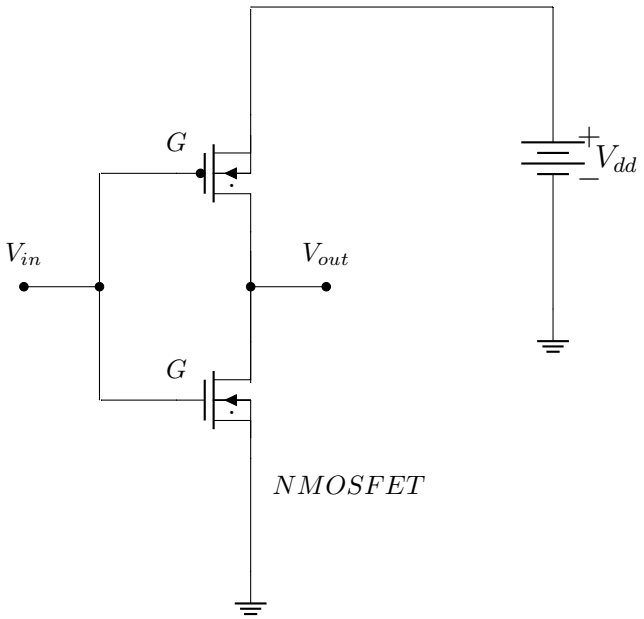
1 Aim

our aim here is to understand the logic gates i.e. NOT gate , NAND gate and AND gate.

NOT Gate

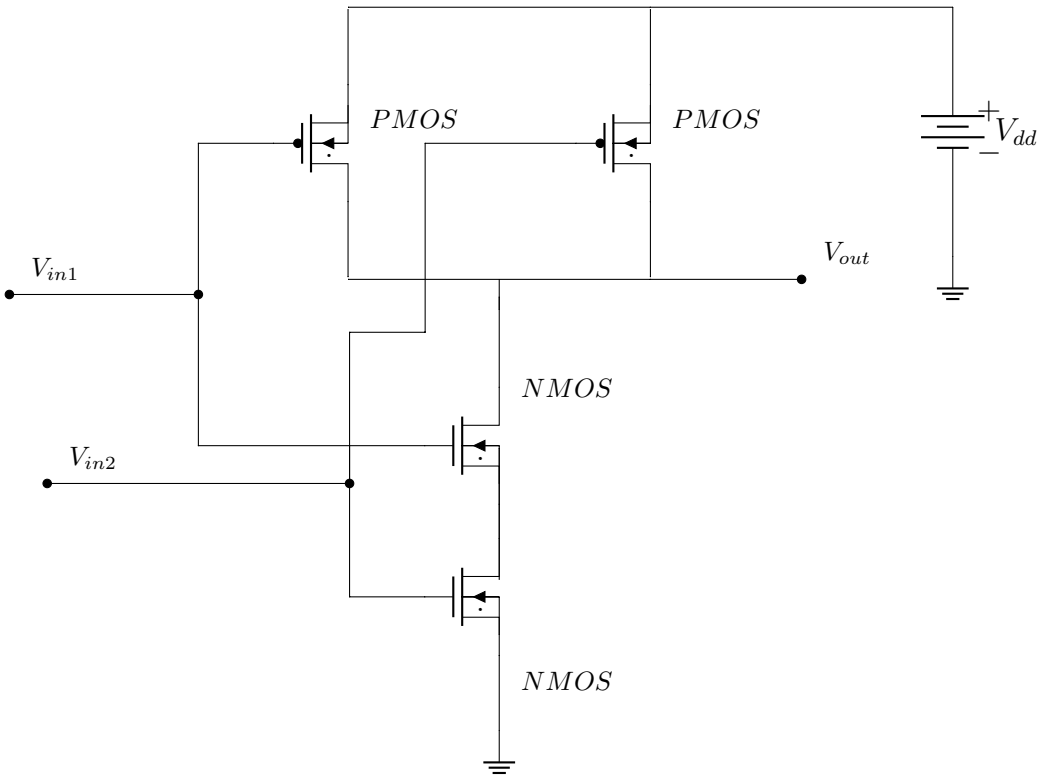
An inverter or NOT gate is a logic gate which implements logical negation.



NOT Gate circuit diagram

NAND Gate

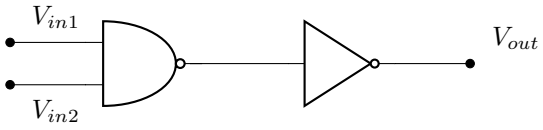
A NAND gate (NOT-AND) is a logic gate which produces an output which is false only if all its inputs are true.



NOT Gate circuit diagram

AND Gate

An AND gate is a logic gate which produces an output which is true only if all its inputs are true.



AND Gate using NAND and NOT Gates

2 Problem statement(Group 1)

• Implement NOT Gate in NgSPICE with W = 10 m W_p = 1 m and plot the V_{in} v/s V_{out} and explain the operation.

• Implement 2 input NAND logic gate and verify the operation. The inputs are through the pulse generator.

• Using NAND and NOT gate implement AND gate in NgSPICE (use sub-circuits). Verify the operation of the AND gate.

3 Procedure

NOT Gate

• First we need to write spice scripts for the NOT Gate circuit with given gate width values and varying input(V_{in}).

• Now we need to plot the V_{out} vs V_{in} and analyse the output.

• Now we need to explain the operation by using MOSFET characteristics.

• We should also explain the effect of gate width on the output.

NAND Gate

• First we need to write spice scripts for the NAND Gate circuit with given values and use inputs with pulse generator.

• We need to use square waveform like pulses with 1 input frequency twice the other to verify all the cases and plot the output with respect to time.

• At this point we need to verify the simulation output with the desired output.

AND Gate

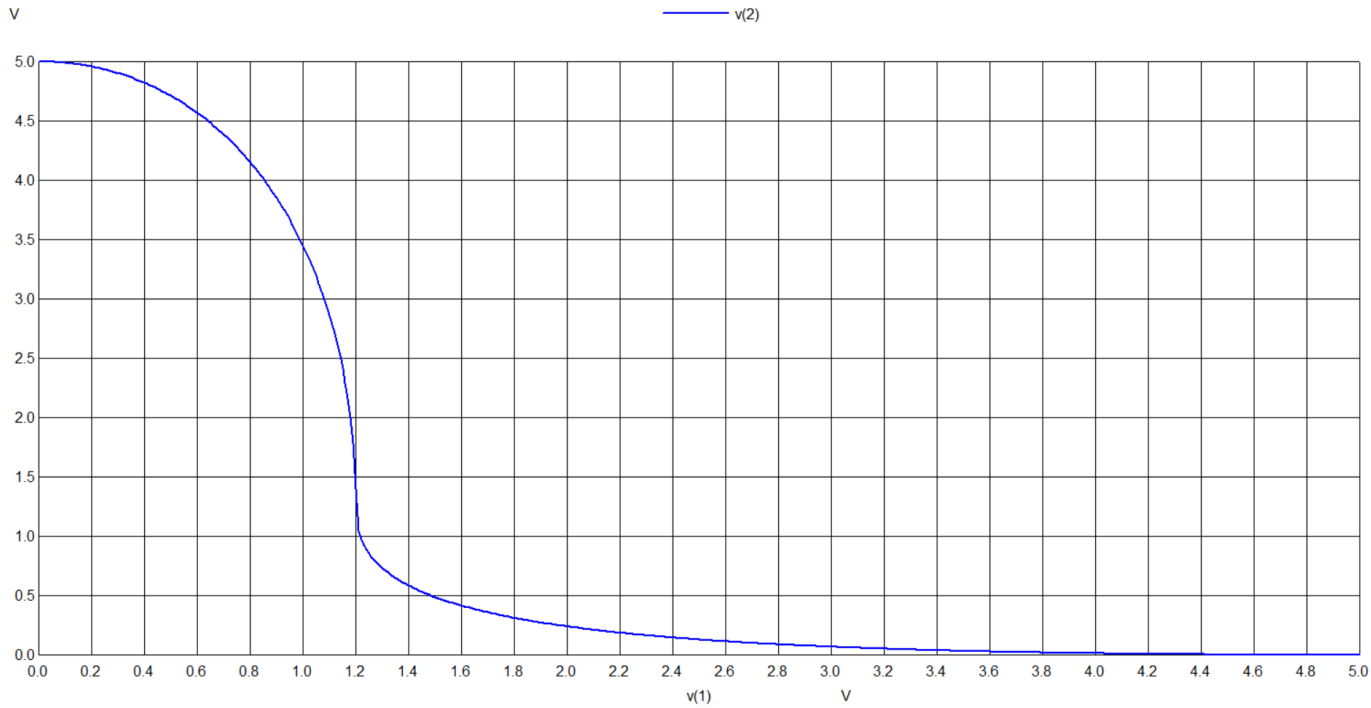
• In this we need to use the script for NAND and NOT gates to make an AND gate with the inputs same as the NAND Gate.

• Here we need to connect the output of NAND to NOT gate and output of NOT gate is the final output.

• At this point we need to verify the simulation output with the desired output.

4 Results and observations

NOT Gate output



Plot: V_{out} **Vs** V_{in}

• In the above plot We can see that the output is 5V when input is 0V and the output decreases as input increases at some point it decreases quickly and now slowly decreses to 0V as input approaches 5V .

Working of NOT Gate

• When the input is 0V, the NMOSFET's channel has high resistance(R_N) limiting the current flow from ground to output and the PMOSFET's channel has low resistance(R_P) allowing the current flow from supply to the output.the voltage drop between the supply voltage and output due to a current drawn from Output is small. Therefore the output,registers 5V.

• When input is 5V, the NMOSFET's channel has low resistance(R_N) allowing much more the current flow from ground to output and the PMOSFET's channel has high resistance(R_P) limiting the current flow from supply to the output.the voltage drop between the ground and output due to a current drawn from Output is small. Therefore the output,registers 0V.

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• We can better understand this from below equation.

$$V_{out} = \frac{V_S R_N}{R_N + R_P} + \frac{V_D R_P}{R_N + R_P} = \frac{5R_N}{R_N + R_P} \tag{1}$$

• Please note that the Values of R_N and R_P are not constant and that there are no actual resistors but just the effect of them , the above equation is only for the understanding.

Effect of Gate width(W)

• Here the effect of gate width can be seen in the transient output between input 0V and 5V.

$$V_G = V_{ch} + Et_{ins} \tag{2}$$

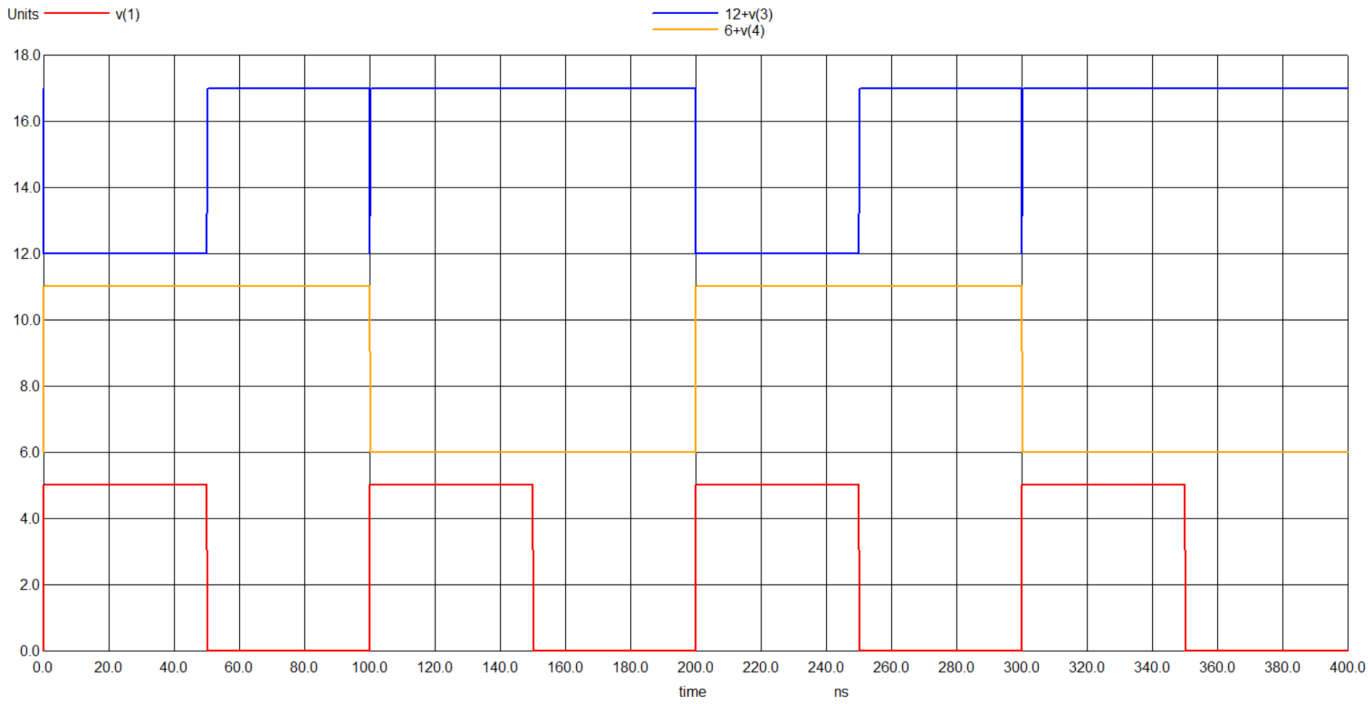
where V_G = gate voltage,V_{ch} = voltage at channel side of insulator,E = electric field and t_{ins} = W =insulator thickness.

• Now if we increase the gate Width (W) the voltage at channel side of insulator V_{ch} decreases which results in higher resistance state in NMOSFET.

• Now if we increase the gate Width (W) the voltage at channel side of insulator V_{ch} decreases which results in lower resistance state in PMOSFET.

• Now we can see why the output is saturated to 0V when input is 5V when compared to 5V output when the input is 0V.

NAND Gate output



Plot: V_{out}(blue),V_{in2}(red),V_{in1}(orange) Vs Time (ns)

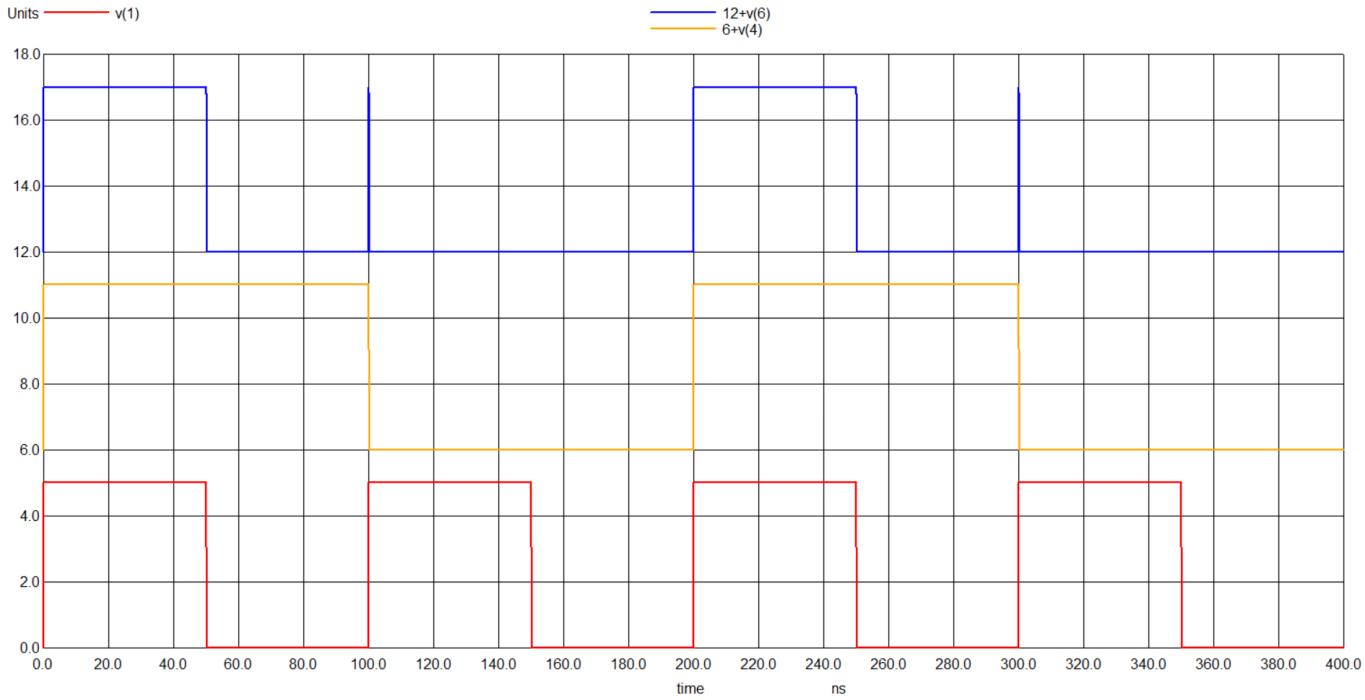
• In the above plot We can see that the input 1 has timeperiod of 200ns and input2 has timeperiod of 100ns which gives all four types of inputs for NAND Gate i.e. (5v,5v),(5v,0v),(0v,5v),(0v,0v).

Verification of NAND Gate

V_{in1}	V_{in1}	V_{out} (Simulation output)	Desired output
0V	0V	5V	5V
5V	0V	5V	5V
0V	5V	5V	5V
5V	5V	0V	0V

• The desired output matches with simulation output.

AND Gate output



Plot: V_{out}(blue),V_{in2}(red),V_{in1}(orange) Vs Time (ns)

• In the above plot We can see that the input 1 has timeperiod of 200ns and input2 has timeperiod of 100ns which gives all four types of inputs for AND Gate i.e. (5v,5v),(5v,0v),(0v,5v),(0v,0v).

Verification of AND Gate

V_{in1}	V_{in1}	V_{out} (Simulation output)	Desired output
0V	0V	0V	0V
5V	0V	0V	0V
0V	5V	0V	0V
5V	5V	5V	5V

• The desired output matches with simulation output.

5 Conclusions

• We can conclude that NOT Gates can be used for different purposes by changing its gate width.

• We should also note that there is a slight impulse in output at 100ns which can be accounted to transient of inputs changing from 0V to 5V and the other from 5V to 0V.

• We use these logic gates in almost every device we use daily , a phone, laptop , a TV,etc.

• Key advantage of a Logic Gates is the extremely micro size of the MOSFETs and that it's completely voltage controlled.

• We can perform the most basic operations such as Addition, Subtraction using Logic gates very easily.

Thank you