EE3301 : Introduction to VLSI Design
Homework Assignment 1

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Contents

1 SPICE Analyses

1.1 Problem Statement

(a) Calculate the operating point of the circuit in Figure 1 using '.op' command given $V_{IN} = 2.5$ V .

(b) Perform a transient simulation to calculate the phase lag introduced by the circuit if $V_{IN} = \sin \omega t$ with $\omega = 100$ Hz and 1 MHz. Estimate the phase lag using analytical expression and compare.

(c) Plot the amplitude and phase transfer characteristics of the filter using $V_{IN} = \sin \omega t$. Determine the 3 dB point and the corresponding phase lag.Compare with analytic expressions.

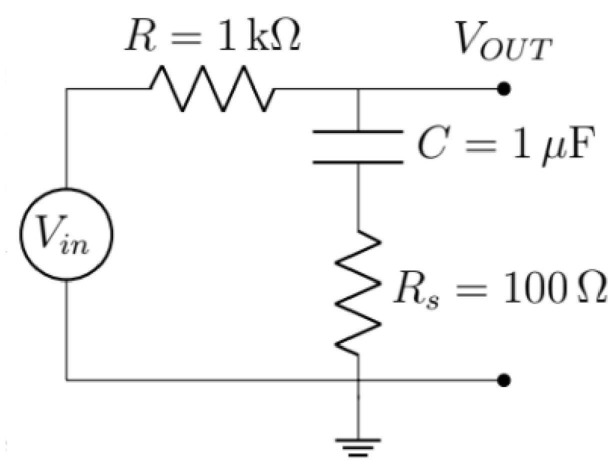


Figure 1

1.2 Spice Netlist

```
C1 N002 N003 1µ
V1 N001 0 SINE(0 1 1000)
R1 N003 0 100
R2 N002 N001 1k
.meas t1 TRIG v(n001)=0 RISE=5 TARG v(n001)=0 RISE=6
.meas t2 TRIG v(n001)=0 RISE=5 TARG v(n002)=0 RISE=5
.meas phase param 360*(t2/t1)
.tran 1
.backanno
.end
```

1.3 Solution

(a) The DC operating point values are as follows:

- V(R) = 0V
- V(R_s) = 0.25 fV
- V(C) = $2.5-\left(2.5\times10^{-16}\right)\approx 2.5V$
- I(R) = $-2.66454\times10^{-18}A$
- I(R_s) = $2.5\times10^{-18}A$
- I(C) = $2.5\times10^{-18}A$

(b)

f= 100 Hz

The simulated value of phase ϕ = 31.4735°

Analytical

$$\phi = tan^{-1}\left(\frac{1}{\omega R_s C}\right) - tan^{-1}\left(\frac{1}{\omega(R_s+R)C}\right) = 31.1^\circ \tag{1}$$

f= 1000 Hz

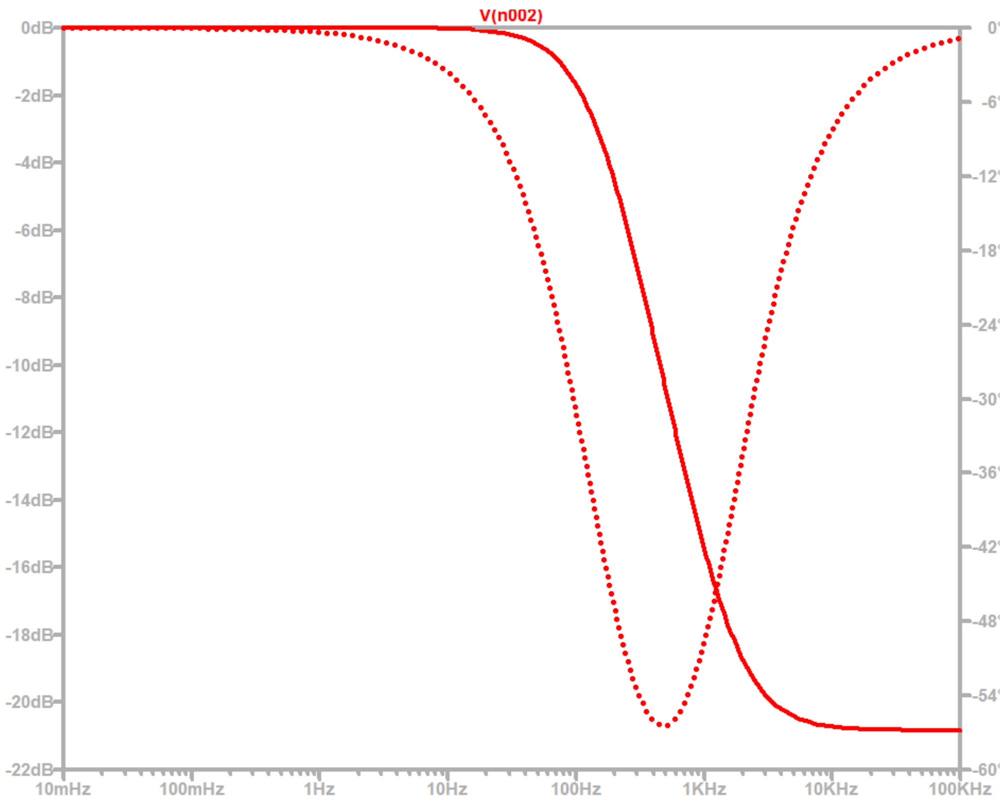
The simulated value of phase ϕ = 48.6276°

Analytical

$$\phi = tan^{-1}\Big(\frac{1}{\omega R_s C}\Big) - tan^{-1}\Big(\frac{1}{\omega (R_s + R) C}\Big) = 49.7^{\circ} \tag{2}$$

(c)

Bode Plot



V_o Bode Plot

$$\omega(-3dB) = 145.72075\ Hz \tag{3}$$

$$phase\ lag = 7.45^\circ \tag{4}$$

Analytical expressions

$$\frac{V_o}{V_{in}} = \frac{1 + SR_sC}{1 + S(R_s + R)C} \tag{5}$$

$$Magnitude = \frac{\sqrt{1 + (R_sC\omega)^2}}{\sqrt{1 + ((R_s + R)C\omega)^2}} \tag{6}$$

$$\omega(-3dB) = \sqrt{\frac{1}{((R_s + R)C)^2 - 2(R_sC)^2}} = 145.89Hz \tag{7}$$

$$Phase = tan^{-1}\left(\frac{1}{\omega R_sC}\right) - tan^{-1}\left(\frac{1}{\omega(R_s + R)C}\right) = -7.44^\circ \tag{8}$$

2 Analytic calculations vs SPICE simulations

2.1 Problem Statement

(a) Consider the adjacent circuit. Using a simple model, with V_{Don}= 0.7 V, solve for I_D.

(b) Find I_D and V_D using the ideal diode equation. Use $I_s = 10^{-14}$ A and T = 300 K.

(c) Run a SPICE simulation to validate your results in (a) and (b).

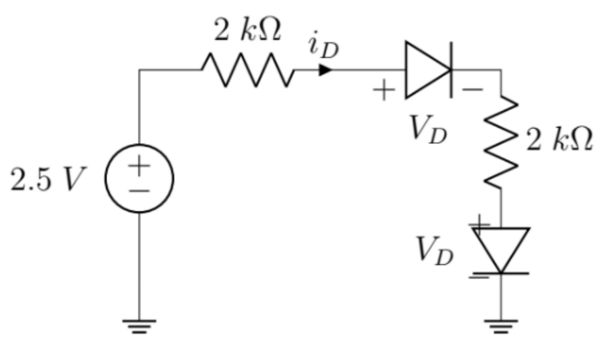


Figure 2

2.2 Spice Netlist

```
D1 N002 N003 D
D2 N004 0 D
R1 N003 N004 2k
R2 N002 N001 2k
V1 N001 0 2.5
.model D D
.lib standard.dio
.tran 1
.backanno
.end
```

2.3 Solution

(a)

Using Kirchhoff's Voltage Law,

$$V_{in} = 2I_D R + 2V_D \tag{9}$$

$$I_D = \frac{V_{in} - 2V_D}{2R} \tag{10}$$

where R = 2k Ω, V_{Don}= 0.7 V.

- I_D = 275 mA for simple model here.

(b) **Ideal Diode Equation :**

$$I_D = I_s\left(e^{\frac{qV_D}{nkT}} - 1\right) \tag{11}$$

$$I_D = \frac{V_{in} - 2V_D}{2R} \tag{12}$$

Intersection point of Equations (11) and (12) is the Q - point.

- I_D = 312.077 mA , V_D = 0.625845 V.

(c)

```
       --- Operating Point ---

V(n002):       1.87503        voltage
V(n003):       1.25           voltage
V(n004):       0.625033       voltage
V(n001):       2.5            voltage
I(D2):         0.000312489    device_current
I(D1):         0.000312489    device_current
I(R2):         -0.000312483   device_current
I(R1):         0.000312483    device_current
I(V1):         -0.000312483   device_current
```

The simulation values are I_D = 312.489 mA, V_D = 0.625033 V.

The simulation values are closer to Ideal diode equation values compared to Simple model values

3 Controlled sources

3.1 Problem Statement

A voltage controlled current source is driven by ac source, $v_{in} = 1\ V_{p-p}$, 1 kHz. Simulate the output response and calculate the gain in the circuit.

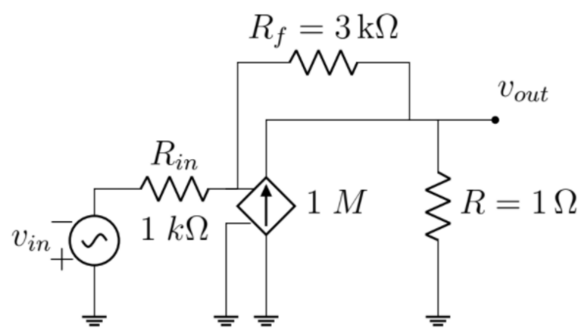


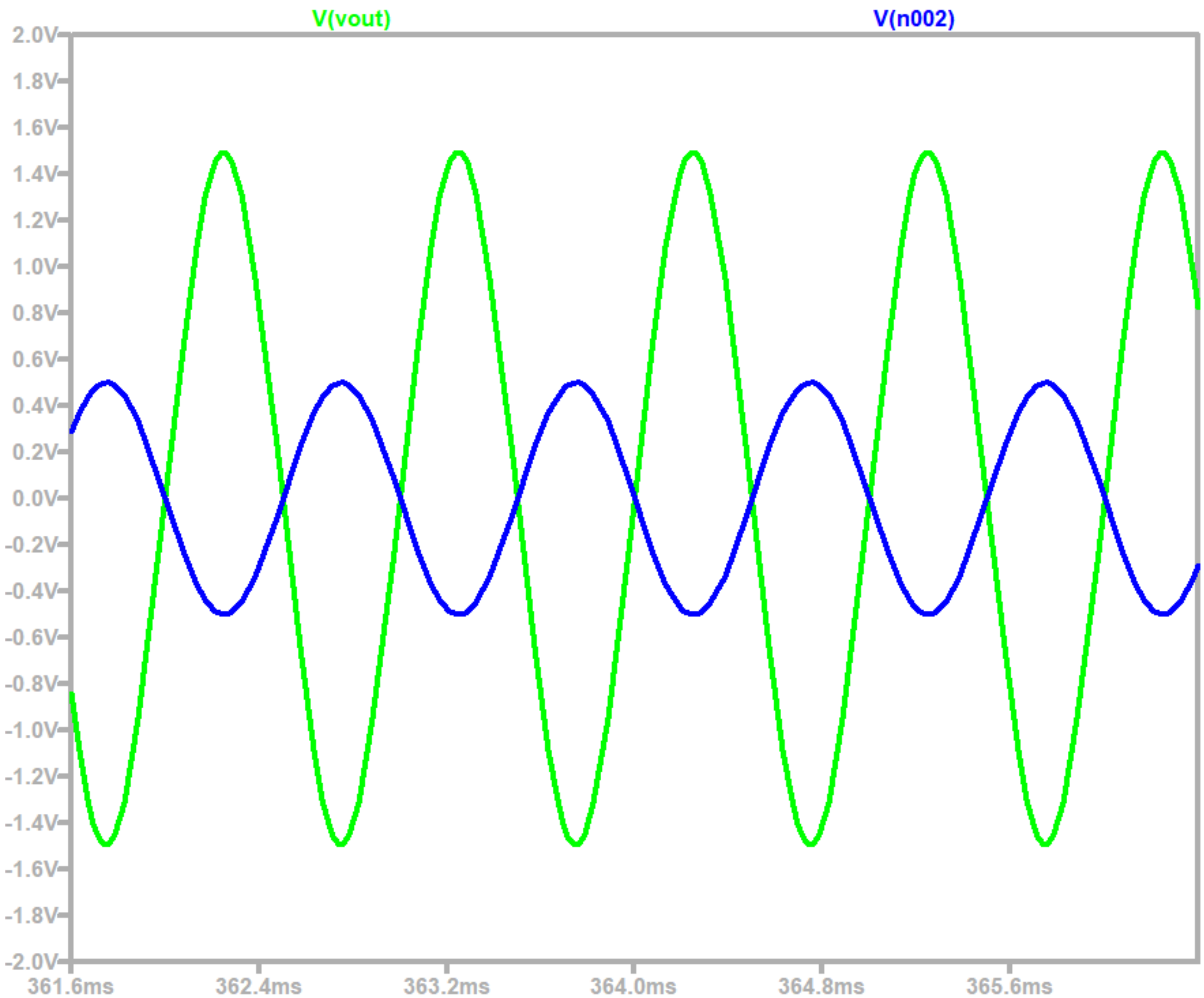
Figure 3

3.2 Spice Netlist

G1 0 Vout N001 0 1Meg
Rin N001 N002 1k
Vin 0 N002 SINE(0 0.5 1k)
R Vout 0 1
Rf Vout N001 3k
.tran 1
.backanno
.end

3.3 Solution

Output Response



V_{out}(Green) and V_{in}(Blue)

$$Gain = \frac{V_{out}}{V_{in}} = -\frac{V_{out(p-p)}}{V_{in(p-p)}} = -2.98 \tag{13}$$

4 MOSFET Characteristics

4.1 Problem Statement

Consider long and short channel MOSFETs with L = 10 µm and L = 0.18 µm respectively. Both devices have identical W/L of 1.5.

(a) Simulate the IV characteristics of PMOS and NMOS devices using 180 nm Predictive Technology Model (PTM). Your results will be similar to Fig. 3.19 and 3.21 of reference [1]. Remember the maximum supply voltage for regular devices is only 1.8 V in this technology.

(b) Identify the transition between linear and saturation regions of operation of these MOSFETs. Annotate the regions of operation on the graphs obtained in part (a). Indicate the differences between short and long channel MOSFETs in your graphs.

(c) Calculate the small signal output resistance of NMOS and PMOS devices.

(d) Simulate the I_d-V_g characteristics of the NMOS and PMOS devices with $|V_{ds}| = 1.8$V. Plot on a log-lin scale and calculate the sub-threshold slope of NMOS and PMOS devices. The subthreshold slope of MOSFET is given by S = n(kT/q)ln(10), where n is a geometry and technology dependent parameter.Calculate n from your simulations of 180 nm technology.

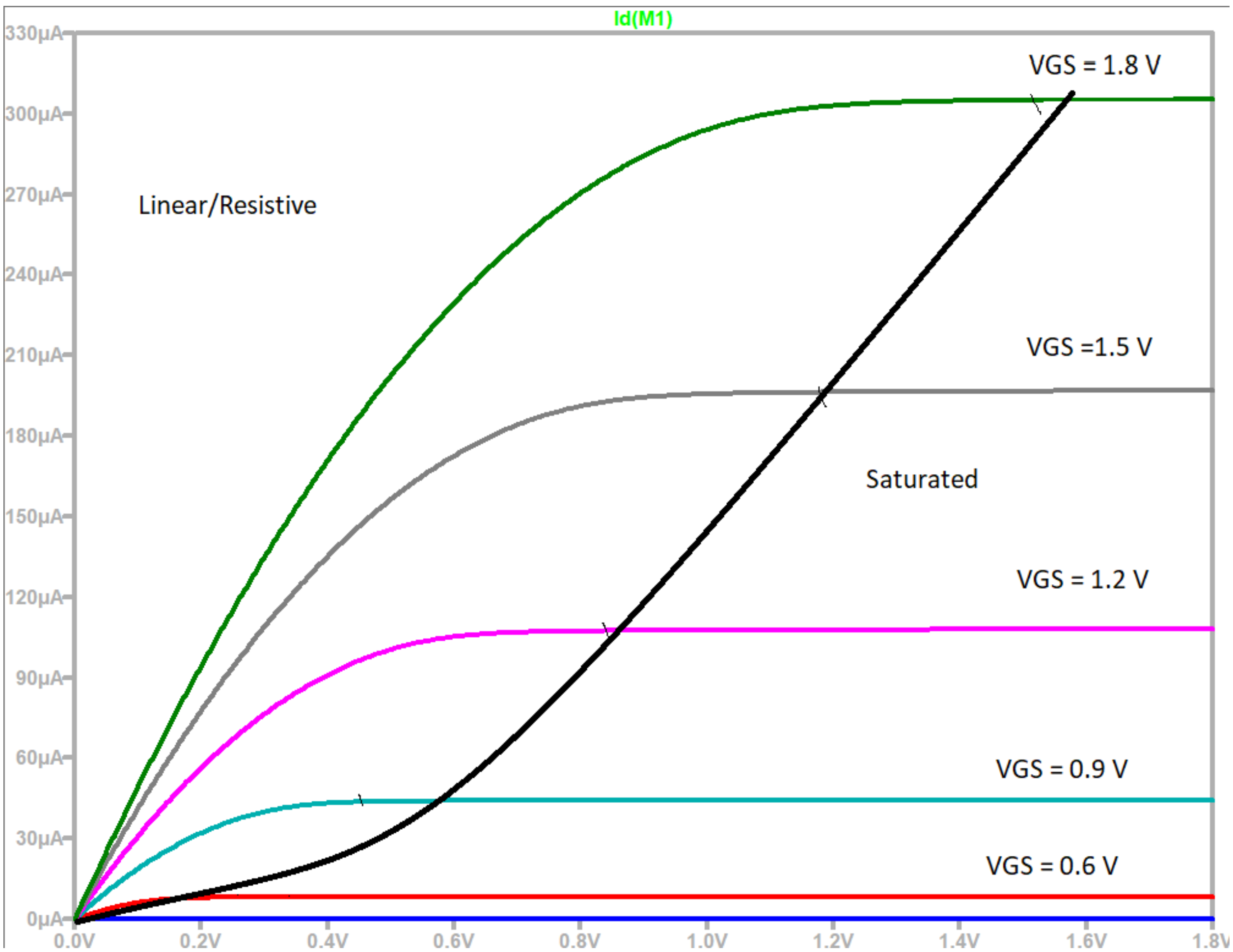
4.2 Spice Netlist

```
M1 N001 N002 0 0 nch_tt L = 10u, W= 15u
V1 N001 0 1
V2 N002 0 X
.model NMOS NMOS
.model PMOS PMOS
.lib C:standard.mos
.include "TSMC180.lib"
.dc V1 0 2.5 0.0001
.step param X 0 2.5 0.5
.backanno
.end
```

4.3 Solution

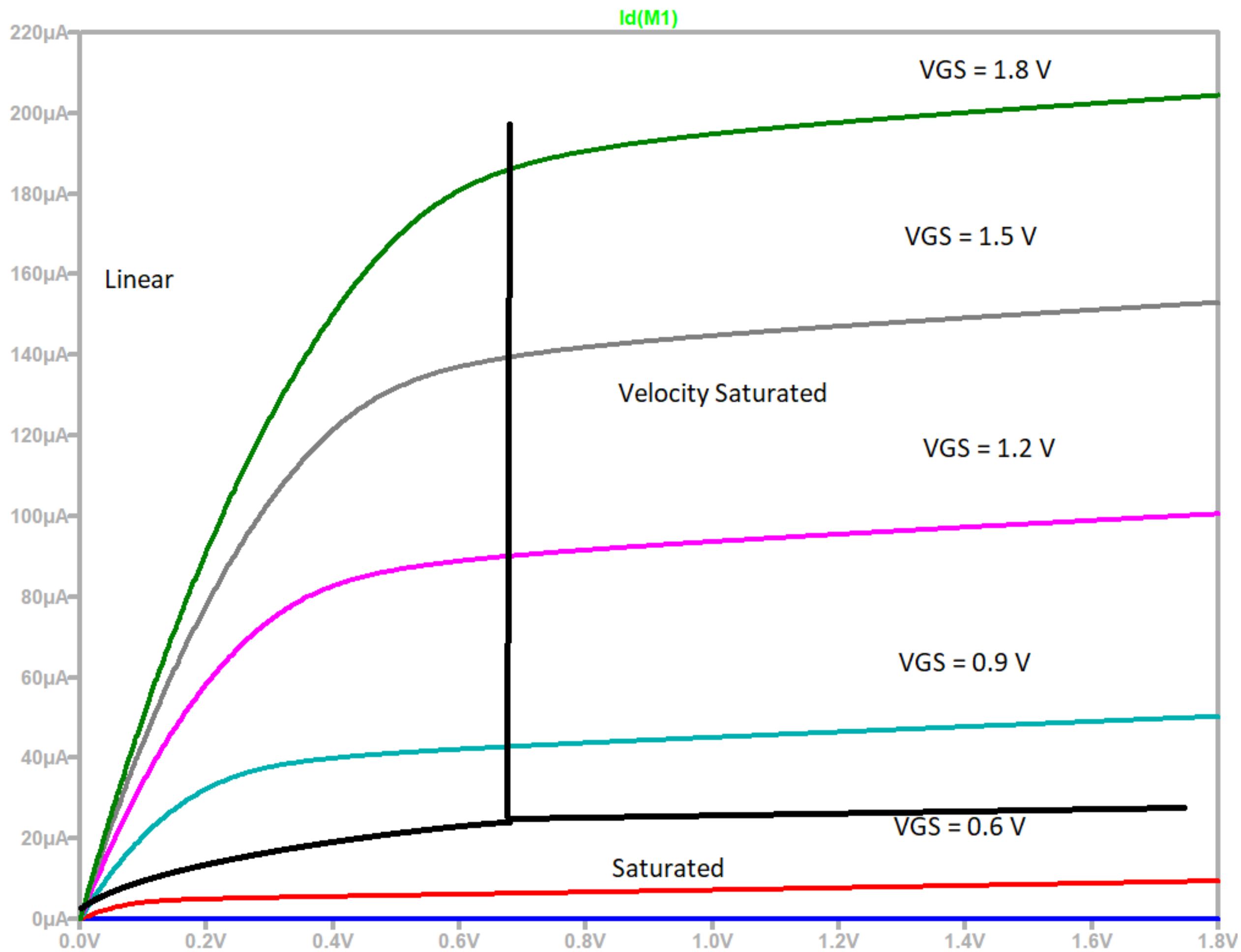
(a),(b)

Long channel NMOS



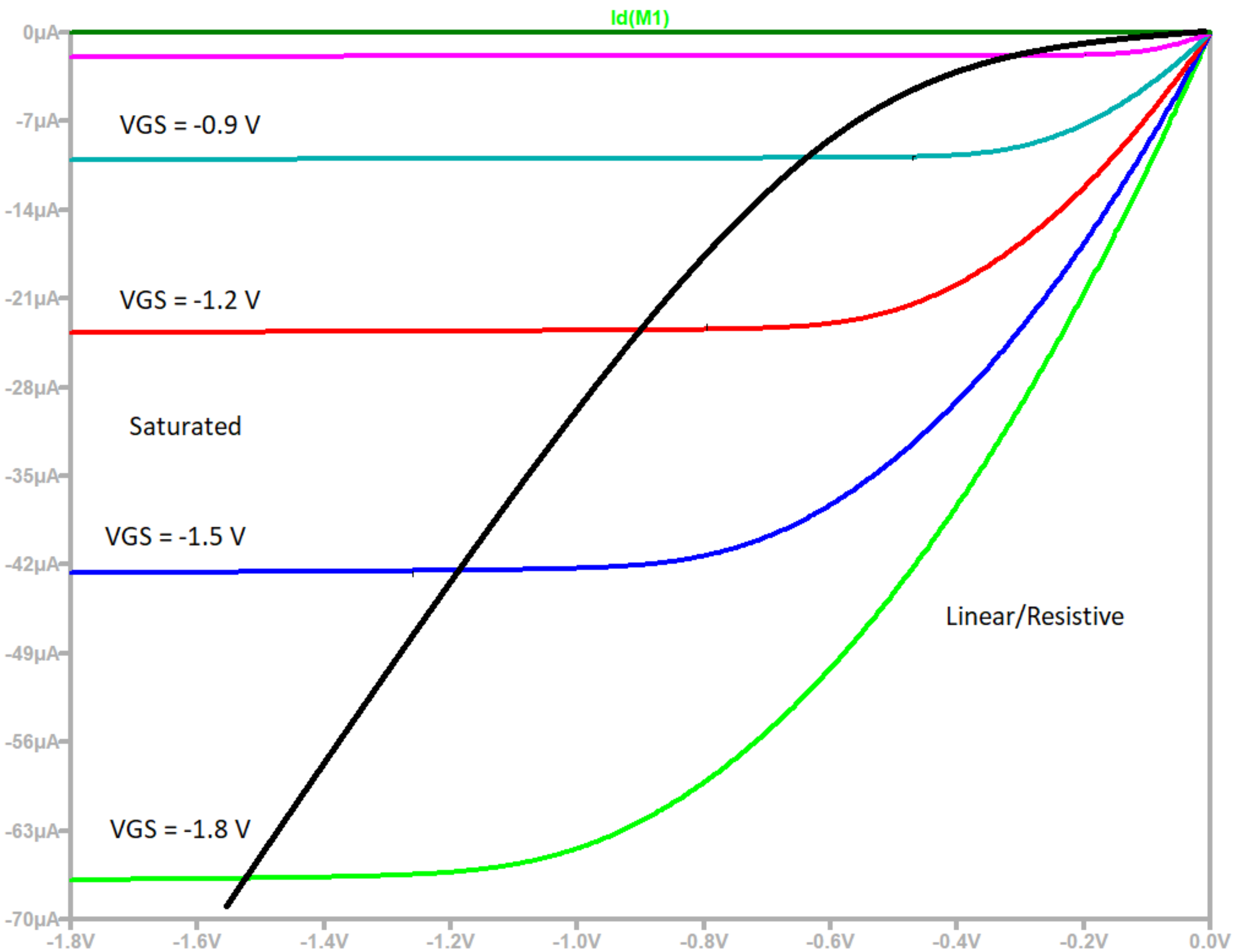
I-V Characteristics

Short channel NMOS



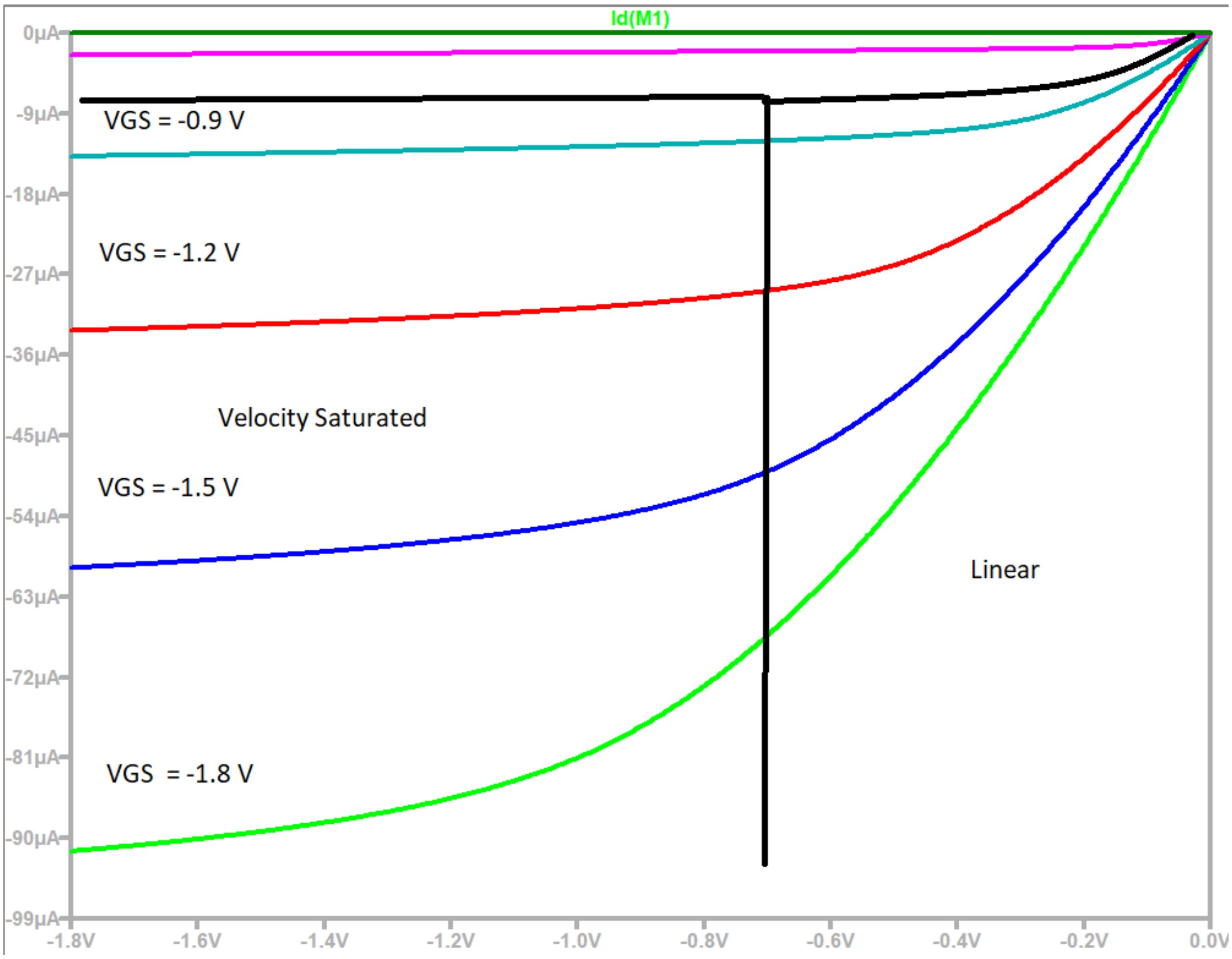
I-V Characteristics

Long channel PMOS



I-V Characteristics

Short channel PMOS



I-V Characteristics

- V_{GS} and I_{DS} linear dependence for short channel and quadratic for long channel.

(c)

The small signal output resistance is given by

$$R_o = \frac{\partial V_{DS}}{\partial I_{DS}} = \frac{1}{\lambda I_{DS}} \tag{14}$$

we will use $|V_{GS}| = |V_{DS}| = 0.9$ V for simulation and use the slope of I-V graph.

Long Channel NMOS

$$R_o = \frac{1}{slope} = \frac{1}{3.47882e^{-007}} = 2.8745M\Omega \tag{15}$$

Short Channel NMOS

$$R_o = \frac{1}{slope} = \frac{1}{6.94591e^{-006}} = 143.969K\Omega \tag{16}$$

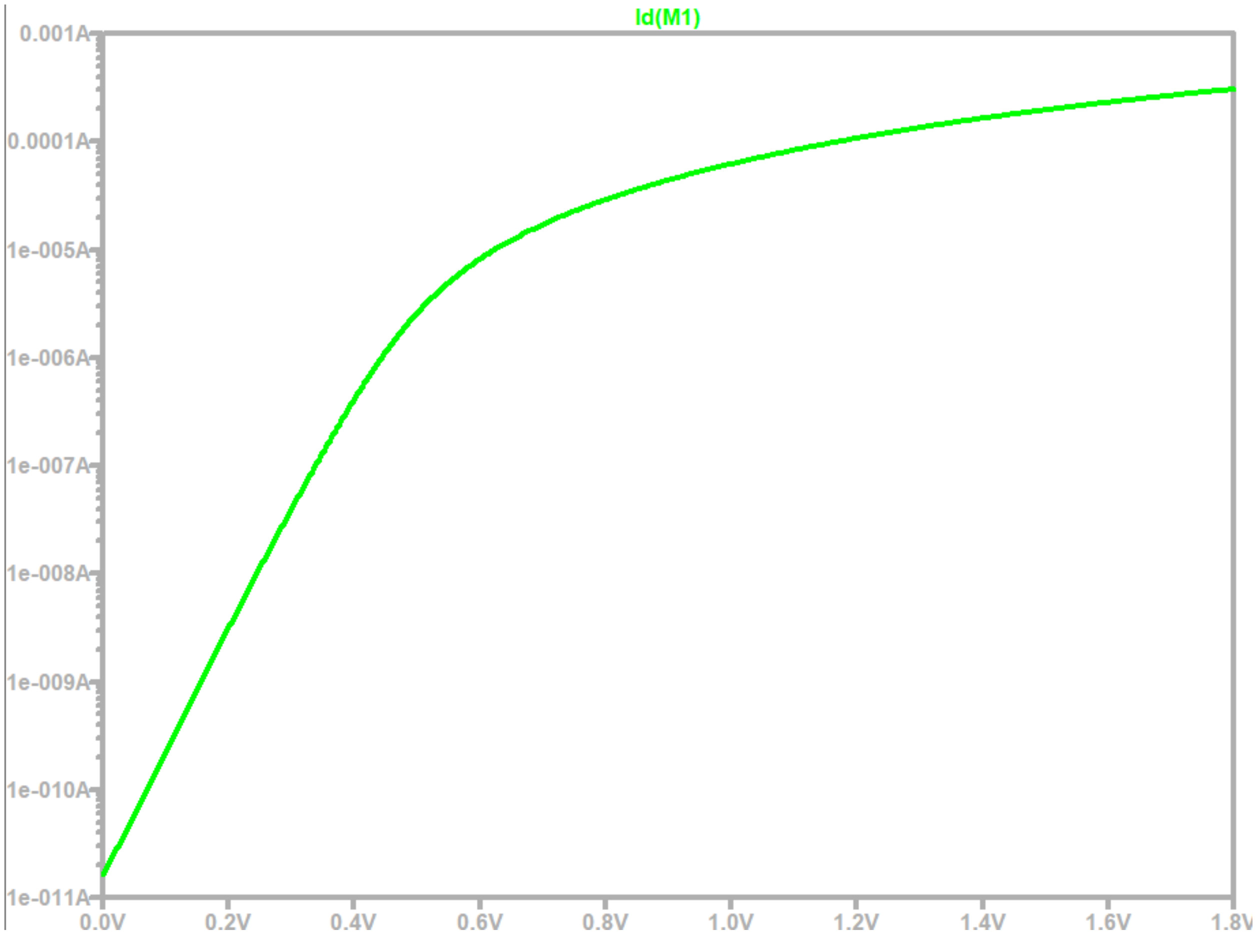
Long Channel PMOS

$$R_o = \frac{1}{slope} = \frac{1}{1.36379e^{-007}} = 7.3325M\Omega \tag{17}$$

Short Channel PMOS

$$R_o = \frac{1}{slope} = \frac{1}{2.02722e^{-006}} = 493.286K\Omega \tag{18}$$

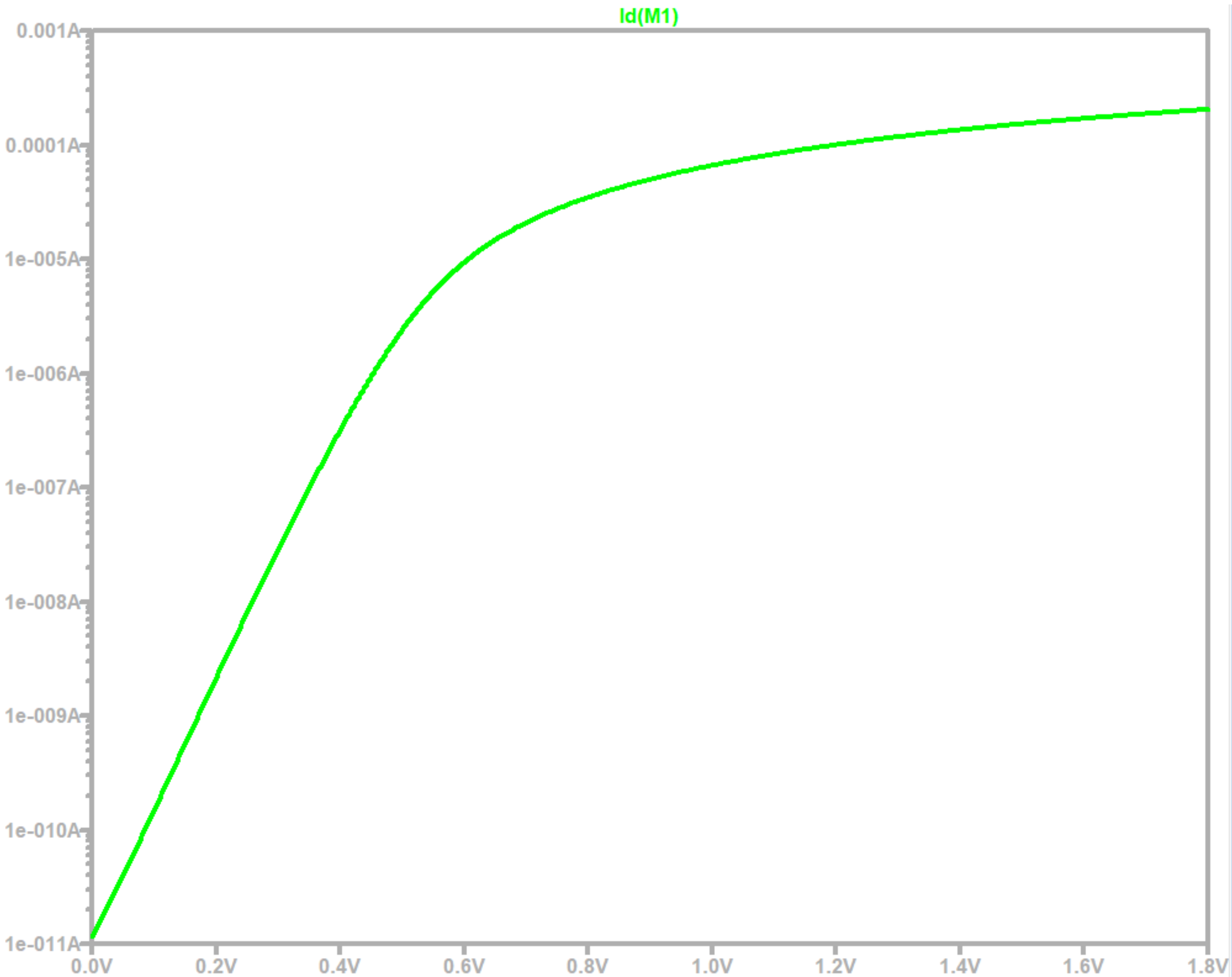
(d) **Long channel NMOS**



I_g-V_g (Log-lin scale) Characteristics

$$S = n(kT/q)ln(10) = 93.649238\ mV/decade \tag{19}$$

$$n = 1.5718 \tag{20}$$

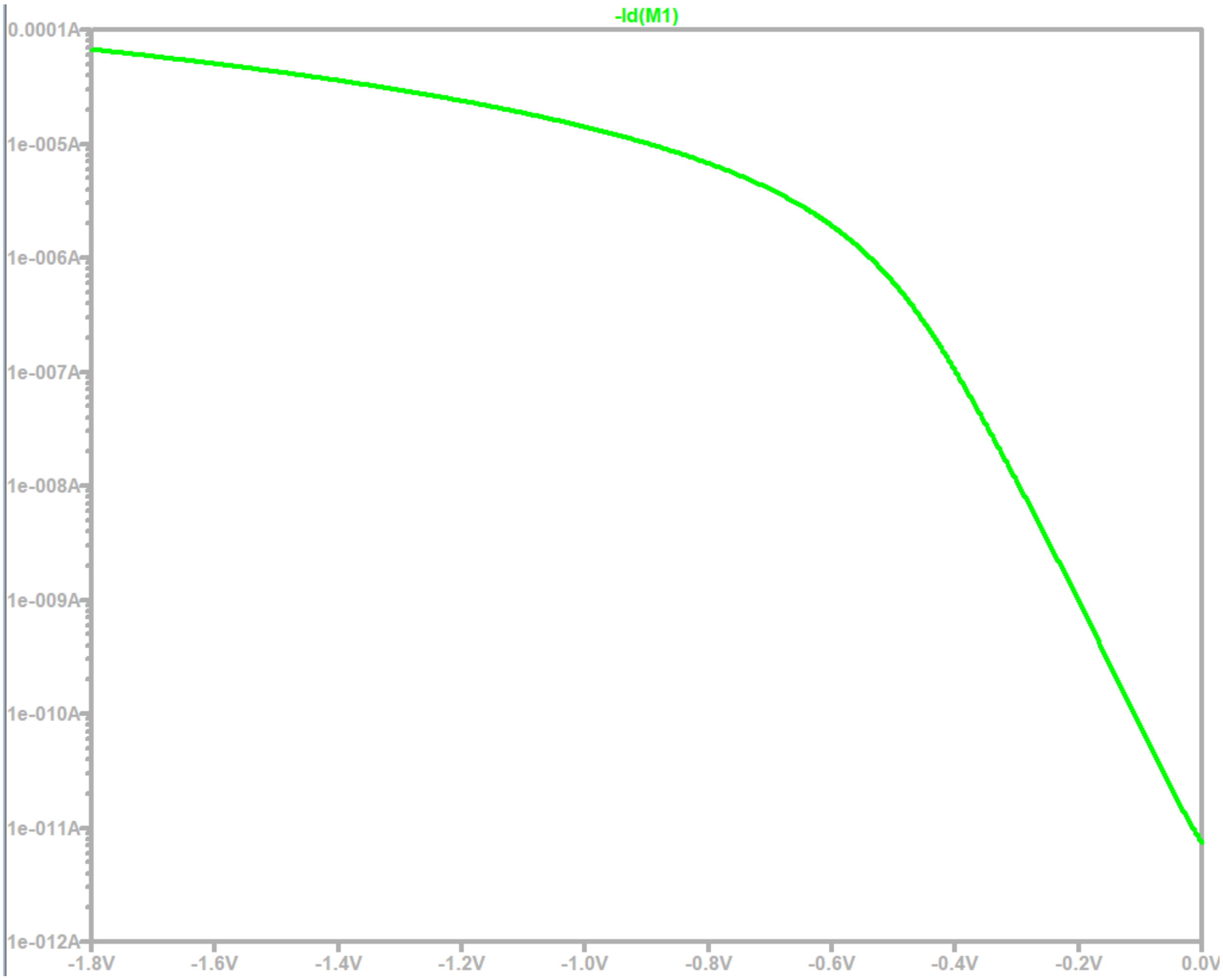


I_g-V_g (Log-lin scale) Characteristics

$$S = n(kT/q)ln(10) = 86.254869\ mV/decade \tag{21}$$

$$n = 1.44773 \tag{22}$$

Long channel PMOS

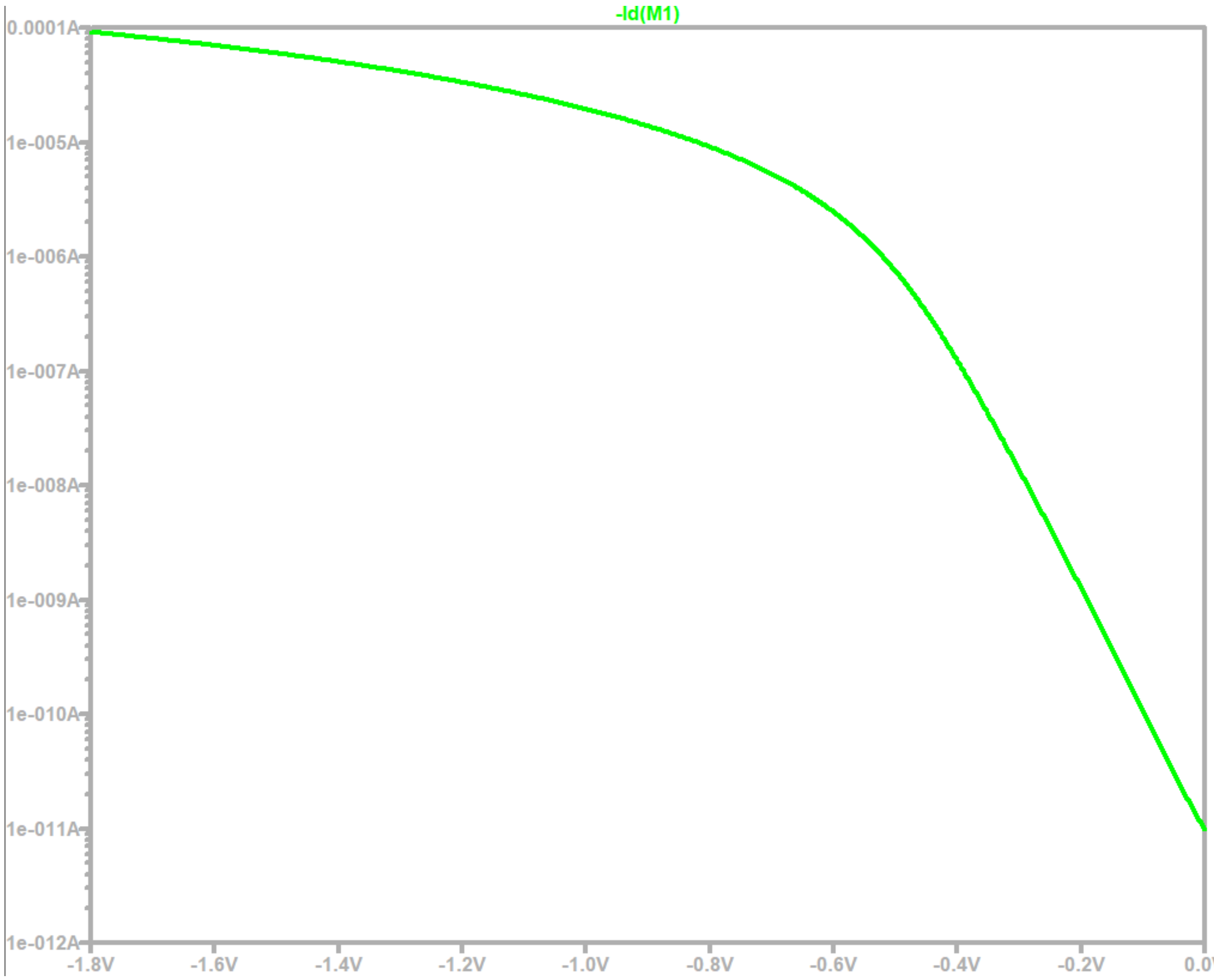


I_g-V_g (Log-lin scale) Characteristics

$$S = n(kT/q)ln(10) = 90.967742\ mV/decade \tag{23}$$

$$n = 1.5268 \tag{24}$$

Short channel PMOS



I_g-V_g (Log-lin scale) Characteristics

$$S = n(kT/q)ln(10) = 98.180816\ mV/decade \tag{25}$$

$$n = 1.6479 \tag{26}$$

5 Propagation Delay

5.1 Problem Statement

A first order RC circuit is frequently used to estimate the propagation delay in logic gates. In the class we have seen that the propagation delay for an ideal step input($t_{r,in}$ = 0) is t_p = 0.69RC. Further, the output rise time t_r = 2.2RC.

(a) Verify the expressions given above using SPICE simulations. Choose appropriate values for R and C components.

(b) Now consider a non-ideal step input with 10 ps $\leq$ $t_{r,in}$ $\leq$ 10 ns. Simulate the propagation delay, and plot t_p as a function of $t_{r,in}$.

(c) Arrive at an analytical (or empirical!) expression for propagation delay in presence of non-ideal step input.

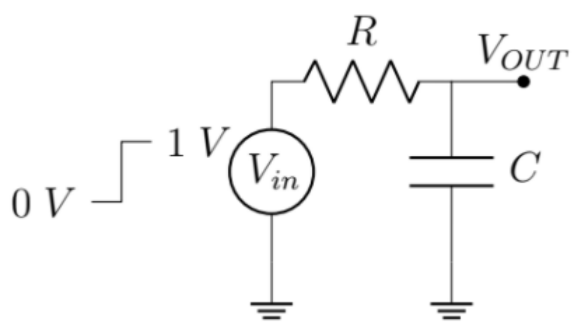


Figure 4

5.2 Spice Netlist

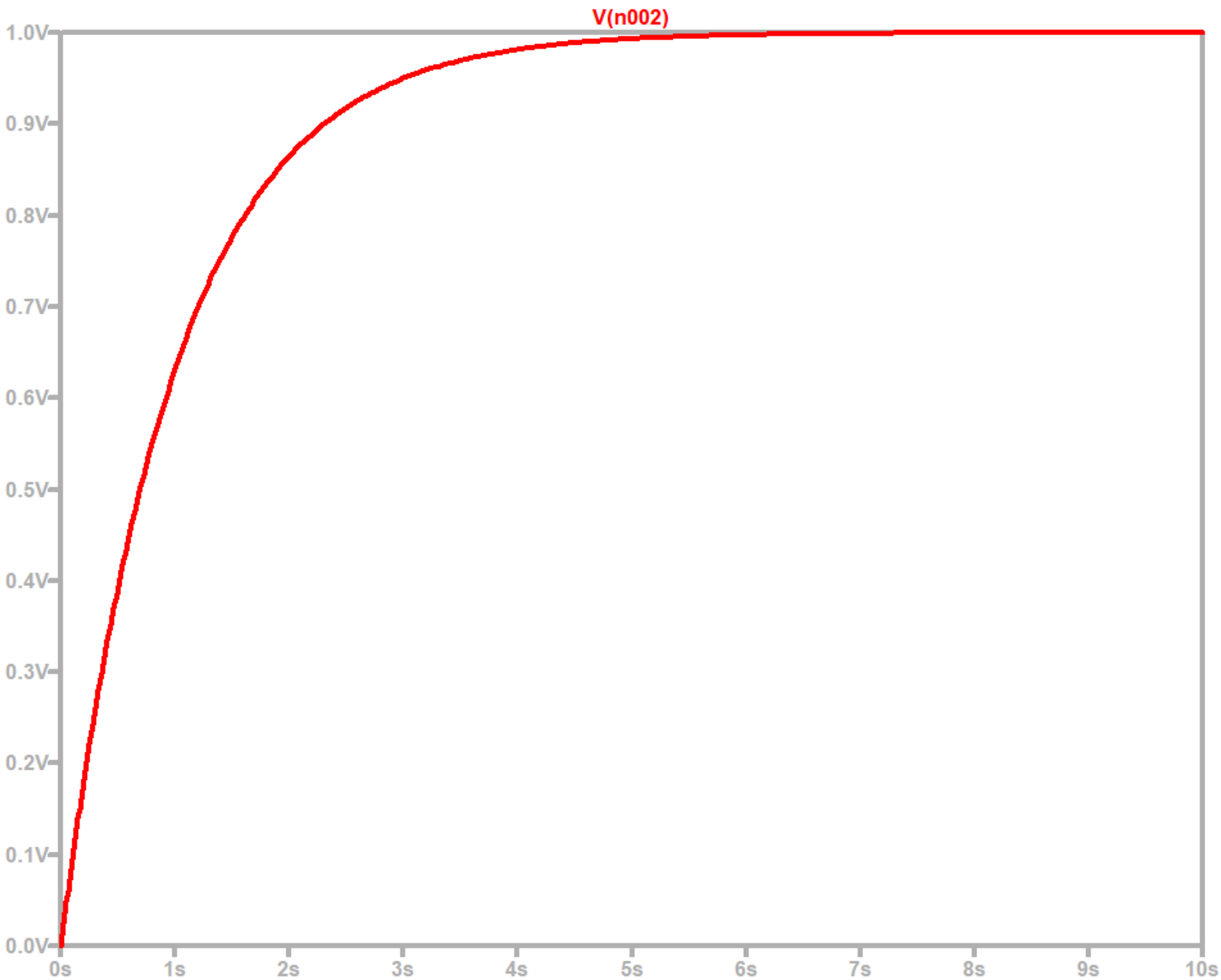
```
R1 N002 N001 1
C1 N002 0 1
V1 N001 0 PULSE(0 1 0 1p 1p 999 1000)
.tran 10
.backanno
.end
```

5.3 Solution

(a)

Here to use an ideal step We are taking RC >> Rise time.

Output Transient



V_{out} **Vs Time**

Propagation delay

Time taken for calculated at 50% of input-output transition i.e 0.5 V here.

Simulated Value = 0.691854 s

Ideal Propagation Delay = 0.69RC = 0.69s.

Rise Time

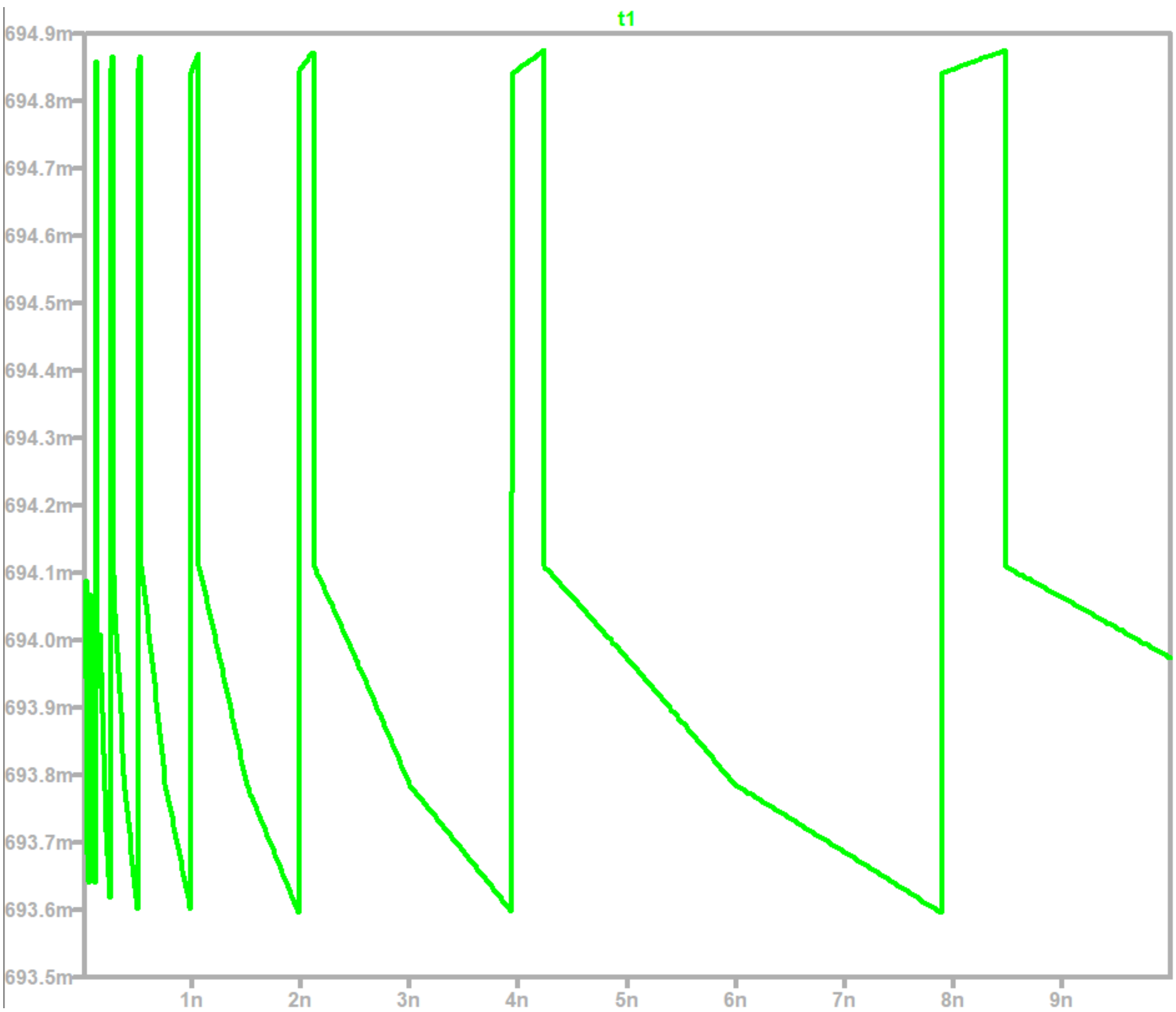
Time required for a pulse to rise from 10 per cent to 90 per cent of its steady value.

Simulated Value = 2.19806 s

Ideal Propagation Delay = 2.2RC = 2.2s.

(b)

Propagation Delay Vs Rise Time



t_p **vs** $t_{r,in}$

(c)

Now we will use two case, first 0 to Rise time and second from rise time to infinity.

$$V_{in} = \frac{t}{t_{r,in}} \tag{27}$$

$$V_{in} = RC\frac{dV_c}{dt} + V_c \tag{28}$$

$$\frac{dV_c}{dt} + \frac{V_c}{RC} = \frac{t}{RCt_r} \tag{29}$$

Multiplying $e^{\frac{t}{RC}}$ on Both sides.

$$e^{t/RC}dV_c + e^{t/RC}\frac{V_c}{RC}dt = \frac{V_{in}}{RC}dt \tag{30}$$

Integrating on Both sides

$$\int d(e^{t/RC}V_c) = \int \frac{V_{in}}{RC}dt \tag{31}$$

$$\int_0^t d(e^{t/RC}V_c) = \int_0^{tr} \frac{V_{in}}{RC}dt + \int_{tr}^t \frac{V_{in}}{RC}dt \tag{32}$$

$$e^{t/RC}V_c = 1 - \frac{RC}{t_r}(1 - e^{-\frac{tr}{RC}}) + e^{\frac{t}{RC}} - e^{\frac{tr}{RC}} \tag{33}$$

Now put t = t_p and $V_c = 0.5$

$$0.5e^{\frac{tp}{RC}} = \frac{RC}{t_r}(1 - e^{\frac{tr}{RC}}) \tag{34}$$

$$t_p = RCln\left(2\frac{(1 - e^{\frac{tr}{RC}})}{\frac{tr}{RC}}\right) \tag{35}$$


thank you