EE3301 : Introduction to VLSI Design
Homework Assignment 3

EE19BTECH11041,
Srijith Reddy Pakala
Department of Electrical Engineering
IIT Hyderabad

November 25, 2021

Contents

1 SRAM Operation **2**
1.1 Problem Statement 2
1.2 Spice Netlist 3
1.3 Solution 4

2 Impact of Sizing on Performance **6**
2.1 Problem Statement 6
2.2 Spice Netlist 6
2.3 Solution 7

1 SRAM Operation

1.1 Problem Statement

Static Random Access Memory (SRAM) is an important class of memory used in computers. Static refers to the fact that data is retained through feedback till the power is supplied. SRAM is faster and more expensive than Dynamic Random Access Memory (DRAM)1, and it is used in cache and registers. A standard SRAM cell consists of two cross coupled inverters which have two stable states Q and $\overline{Q}$ to denote 0 and 1. M5 and M6 are the access transistors enabled by the wordline(WL) and connected to bitline(BL) and $\overline{BL}$. The sizing of the transistors should be such that the state is weak enough to be overpowered during a write, and yet strong enough not be disturbed during a read. We will discuss the SRAM sizing later in the course.

(a) Implement the SRAM cell in SPICE with the following parameters: Pull down transistors M1 and M3 are of size 8/2λ, pull up transistors M2 and M4 are of size 3/3λ, and access transistors M5 and M6 are of size 4/2λ (where λ = 90; nm in 180 nm technology).

(b) Verify the read operation by initializing Q and $\overline{Q}$ to be 0 and 1 respectively. set both bitlines (BL and $\overline{BL}$) to be floating 1. Verify that when the WL is enabled BL will switch to zero.

(c) Verify the write operation by assuming Q = 0 and $\overline{Q}$ = 1 initially. Set BL = 1 and $\overline{BL}$ = 0. Verify that when WL is enabled Q will be overwritten from 0 to 1.

(d) Estimate the maximum operating speed of the SRAM?

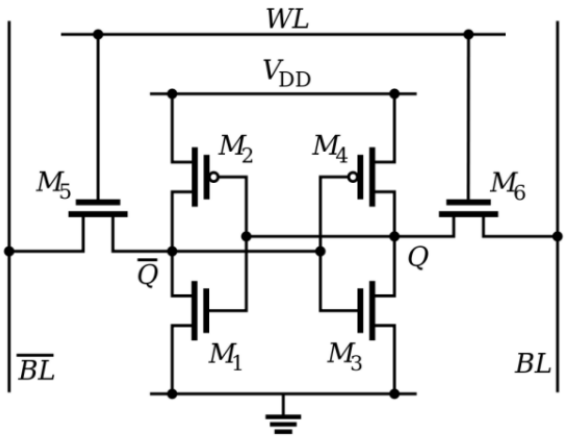


Figure 1

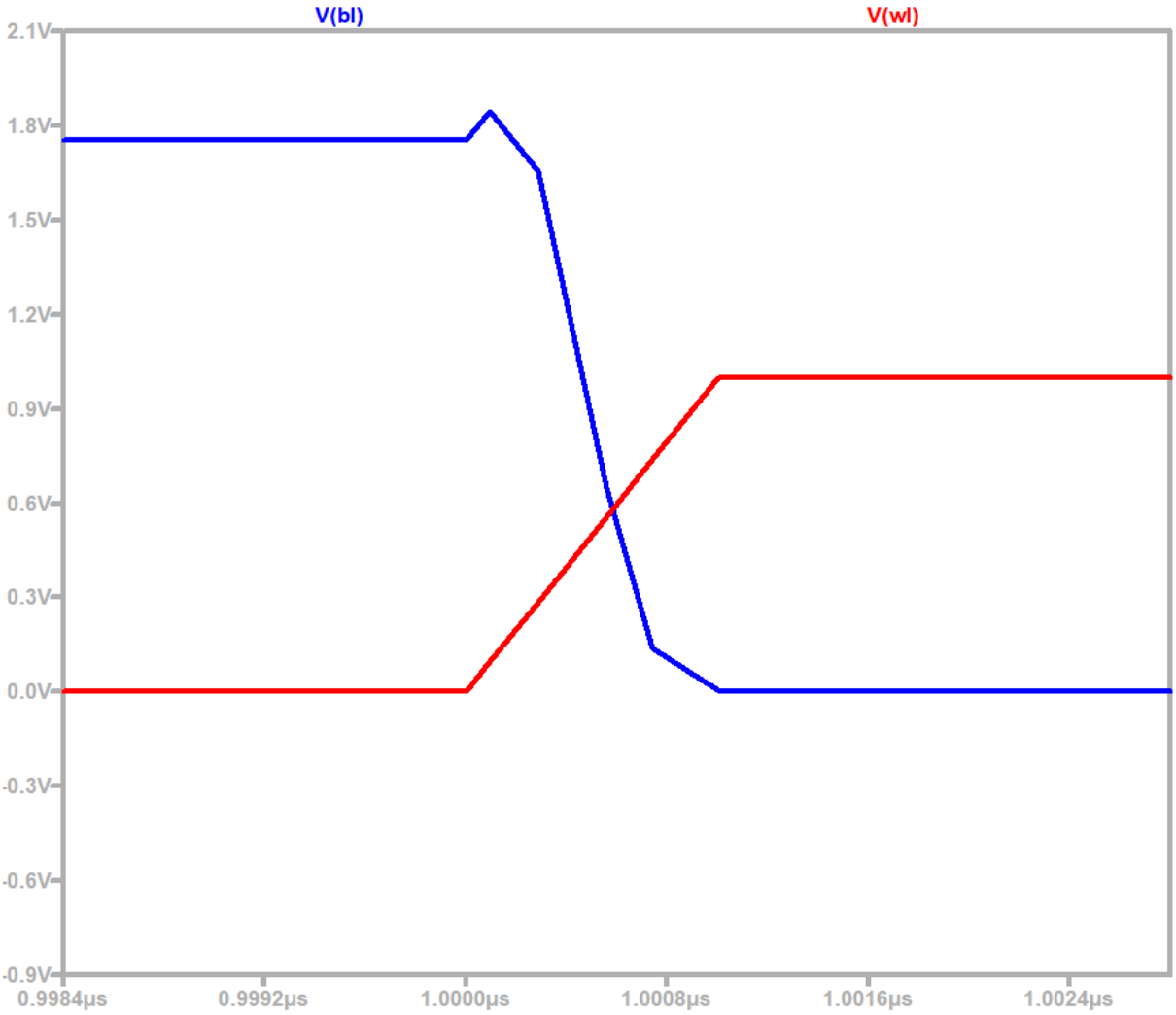
1.2 Spice Netlist

```
M2 Qbar Q VDD VDD pch_tt W = 270n,L=270n
M4 Q Qbar VDD VDD pch_tt W = 270n,L=270n
M1 Qbar Q 0 0 nch_tt W = 720n,L=180n
M3 Q Qbar 0 0 nch_tt W = 720n,L=180n
V1 VDD 0 1.8
M5 Qbar WL BLbar BLbar nch_tt W = 360n,L=180n
M6 BL WL Q Q nch_tt W = 360n,L=180n
V2 WL 0 PULSE(0 1 1u 1n 1n 1u 2u)
.model NMOS NMOS
.model PMOS PMOS
.lib C:standard.mos
.include "TSMC180.lib"
.tran 2u
.ic V(q) = 0 V(qbar) = 1.8 V(bl) = 1.8 V(blbar) = 1.8
.backanno
.end
```

1.3 Solution

(b)

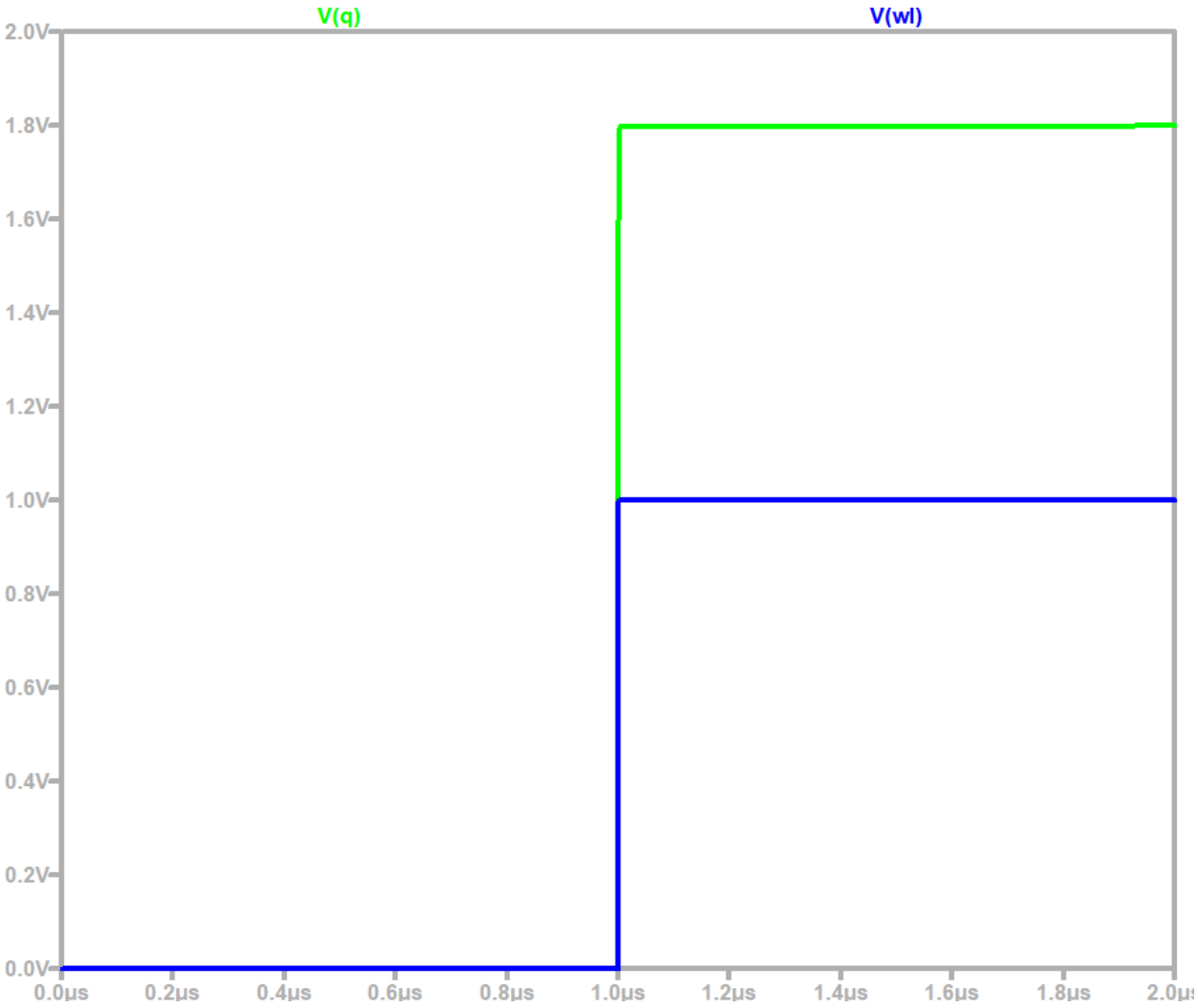
Verify READ



WL and BL

(c)

Verify WRITE



WL and Q

(d)

Using the time delay in write mode the maximum operating speed is 7GHz.

2 Impact of Sizing on Performance

2.1 Problem Statement

Design and implement an inverter such that $V_M = V_{DD}/2$.

(a) Investigate the impact of scaling factor S ≥ 1 (both NMOS and PMOS sizes are increased by a factor S) on the performance of inverter in (i) no external load, and (ii) C_L = 20pF conditions. Tabulate your results.

(b) What is the impact of increasing W_p or W_n on t_{pHL} and t_{pLH}? Substantiate your answer by performing simulations and tabulating results.

2.2 Spice Netlist

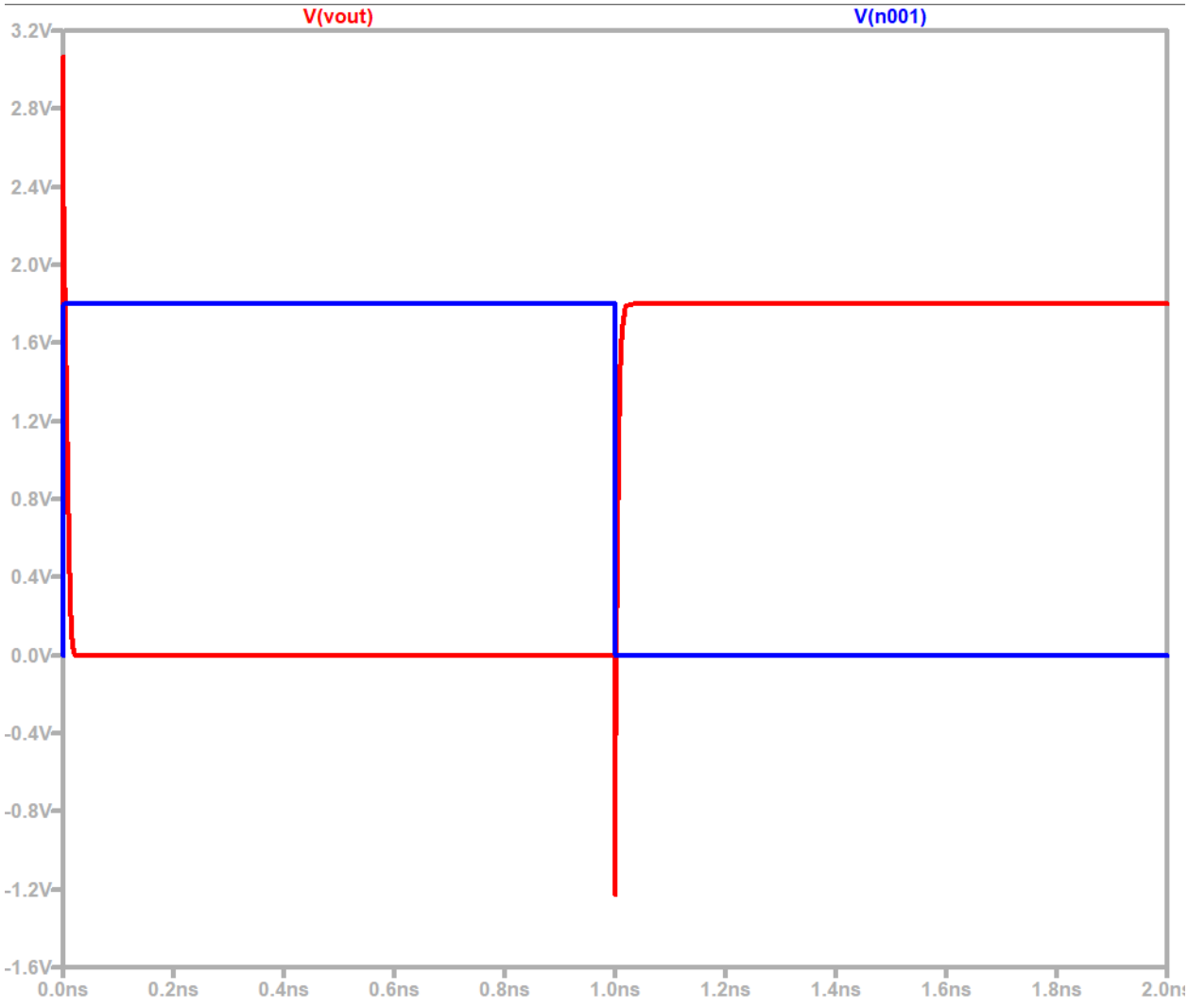
```
M1 Vout N001 0 0 nch_tt W=S*0.18u,L = 0.18u
M2 Vout N001 VDD VDD pch_tt W =S*0.97u,L=0.18u
V1 VDD 0 1.8
V2 N001 0 PULSE(0 1.8 0 1f 1f 1n 2n)
.model NMOS NMOS
.model PMOS PMOS
.lib C:standard.mos
.include "TSMC180.lib"
.tran 2n
.meas tpHL TRIG V(n001)=0.9 RISE=1 TARG V(vout)=0.9 FALL=1
.meas tpLH TRIG V(n001)=0.9 FALL=1 TARG V(vout)=0.9 RISE=1
.meas tp PARAM (tpLH+tpHL)/2
.step param S 1 10 1
.backanno
.end
```

2.3 Solution

V_{DD}= 1.8V and V_M =0.9 V. By trial and error to get VM=VDD/2 the design parameters obtained at S=1 are: $\beta = 5.39 = 0.97/0.18$.

(a)
(i)

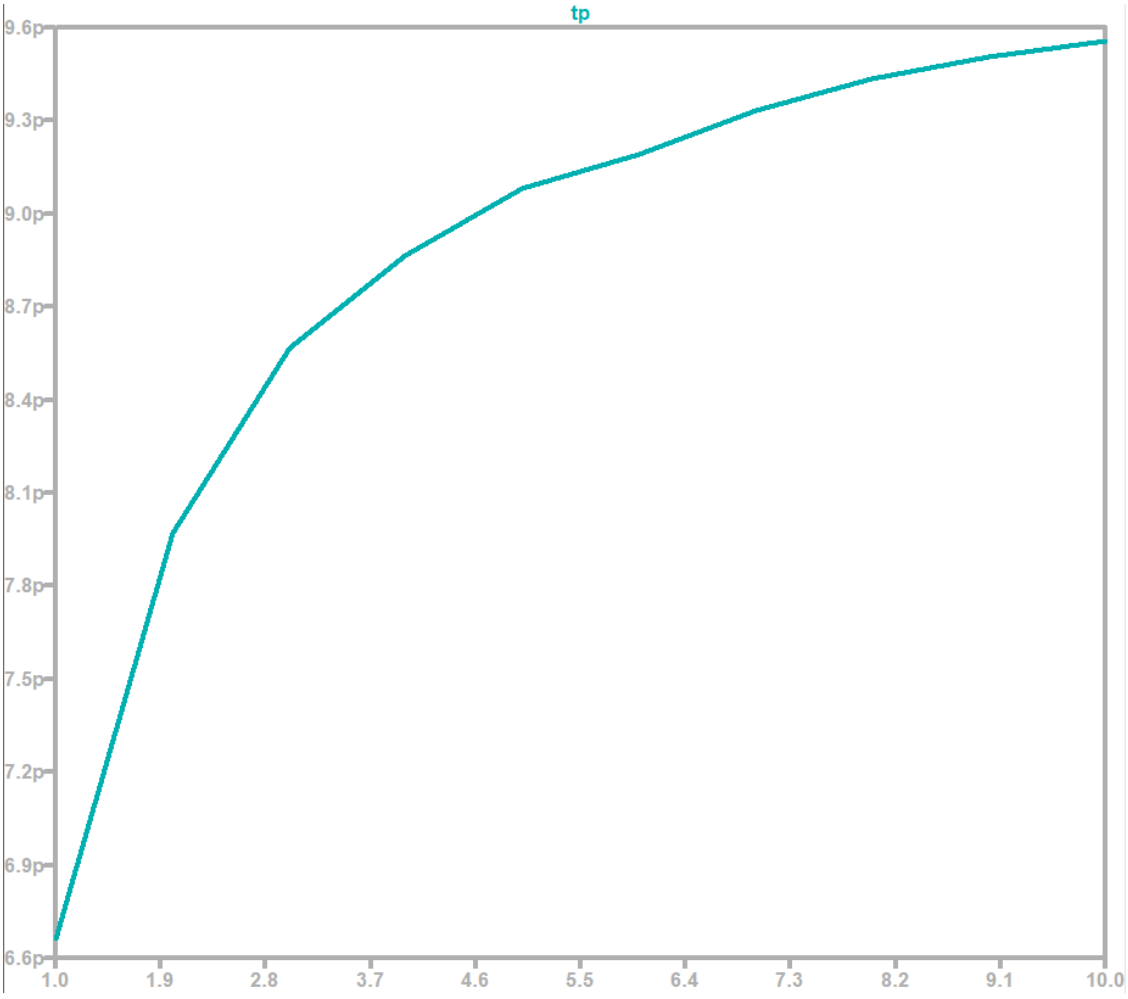
No external Load



V_{in} and V_{out} at S=1

- tp = 6.66 psec at S = 1

S	tpLH (psec)	tpHL (psec)	tp (psec)
1	5.32	8	6.66
2	5.62	10.3	7.97
3	5.82	11.3	8.56
4	5.85	11.8	8.86
5	5.94	12.2	9.08
6	5.89	12.4	9.19
7	5.98	12.6	9.33
8	6.02	12.8	9.43
9	6.04	12.9	9.5
10	6.04	13.0	9.55

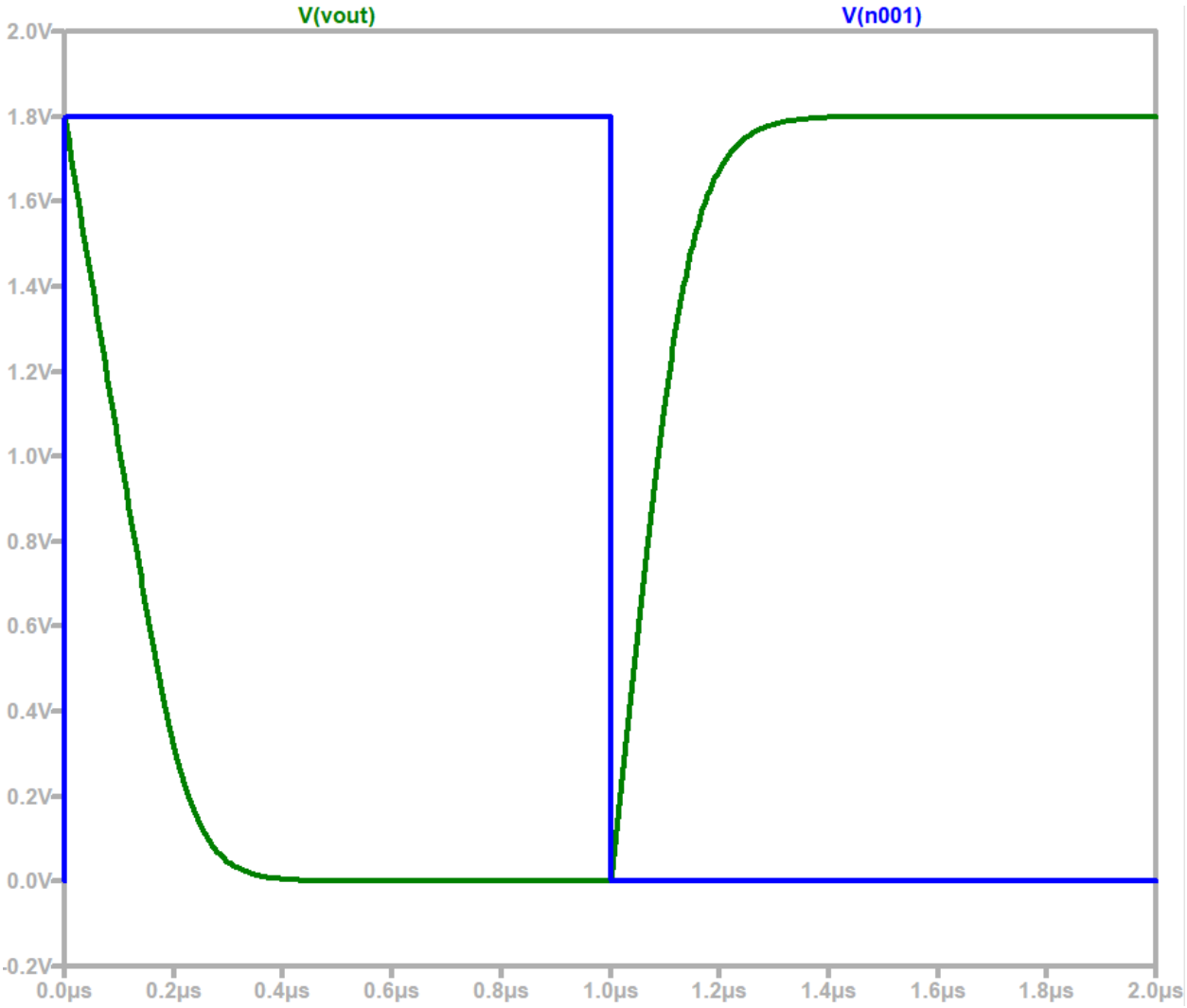


t_p Vs S (No external Load)

.• The propagation delay is almost constant in the absence of external load.

(ii)

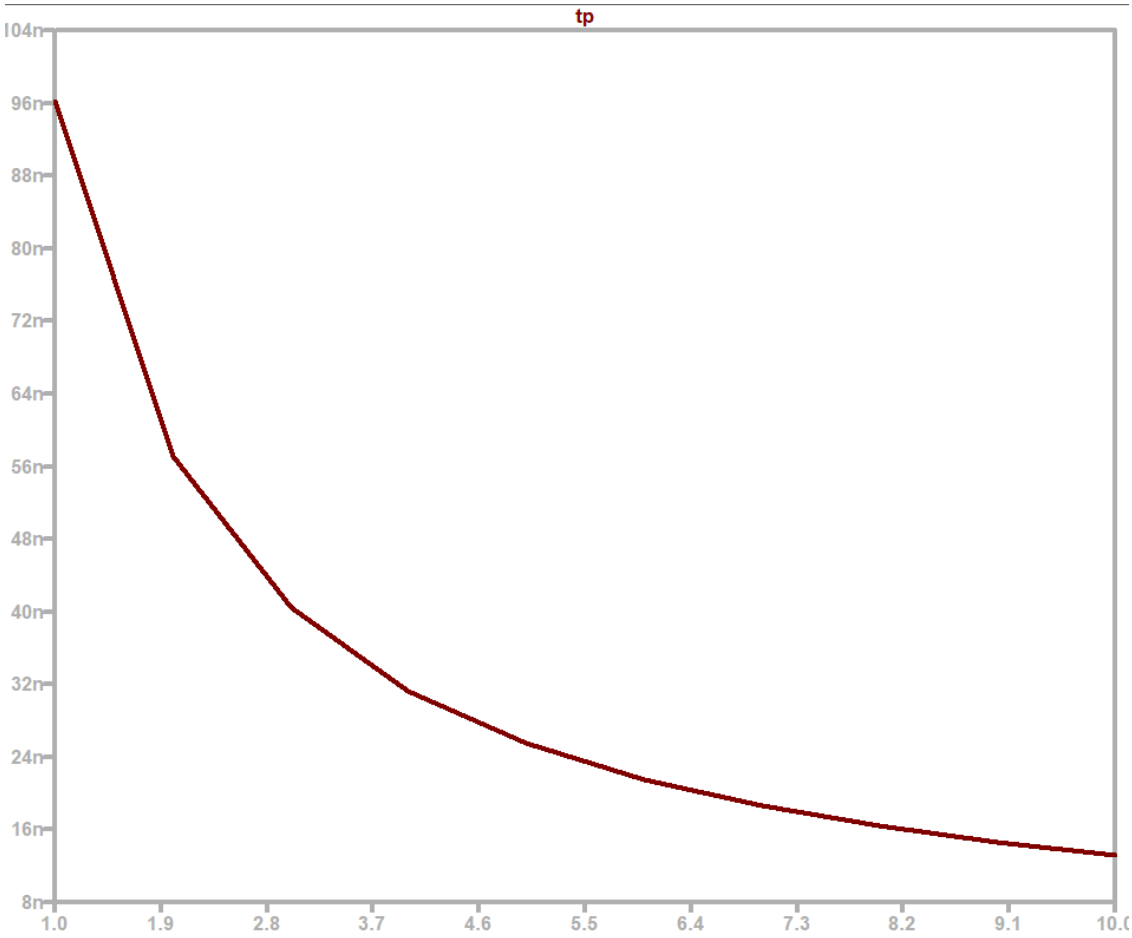
When C_L = 20pF



V_{in} and V_{out} at S=1

- tp = 96 nsec at S = 1

S	tpLH (nsec)	tpHL (nsec)	tp (nsec)
1	77.1	115.2	96.2
2	40.4	73.7	57.1
3	27.3	53.4	40.4
4	20.6	41.8	31.2
5	16.5	34.3	25.4
6	13.8	29.1	21.5
7	11.9	25.3	18.6
8	10.4	22.3	16.3
9	9.29	20	14.6
10	8.38	18.1	13.2



t_p Vs S (No external Load)

.• The propagation delay decreases with scaling in presence of capacitance.

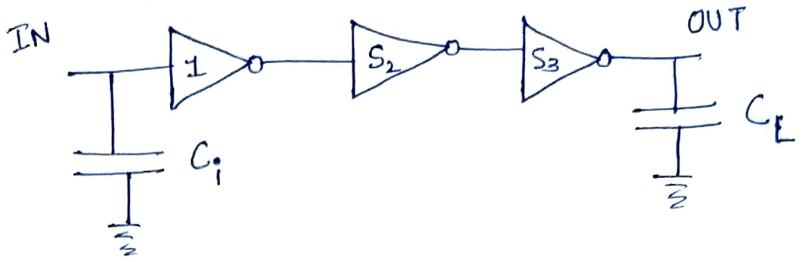
(b) If we increase W_p, β increases. Therefore we seeing the impact of changing β here.

W_p	W_n	t_p (nsec)
0.97u	0.18u	6.9
1.07u	0.18u	7.25
1.17u	0.18u	7.65
1.27u	0.18u	8.08
1.37u	0.18u	8.43
1.47u	0.18u	8.93
1.57u	0.18u	9.27
1.67u	0.18u	9.51
1.77u	0.18u	10.04
1.87u	0.18u	10.2

.• As β increases, Propagation delay t_p increases.

Sizing of Inverters

(3) Given $C_i = 10fF$, $C_L = 20pF$, $t_{p_0} = 70ps$,



(a) $\gamma \approx 1$ $\quad F = \frac{C_L}{C_i} = 2000$, $N = 3$

$$f = \sqrt[N]{F} = \sqrt[3]{2000} = 12.599$$

$$S_1 = 1, \quad S_2 = f = 12.599 , \quad S_3 = f^2 = 158.74$$

$$t_p = t_{p_0} N \left[1 + \frac{f}{\gamma} \right] = 70p \times 3 \times (13.599)$$

$$\boxed{t_p = 2.855n}$$

(b) To acheive minimum delay we can change no of stages

At minimum t_p.

$$f = e^{\left(1 + \frac{\gamma}{f}\right)} = e^{\left(1 + \frac{1}{f}\right)}$$

$$f = 3.591 \approx 3.6$$

(3)

(b)

$$N = \frac{\ln(F)}{\ln(f)} = \frac{\ln(2000)}{\ln(3.6)} = 5.9454 \approx 6$$

If we don't need inverted output we can use N=6

N=6

$$t_p = N t_{p_0}\left(1 + \frac{f}{\gamma}\right) = 6 \times 70p\left(4.6\right) = 1.932ns$$

If we need to have only inverted output we can use N=5

Since N=5 is odd.

N=5

$$t_p = N t_{p_0}\left(1 + \frac{f}{\gamma}\right) = 5 \times 70\ (5.57) = 1.95ns$$

$$f = \sqrt[5]{2000} = 4.573$$

(c) Incase (b) delay is less but requires more area. compared to (a).

(3) (d)

Dynamic power $= C_{Total} V_{DD}^2 \, freq$

Here $C_{Total} = \sum C_i$

$= C_1 + C_2 + \cdots C_N$

$= (C_i + fC_i + f^2 C_i + C_L)$

$= C_i \dfrac{(f^4 - 1)}{(f - 1)}$

$freq = \dfrac{1}{2 t_p} = \dfrac{1}{2 \times 2.855 \times 10^{-9}} =$ 175 MHz

$P_{Dynamic} = C_i V_{DD}^2 \dfrac{(f^4 - 1)}{(f - 1)} \times \dfrac{1}{2N^2 t_{p_0}\left(1 + \frac{f}{\gamma}\right)}$

$= 10 \times 10^{-15} \times (2.5)^2 \times (175.33) \times 10^6 \times \dfrac{((12.6)^4 - 1)}{(11.6)}$

$P_{Dynamic} = 24.39 \text{ mW}$

CMOS LOGIC

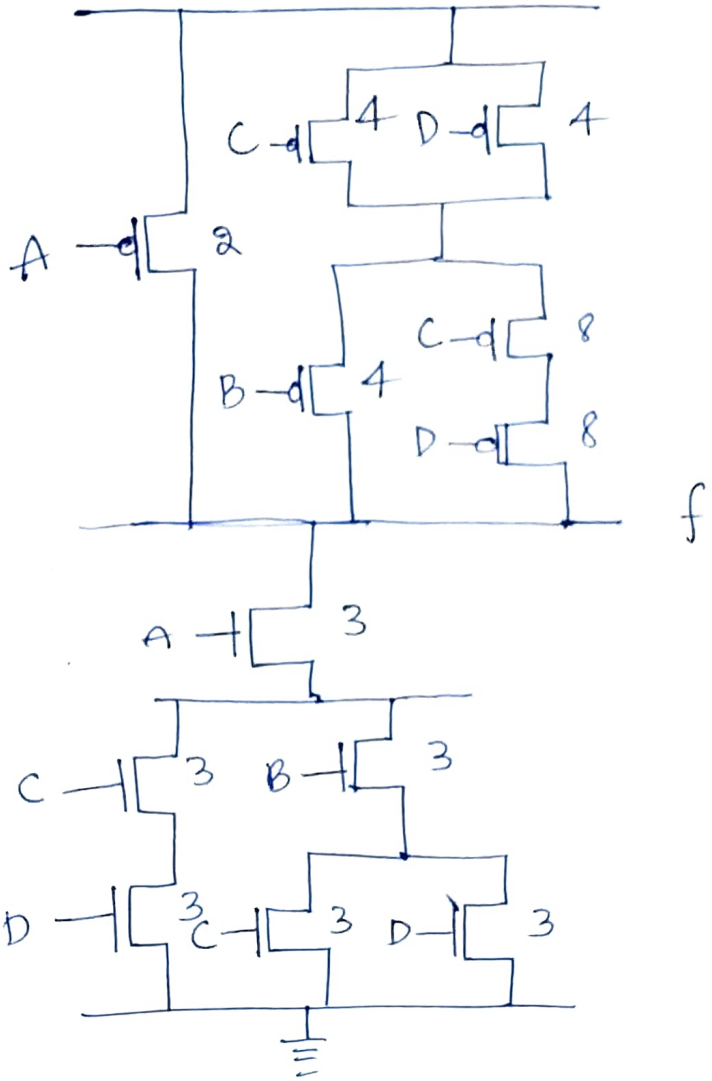
(4) Given $f(A;B:C:D) = \overline{A.(B.(C+D)+C.D)}$

$L_{min} = L_N = L_p = 180nm / 250nm$

$R_p = 2R_N$ for same drive length.

Now we will multiply W_p or W_N to make optimal use.

CMOS LOGIC



The number beside NMOS & PMOS represents width scale.

Worst case scenario : $t_{pHL} = t_{pLH} = 0.69 R_N C_L$.

(5)

CMOS Inverter

Given $V_{t,n} = 0.2V$, $|V_{tp}| = 0.3V$.

$R_n = 2K\Omega * \mu m$, $R_p = 3K\Omega * \mu m$, $V_{DD} = 1V$

$W_p = W_n = 1\mu m$

NMOS ON: $R_{ON,n} = \frac{R_n}{W_n} = 2K\Omega$

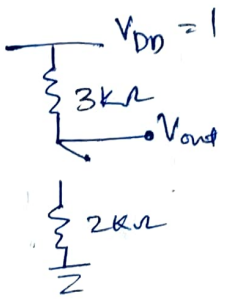
PMOS ON: $R_{ON,p} = \frac{R_p}{W_p} = 3K\Omega$

Region ①

$0 < V_{in} < V_{t,n}$

PMOS → ON

NMOS → $V_{gs} < V_{tn}$ → OFF



$V_{out} = V_{DD} = 1$

Region ②:

$V_{t,n} < V_{in} < V_{DD} - |V_{tp}|$

PMOS → ON

NMOS → ON

$V_{out} = \frac{R_{ON,N} V_{DD}}{R_{ON,P}}$

$V_{out} = 0.4V$

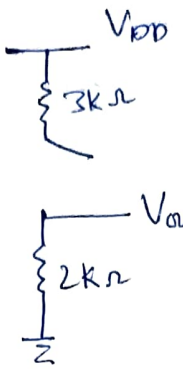
(5)

Region (3)

$V_{in} > V_{DD} - |V_{tp}| = 0.7V$

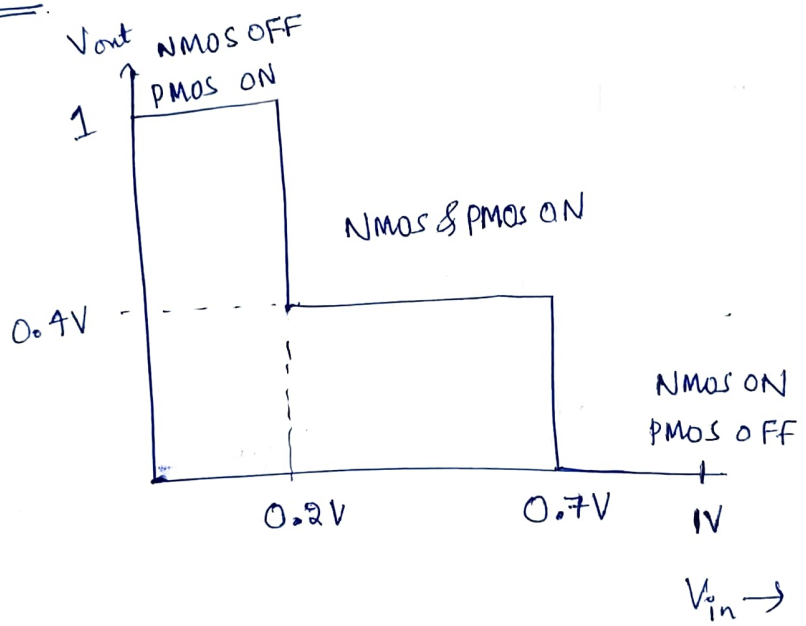
PMOS → $V_{sg} < |V_{tp}|$ → OFF

NMOS → ON



$V_{out} = 0V$

VTC



..

* THE END *