EE3301 : Introduction to VLSI Design
Homework Assignment 2

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November 9, 2021

Contents

1 MOSFET Resistance

1.1 Problem Statement

The MOSFET output small signal resistance is defined by the slope of the I_D - V_D characteristics. However, in digital circuits we are often interested in equivalent resistance presented by the MOSFET during charging/discharging of a capacitor (see example 3.8 of your textbook). In this exercise you will run simulations to determine the equivalent resistance of the regular NMOS and PMOS transistors in 0.18 μm process as a function of V_{DS}.

(a) Perform a transient simulation of the circuit in Figure 1 using W/L = 240/180 or W/L = 400/180 and V_{DD} = 1.8 V . Set the initial voltage across the capacitor to be 1.8 V . You should submit plots of Req as a function of V_{DS} for NMOS and PMOS devices (c. f. Figure 3.27 of course textbook). Note: For PMOS devices you need to modify the circuit.

(b) Compare your answers with Table 3.3 of text- book and explain the differences.

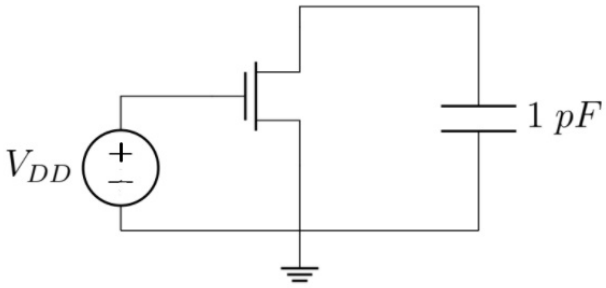


Figure 1

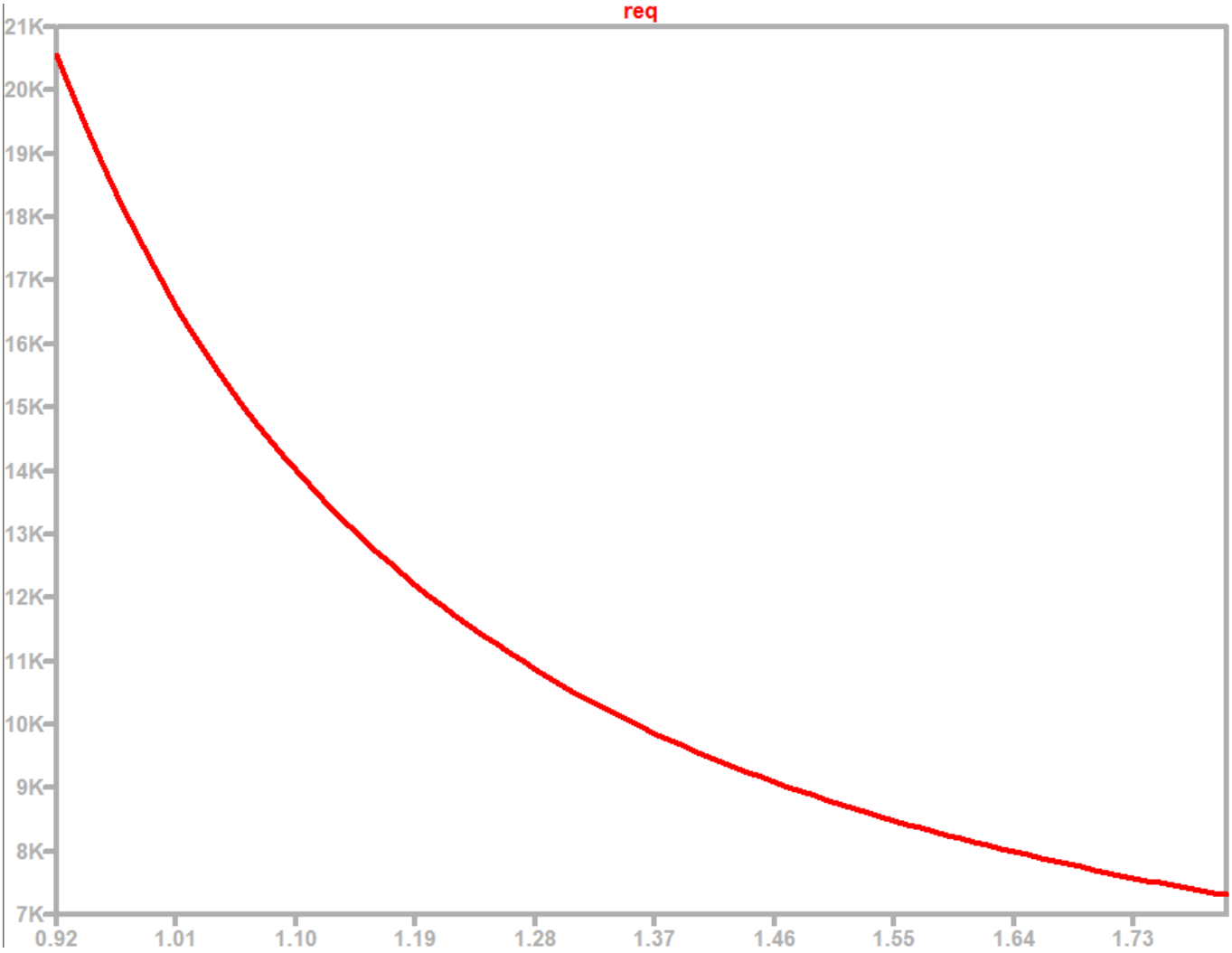
1.2 Spice Netlist

```
M1 N001 N002 0 0 nch_tt L = 0.18u,W = 0.24u
C1 N001 0 1p
V1 N002 0 X
.model NMOS NMOS
.model PMOS PMOS
.lib C:standard.mos
.include "TSMC180.lib"
.ic V(n001)=X
.step param X 0.5 1.8 0.01
.meas TRAN Req AVG (V(n001)/Id(M1)) TRIG time=0 TARG V(n001)=X/2
.tran 1u
.backanno
.end
```

1.3 Solution

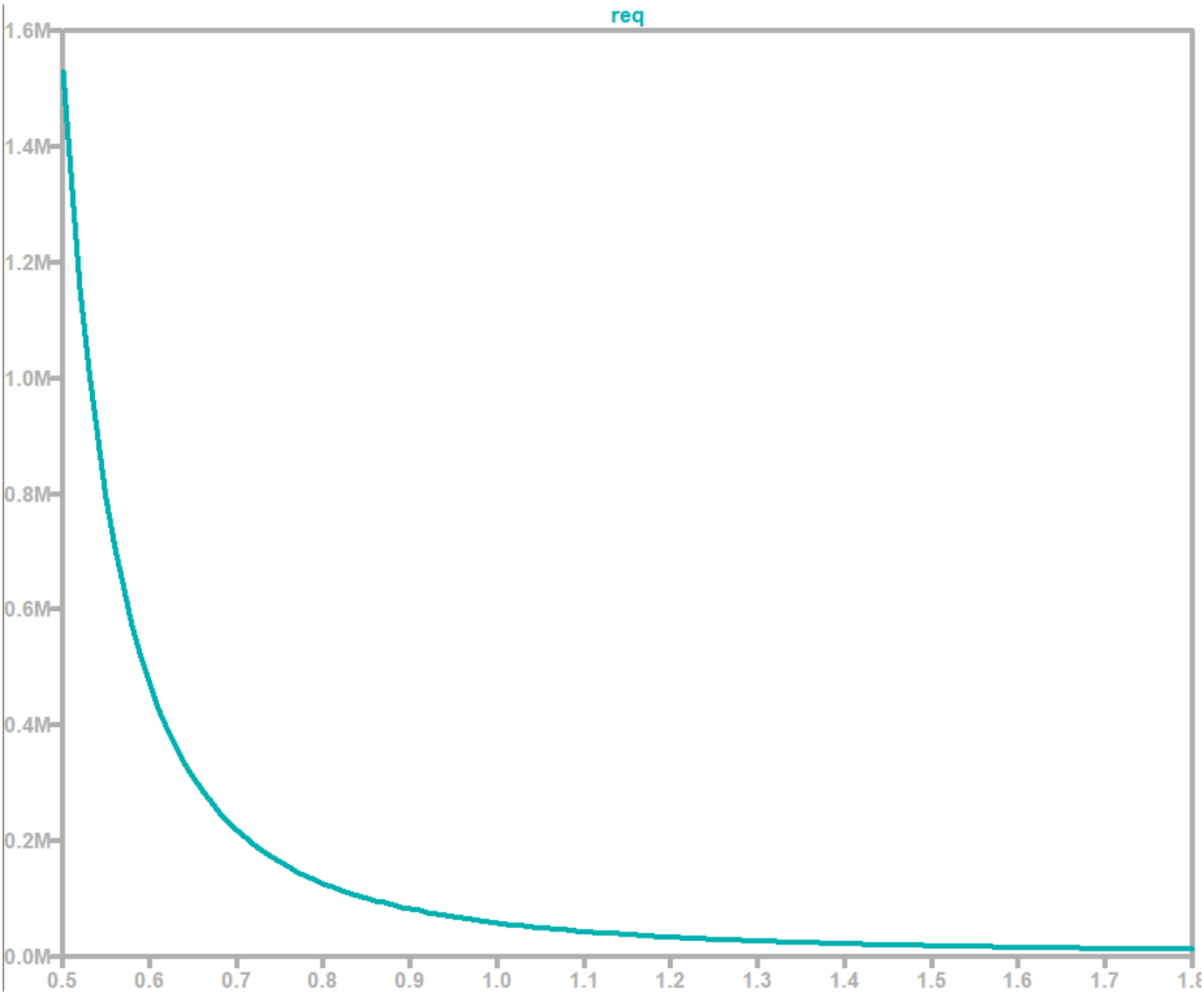
(a)

NMOS



R_{eq} **Vs** V_{DD}

PMOS



R_{eq} **Vs** V_{DD}

(b)

Table 3.3

V_{DD}(V)	1	1.5	2	2.5
NMOS(kΩ)	35	19	15	13
PMOS(kΩ)	115	55	38	31

Simulated Table

V_{DD}(V)	1	1.2	1.4	1.6
NMOS(kΩ)	16.66	12.0	9.56	8.2
PMOS(kΩ)	58.63	34.02	22.41	16.2

• We can clearly see that both tables have similar pattern and for obvious reasons like device size they don't have exactly same values.

• For Both tables Equivalent Resistance Decreases as V_{DD} increases.

2 MOSFET Capacitance

2.1 Problem Statement

The gate capacitance of a MOSFET can be calculated by applying a gate voltage $V_{applied} = V_{CM} + V_0 \sin(\omega t)$ in the circuit in Figure 2. Since $I = CV_0\ \omega\cos(\omega t)$ we can obtain the CV characteristics by sweeping V_{CM} (in ac analysis) and setting AC magnitude to $1/(2\pi f)$, where f is the frequency of choice. The capacitance will then be given by the current in gate terminal.

Consider long and short channel MOSFETs with L = 10 μm and L = 0.18 μm respectively. Both devices have identical W/L of 1.5/2.5.

(a) Simulate the CV characteristics of NMOS devices using 180 nm technology. Generate plots of $C(V_{CM})$ for short and long channel devices, and explain the trends you observe in your simulations. (c. f. Example 3.9 of textbook)

(b) Will the CV characteristics change when you set the frequency to 10 MHz and 10 GHz? Explain your results.

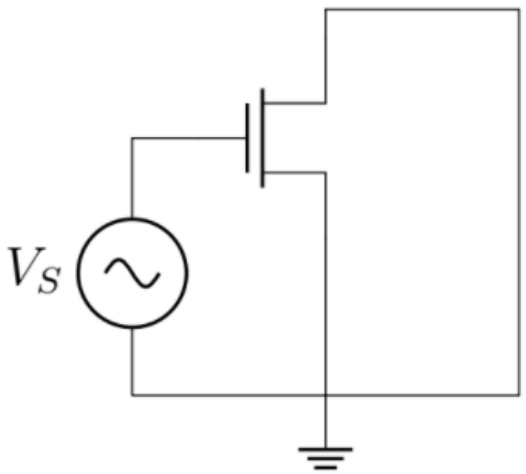


Figure 2

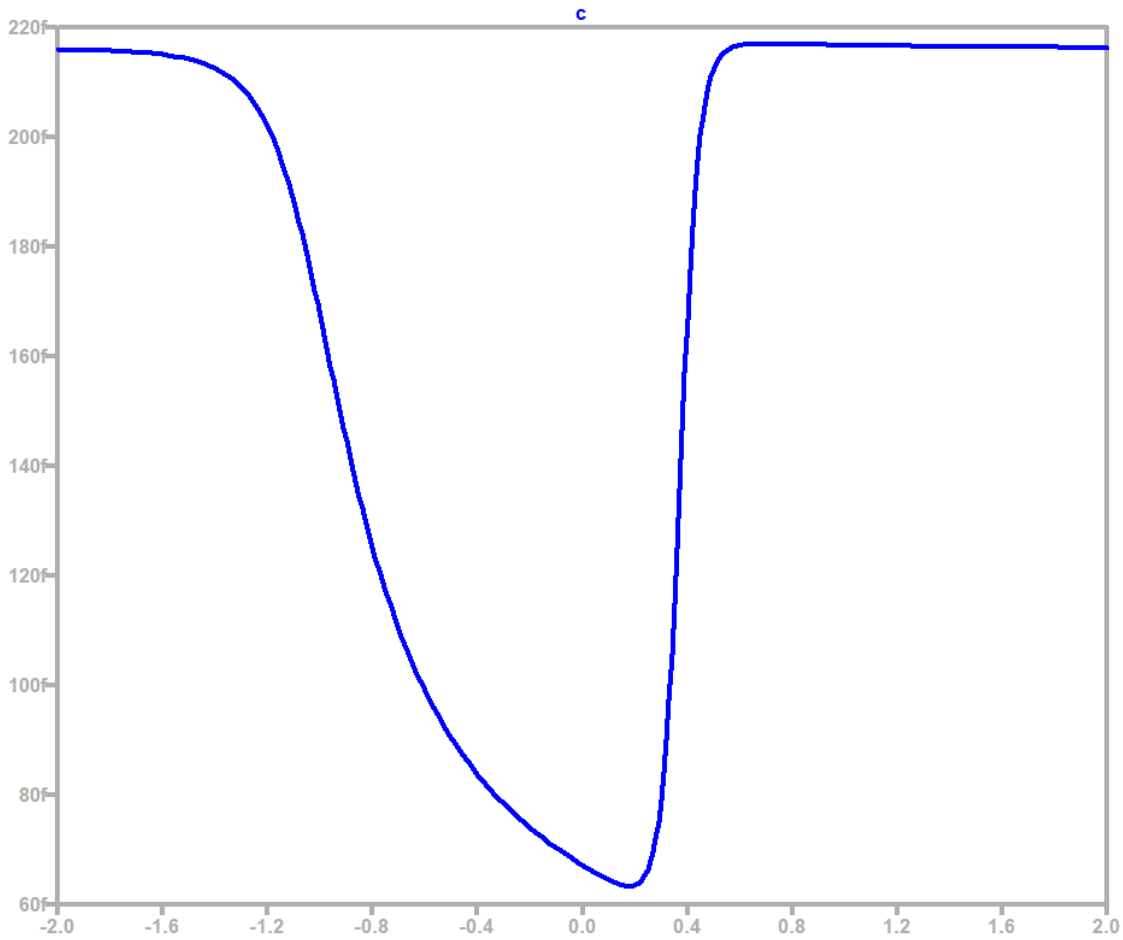
2.2 Spice Netlist

```
M1 0 N001 0 0 nch_tt L = 0.18u ,W = 0.108u
V1 N001 0 X AC 0.159154
.model NMOS NMOS
.model PMOS PMOS
.lib C:standard.mos
.meas AC C FIND Ig(M1) AT 1
.step param X -2 2 0.01
.ac dec 1000 10 100k
.include "TSMC180.lib"
.backanno
.end
```

2.3 Solution

(a)

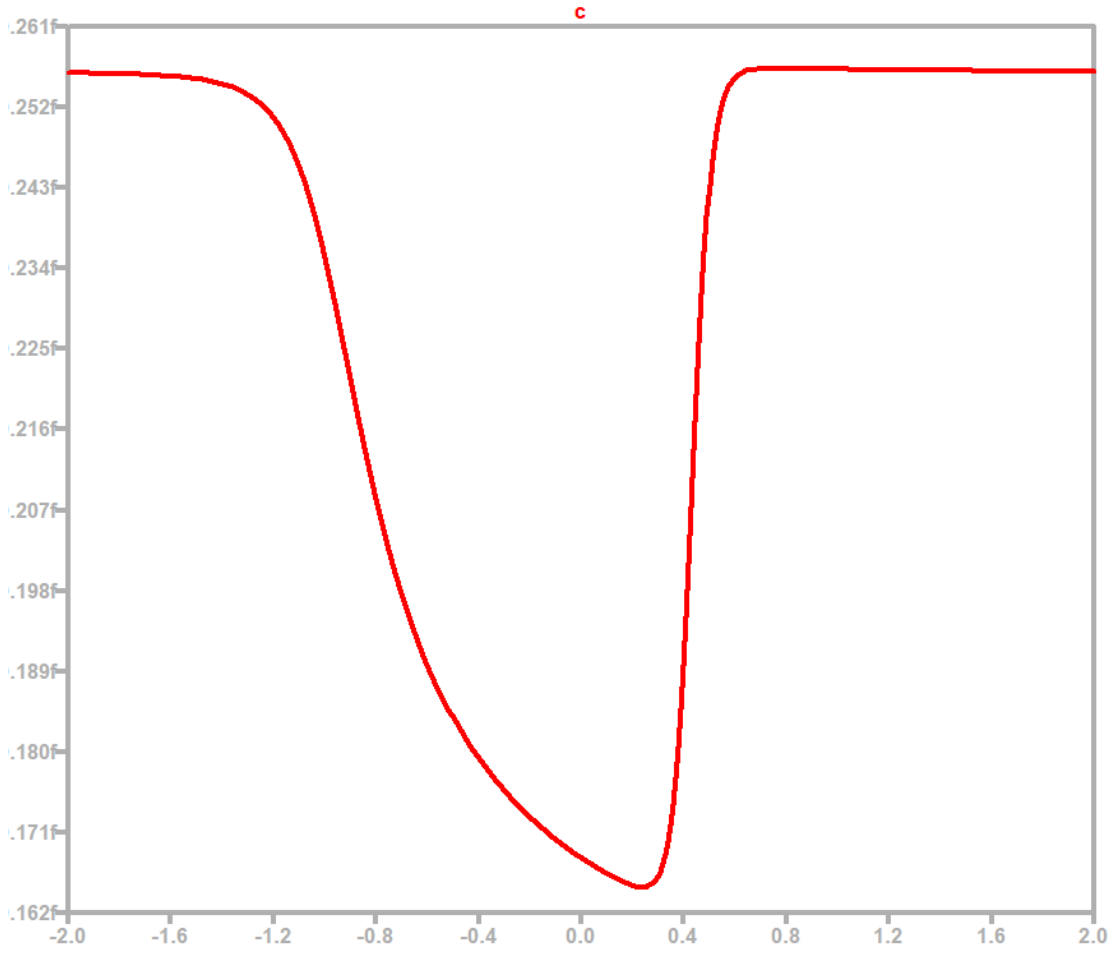
Long channel NMOS



CV characteristics

- From -2 to -1.2 V : Accumulation Region Capacitance is constant.
- From -1.2 to 0 V : Depletion Region Capacitance is decreasing.
- From 0 to 0.2 V : Weak Inversion Region Capacitance is decreasing.
- From 0.2 to 0.4 V : Moderate Inversion Region Capacitance is increasing.
- From 0.4 to 2 V : Strong Inversion Region Capacitance is constant.

Short channel NMOS

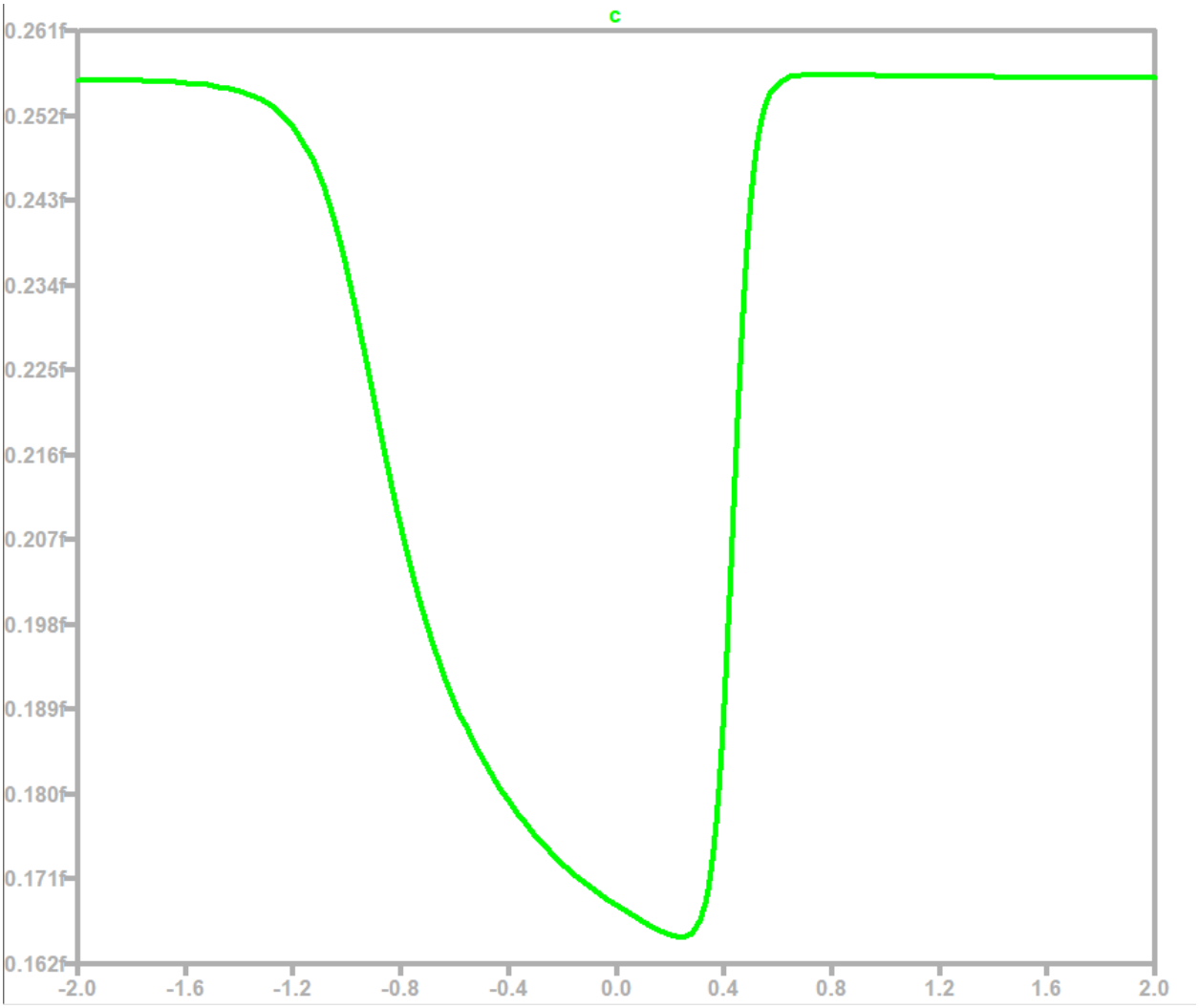


CV characteristics

- From -2 to -1.2 V : Accumulation Region Capacitance is constant.
- From -1.2 to 0 V : Depletion Region Capacitance is decreasing.
- From 0 to 0.2 V : Weak Inversion Region Capacitance is decreasing.
- From 0.2 to 0.4 V : Moderate Inversion Region Capacitance is increasing.
- From 0.4 to 2 V : Strong Inversion Region Capacitance is constant.

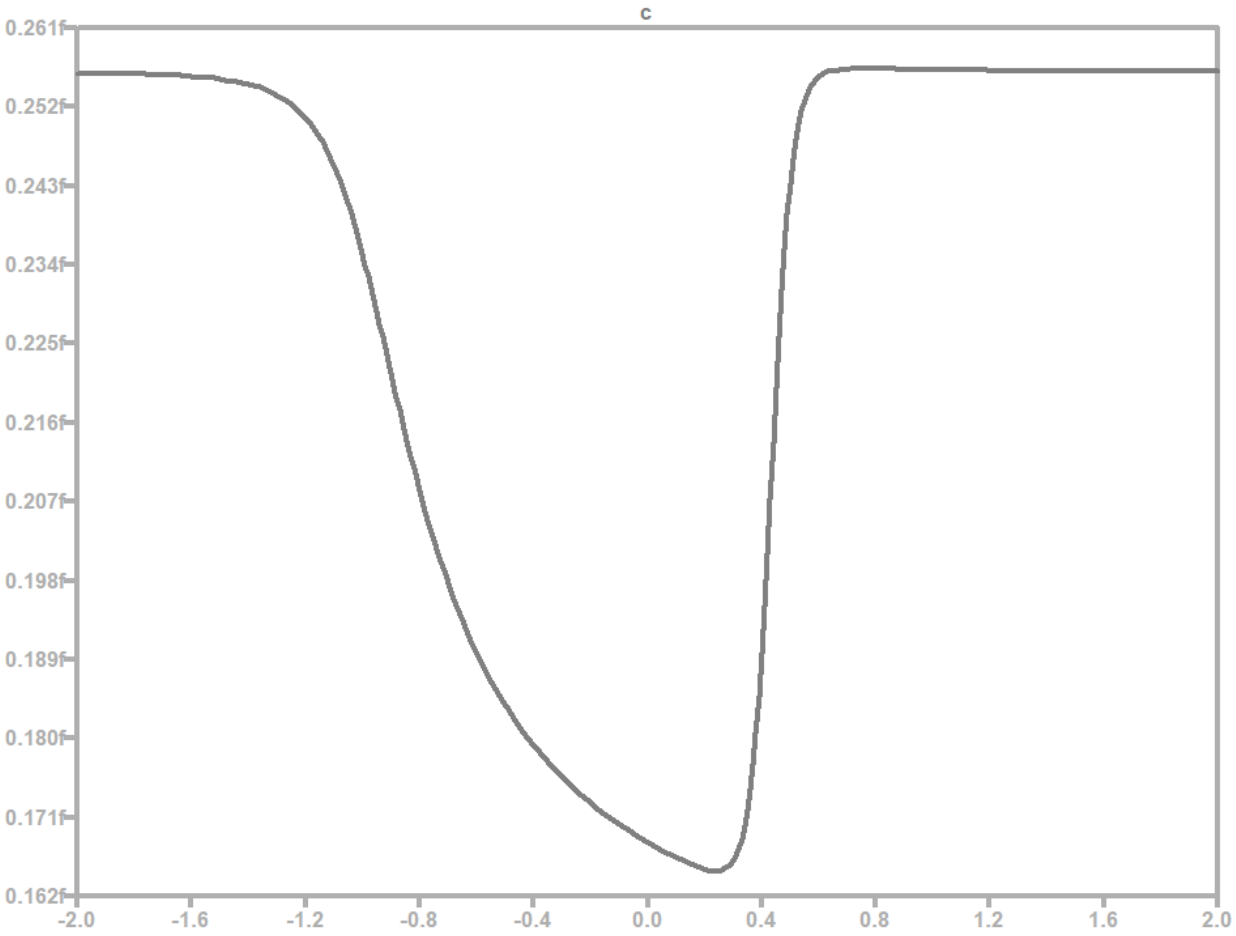
(b)

f = 10MHz



CV characteristics

f = 10GHz



CV characteristics

•. The plots at both frequencies are same which can be explained from the equation given in question.

3 Inverter Implementations

3.1 Problem statement

The circuits in Figure 3 show different implementations of a digital inverter($V_{DD} = 1.2$ V), whose output is connected to a capacitor. Assume $V_{T_N} = |V_{T_P}| = 0.3$ V , and the output capacitor, C_L, is initially discharged. Ignore sub-threshold conduction and body effect. Without running simulations answer the following:

(a) Which one(s) of the circuits consume(s) static power when the input is high ($V_{IN} = 1.2$ V)?

(b) Which one(s) of the circuits consume(s) static power when the input is low($V_{IN} = 0$ V)?

(c) V_{OH} of which circuit(s) is 1.2 V (if possible)?

(d) V_{OL} of which circuit(s) is 0 V (if possible)?

(e) The proper functionality of which circuit(s) depends on the size of the devices? (Note that they are designed for a digital inverter)

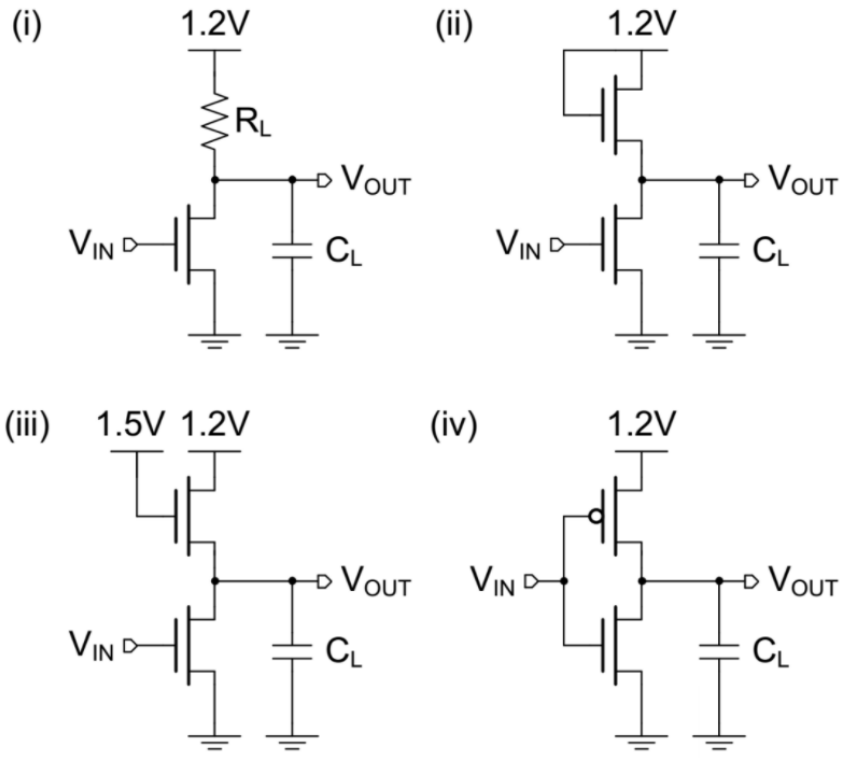


Figure 3

3.2 Solution

(a) All inverters but the CMOS inverter, (iv), consume static power when the input is high. Notice that in the first three inverters, (i) (iii) when the input is high, there is always a direct connection from VDD to GND.

(b) None of the static inverters consumes power when the input is low because there is no path from VDD to GND.

(c) All inverters but the saturated enhancement inverter,(ii), has a V_{OH} of 1.2 V.

(d) Only the CMOS inverter, (iv), has a V_{OL} of 0 V

(e) Except for the CMOS inverter, (iv), all the other inverters' functionality depend on the relative sizes of the transistors.

4 NMOS Inverter - manual analysis

4.1 Problem statement

Consider a NMOS inverter shown in Figure 4.

(a) Calculate V_{OH}, V_{OL} and V_M.

(b) Derive expressions for V_{IL}, V_{IH} and hence determine the noise margin. You may ignore channel length modulation in your analysis.

(c) Derive an expression for the peak gain and estimate the same.

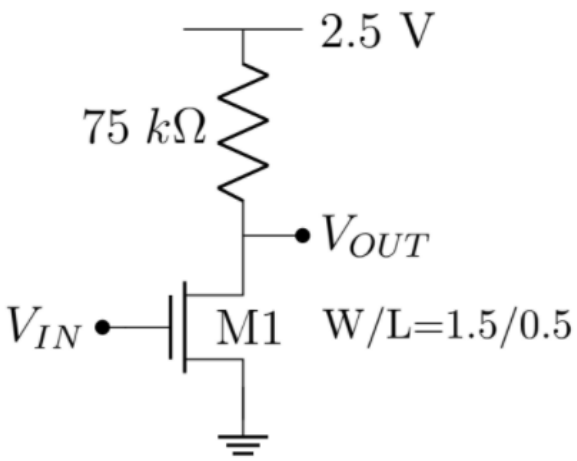


Figure 4

4.2 Solution

(a)

V_{OH} :

Assuming negligable leakage, when $V_{in} \leq V_T$, transistor M1 is off and V_{OH}=2.5 V.

V_{OL} :

For V_{in}=2.5 V, assume M1 is in the linear region, and because V_{DS} is negligible in the linear region, channel-length modulation can be ignored.

$$\frac{2.5 - V_{min}}{75K} = \frac{k_n W}{L}\left(V_{GT}V_{DS} - \frac{V_{DS}^2}{2}\right) \tag{1}$$

For the linear region, V_{min}=V_{DS}=V_{out}=V_{OL} =46.25m. Checking the assumption: V_{GT}=2.07 V, V_{DSat}=0.63 V, and V_{DS}=46.25m, thus, M1 was correctly assumed to be in the linear region.

V_M :

To find V_M, set the resistor current equal to the NMOS current, with an input and output voltage of V_M.

$$\frac{2.5 - V_M}{75K} = \frac{k_n W}{L}\left(\frac{(V_M - V_T)^2}{2}\right)(1 + 0.006V_M) \tag{2}$$

Thus V_M = 0.79 V.

(b)

To find V_{IL} and V_{IH} , the slope of the VTC. at V_M , is derived and the line is extrapolated out to V_{OH} and V_{OL} . respectively. Ignoring the efiects of channel length modulation, the slope is given by the following:

$$\frac{dV_o}{dV_{in}} = -\frac{R_L K_n W}{2L}\Big(2V_{in} - 0.86\Big) \tag{3}$$

Plugging V_M =0.79 V, into the slope equation above, gives a slope of 9.32.

Extrapolating the line back to V_{OH} gives $V_{IL} = 0.607$ V and the extrapolation of the line to V_{OL} gives $V_{IH} = 0.87$ V.

NML = V_{IL} - V_{OL} = 0.607 V and NMH = 2.5V - V_{IH} = 1.63 V

(c)

From the equation (3) as above The gain increases in saturation region and in linear region the gain decreases, Therefore we need to find the point between saturation and linear region to find peak gain, i.e. $V_{GT} = V_{DS}$

$$\frac{2.5 - V_{DS}}{75K} = \frac{k_n W}{2L}\left(\frac{V_{DS}^2}{2}\right)(1 + 0.006V_{DS}) \tag{4}$$

Thus $V_{DS} = 0.402$ V, $V_{in} = 0.832$.

$$Peak\ Gain = \frac{dV_o}{dV_{in}} = -\frac{R_L K_n W}{2L}\Big(2V_{in} - 0.86\Big) = -10.427 \tag{5}$$

5 NMOS Inverter- SPICE simulations

5.1 Problem Statement

Compare the results of question 4 by performing simulations in SPICE with 180 models.

(a) Simulate the VTC and plot the gain of the inverter by calculating $\mathrm{d}V_{out}/\mathrm{d}V_{in}$.

(b) How does the load resistance impact the threshold and peak gain of the inverter? Verify by simulating for a wide range of resistances.

(c) Simulate the frequency response using transient analysis at f = 250 kHz, 50% duty cycle and C_L = 3 pF. Calculate t_r, t_f and t_p for the inverter. Are the rise and fall times equal? Why or why not? What are the geometric parameters that influence the maximum operating frequency of the inverter? What is the dynamic power dissipation assuming that the inverter is clocked at highest possible frequency?

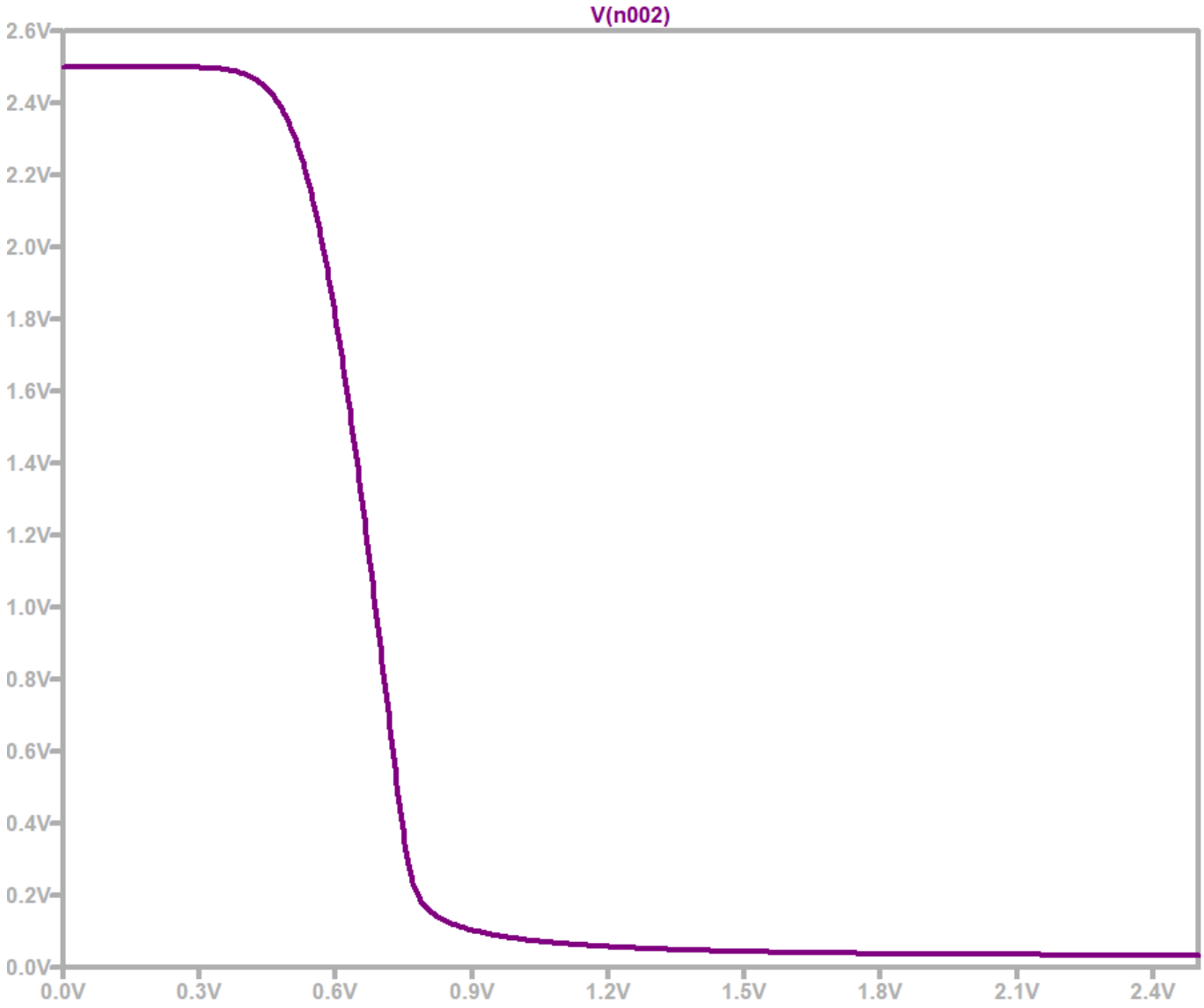
5.2 Spice Netlist

```
R1 N001 N002 75k
M1 N002 N003 0 0 nch_tt
V1 N001 0 2.5
V2 N003 0 0
.model NMOS NMOS
.model PMOS PMOS
.lib C:standard.mos
.dc V2 0 2.5
.include "TSMC180.lib"
.backanno
.end
```

5.3 Solution

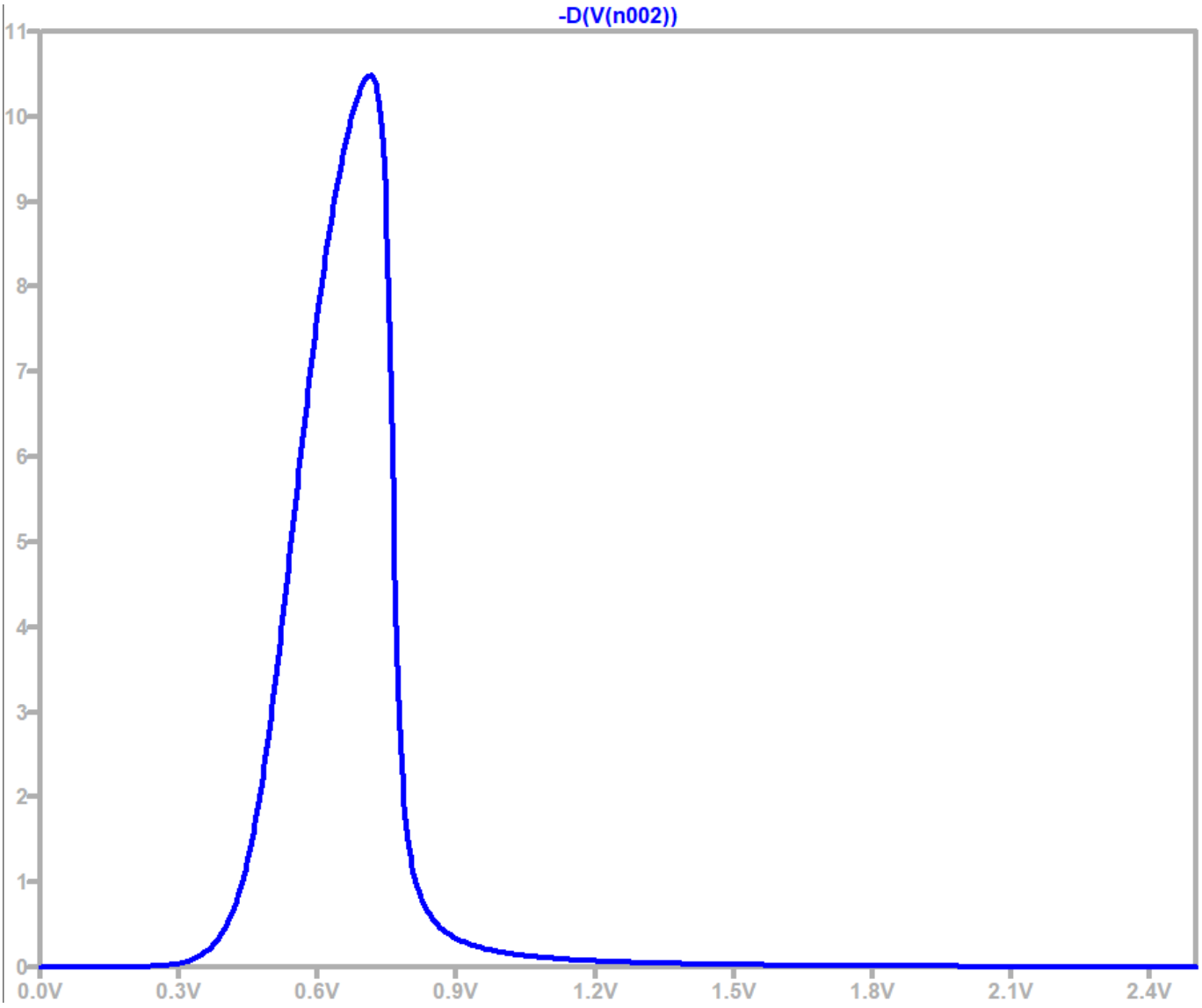
(a)

VTC



VTC

$\mathrm{d}V_{out}/\mathrm{d}V_{in}$

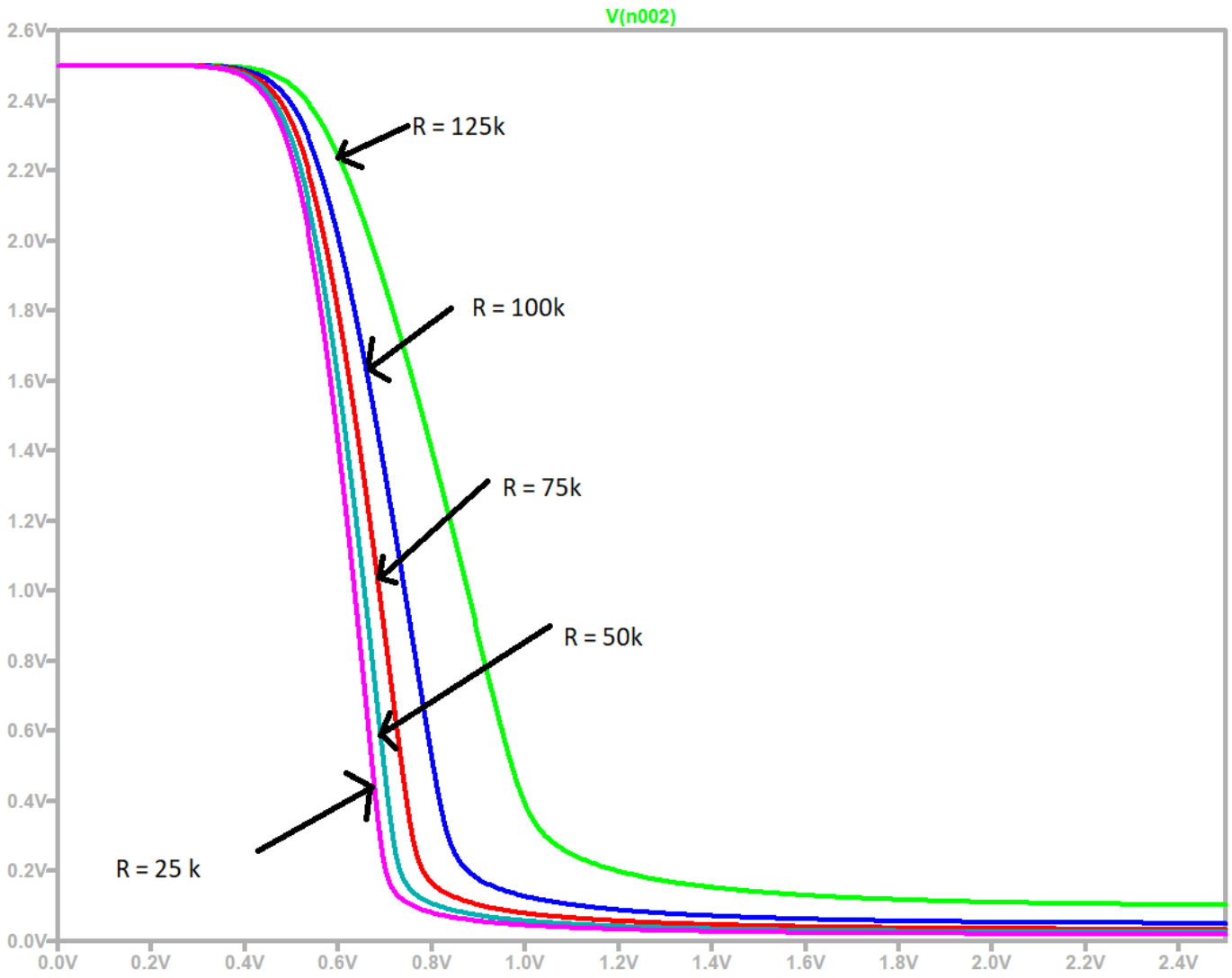


Gain Vs V_{in}

- The plots and values are similar to calculated values.

(b)

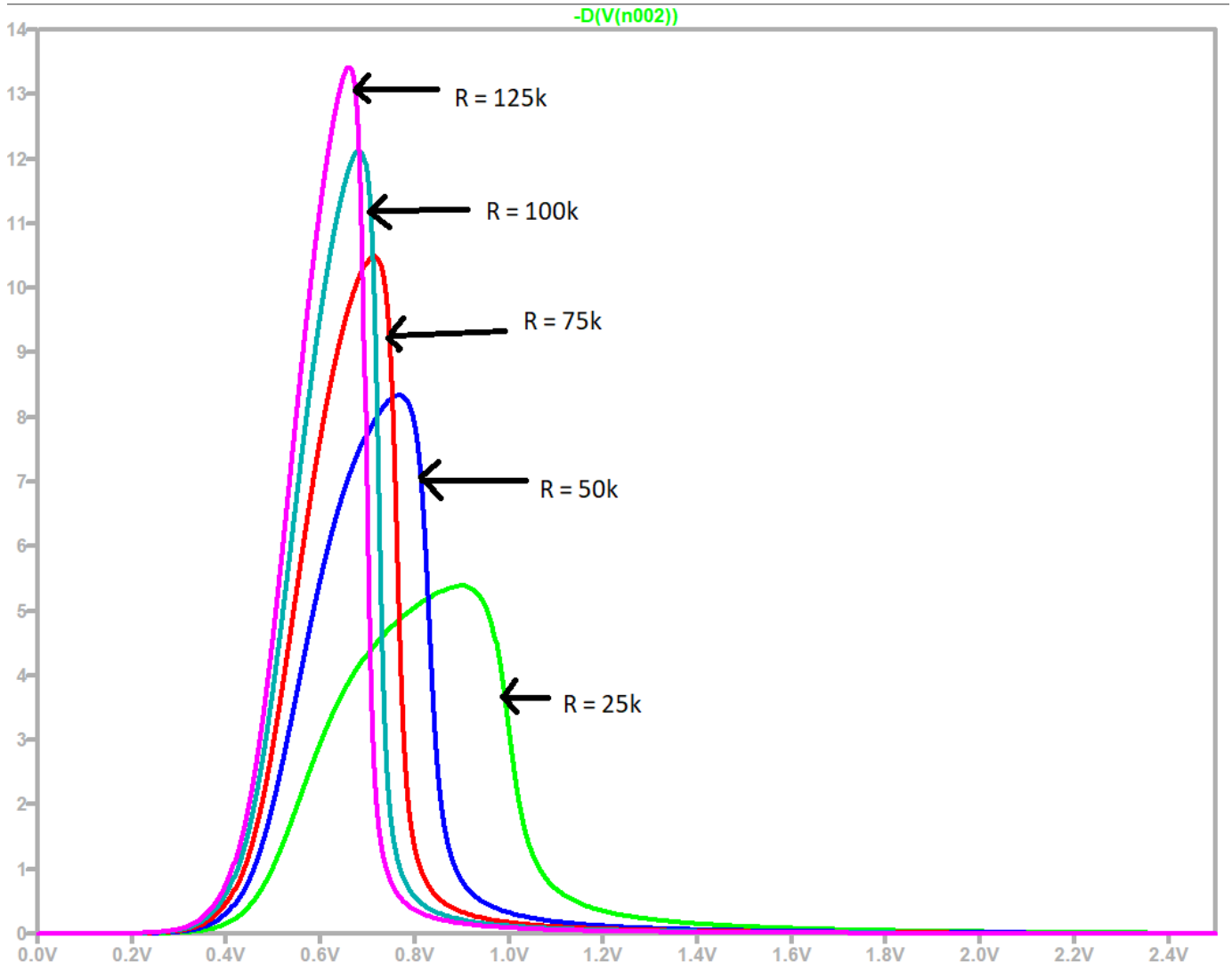
VTC Vs R_L



VTC

- As R_L increases, V_{OL},V_{IL},V_{IH} decrease But V_{OH} remains unchanged.

$\mathrm{d}V_{out}/\mathrm{d}V_{in}$ Vs R_L

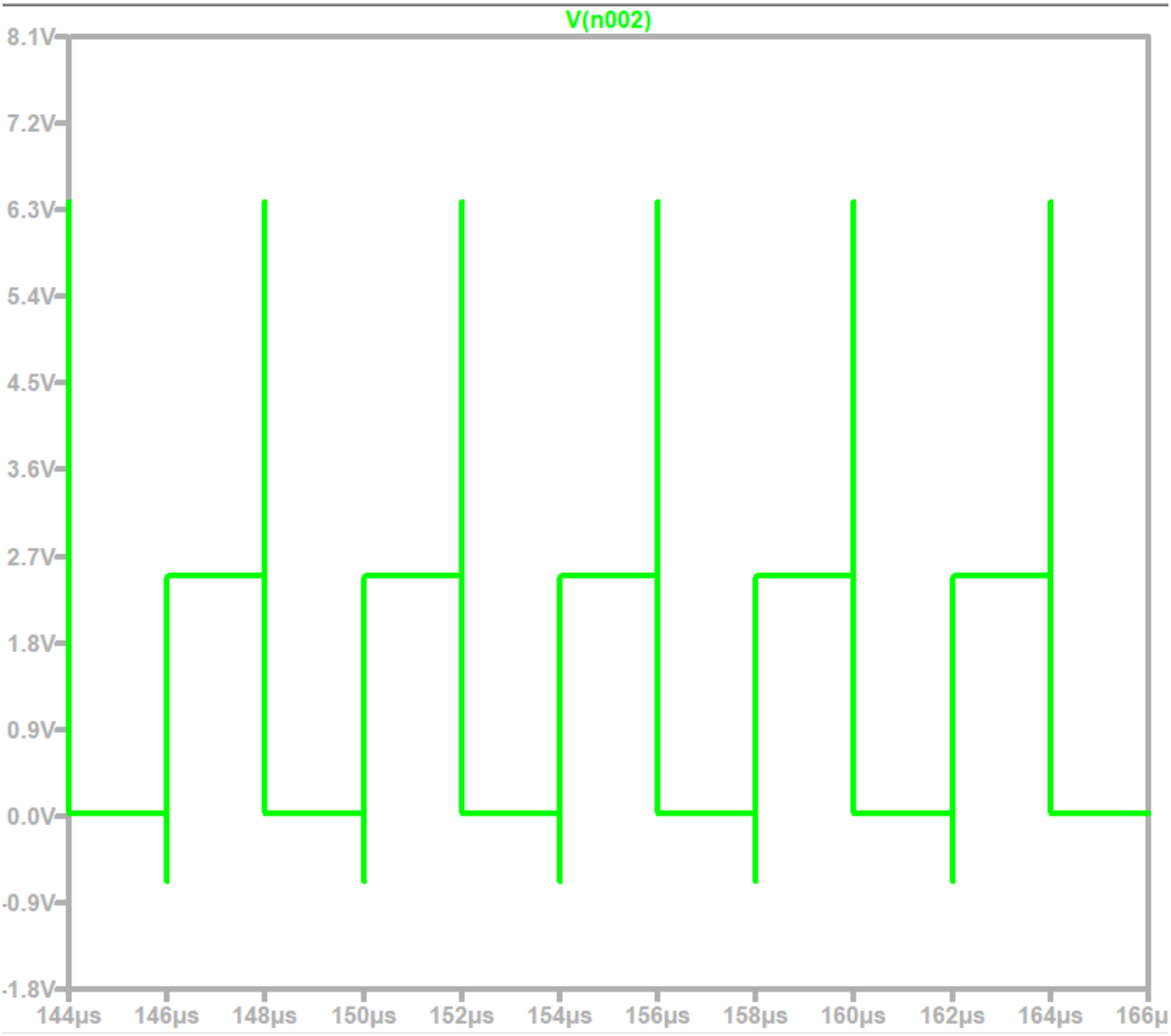


Gain Vs V_{in}

- The peak gain increases as Load Resistance increases.

(c)

Transient Response



V_{out} **Vs time**

- From simulation $t_r = 150.86063$ psec , $t_f = 8$psec, $t_p = 79$psec.

Calculation:

$t_r = 0.69 R_L C_L = 155$nsec

For t_f: First calculate R_{ON} for V_{out} at 2.5V and 1.25V. At V_{out} =2.SV, I_{DVsat}=O.439mA giving Ron: 5695k and when V_{out}=1.25V, I_{DSat}=0.41m giving Ron: 3049W.

Thus, the average resistance between V_{out}=2.5Vand V_{out}=l.25V is R_{avg}=4372k

t_f=O.69$R_{avg}C_L$=9.05nsec.

t_p = Avg(t_r,t_f) = 82 nsec.

• $t_r \gg t_f$ because R_L=75kΩ is much larger than the effective linearized on-resistance of M1.

• W,L values influence the maximum Operating frequency.

Dynamic Power calculation

$f_{max} = 1/t_p$

$$P_{Dyn} = C_L * \Delta V * V_{DD} * f_{max} = 0.225mW. \tag{6}$$


thank
you