



EE5192 : Integrated Circuits For Wireless Communication

Mini Project 1

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1 Matching Network

1.1 Problem Statement

1. Design a matching network to transform $250\ \Omega$ to $50\ \Omega$ at 1 GHz using any configuration to meet the following design requirements:

- . • Network can use ideal capacitors but inductor(s) must have Q of 15 at 1GHz.
- . • Return loss @ 1 GHz ≥ 15 dB (both the ports).

Objective is to minimize insertion loss while satisfying the above specifications.

Submit the following::

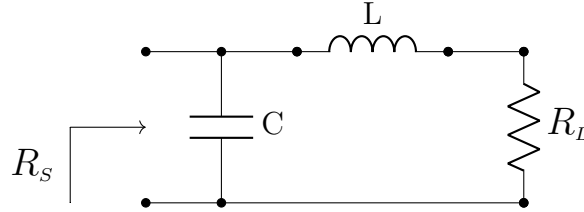
- . • Hand calculation to find the matching network component values.
- . • S-parameters magnitude (in dB) from 0.5 GHz to 5 GHz.

CAD info:

- . • Simulate the matching network in LTspice.

1.2 Calculations

Given $R_L = 50$, $R_S = 250$ and $\omega = 2\pi 10^9$ we will be using an L matching network for this step-down configuraton.



$$\begin{aligned} Q &= \sqrt{R_S/R_L - 1} \\ &= \sqrt{5 - 1} \\ &= 2 \end{aligned} \tag{1}$$

$$Q = X_L/R_L = R_S/X_C \tag{2}$$

$$X_L = \omega L \tag{3}$$

$$X_C = 1/\omega C \tag{4}$$

Using the above equations the component values turnout to be $L = 15.92$ nH, $C = 1.273$ pF. Also given that the Inductor is non ideal with $Q_L = 15$ @ 1GHz, We will find the resistance value of the inductor based on the given quality factor.

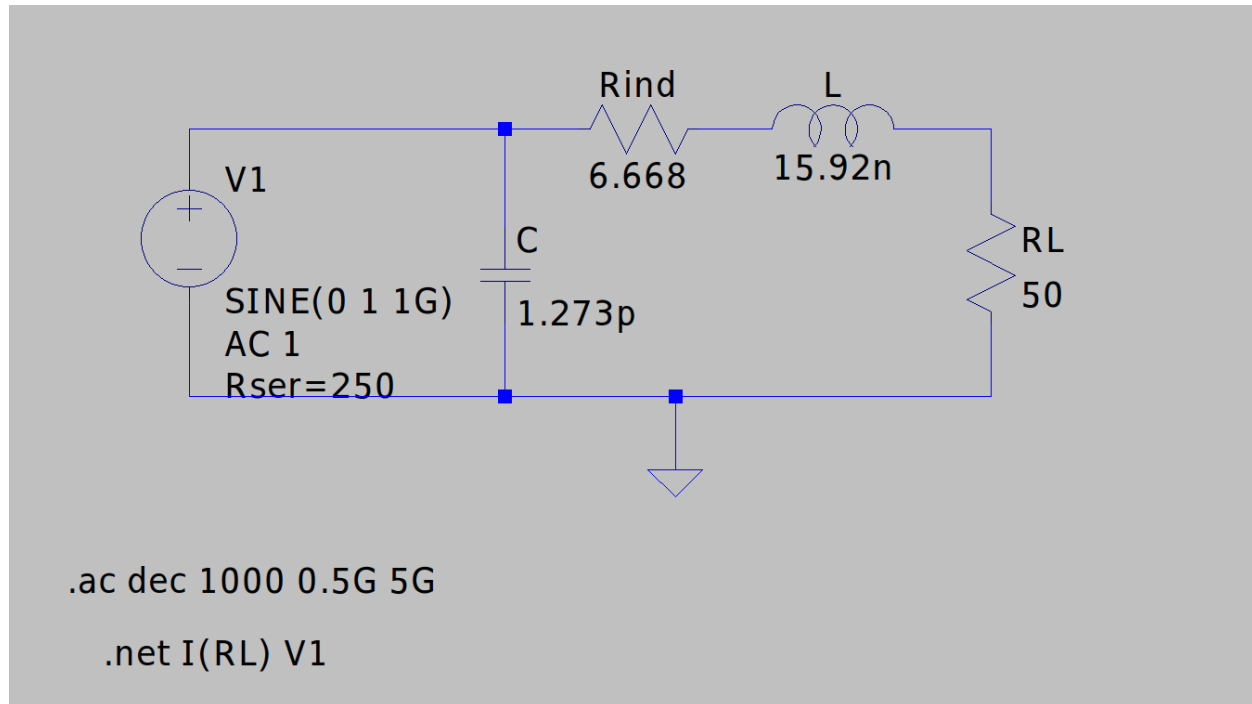
$$R_{ind} = X_L/Q_L \tag{5}$$

$$= \omega L/Q_L \tag{6}$$

$$R_{ind} = 6.668\Omega \tag{7}$$

1.3 Schematic

Circuit

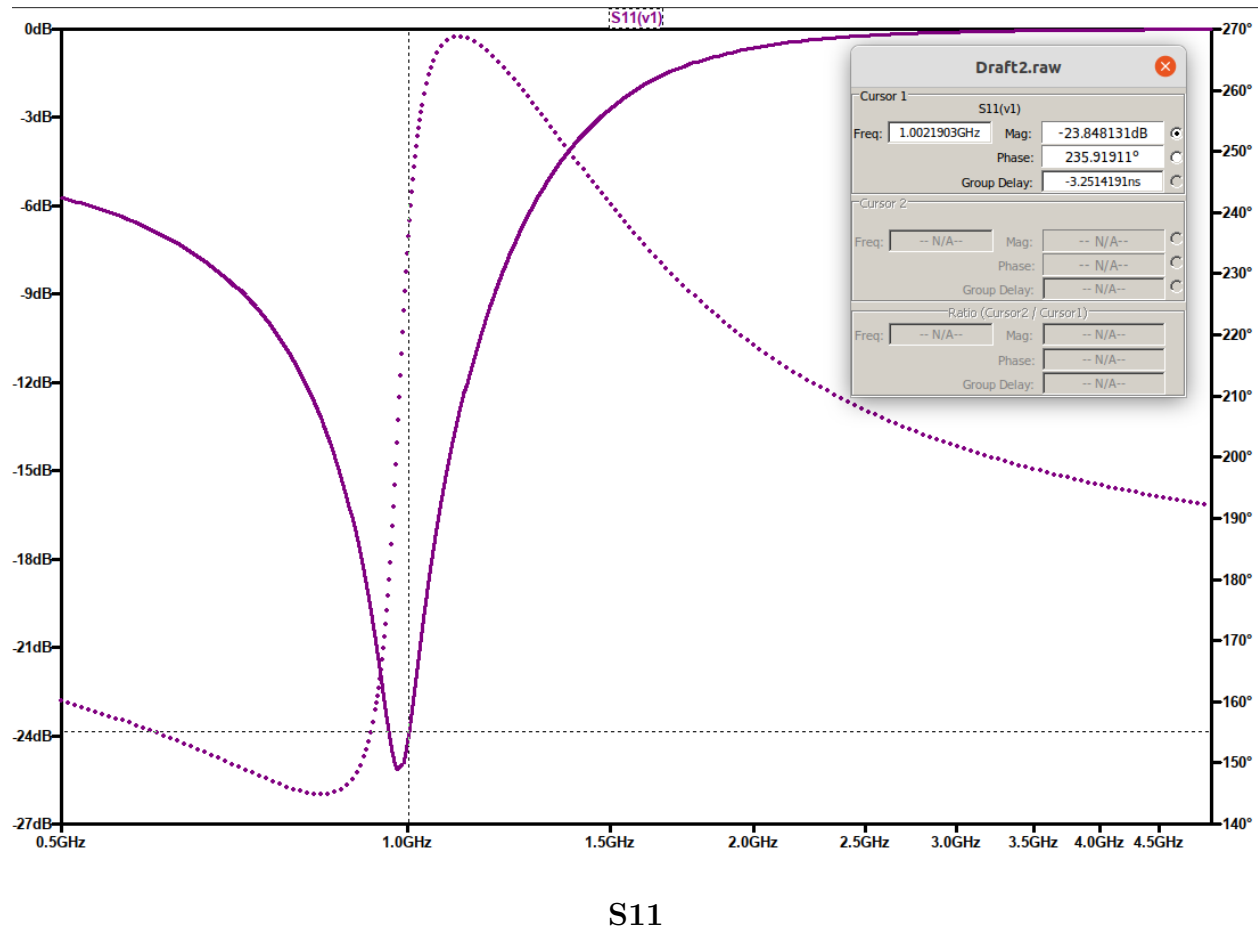


LTSpice schematic of the Matching Network

- Next we will plot the S-Parameters across 0.5GHz to 5GHz.

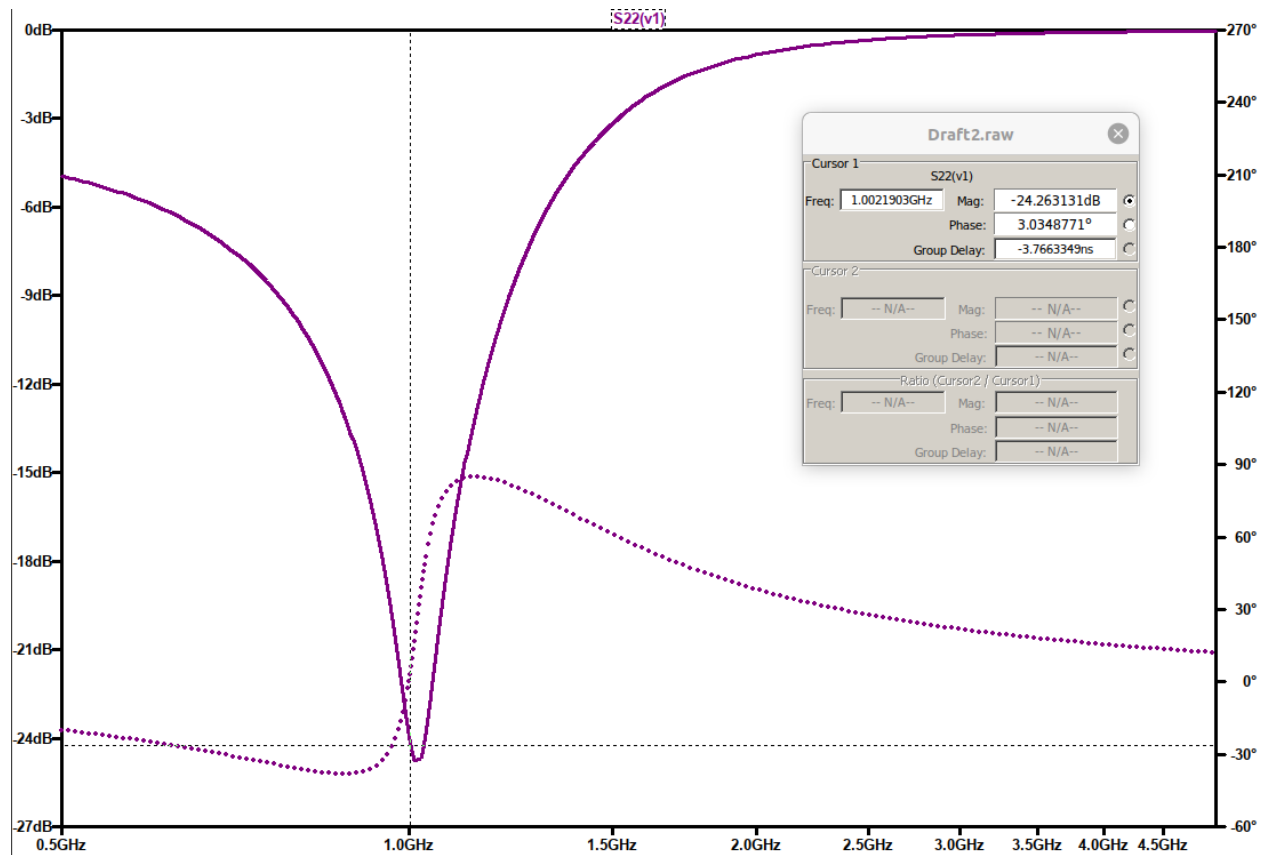
1.4 S-Parameters

S11 (Return loss)



The Return loss at Input Port S11@1GHz = -23.84dB is less than -15dB requirement.

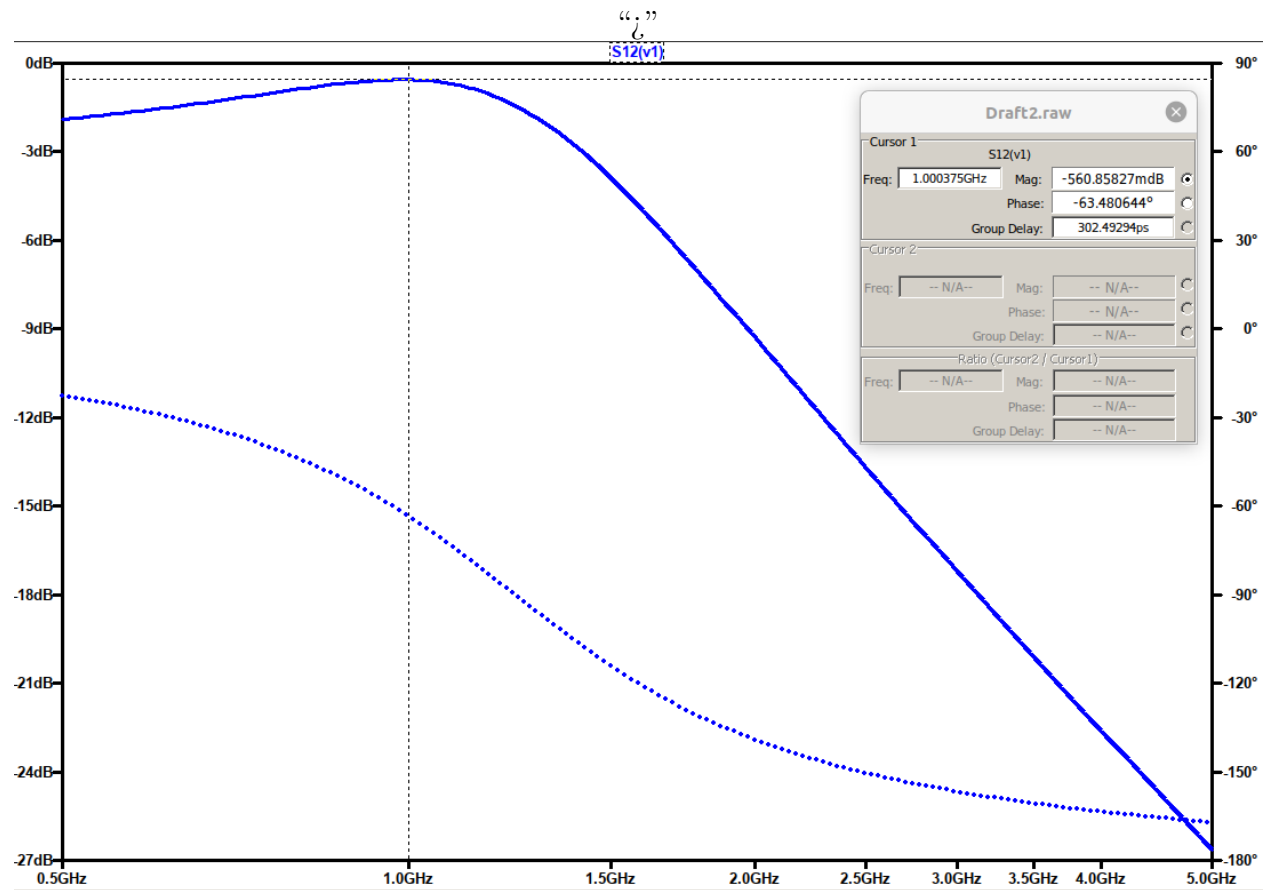
S22 (Return loss)



S22

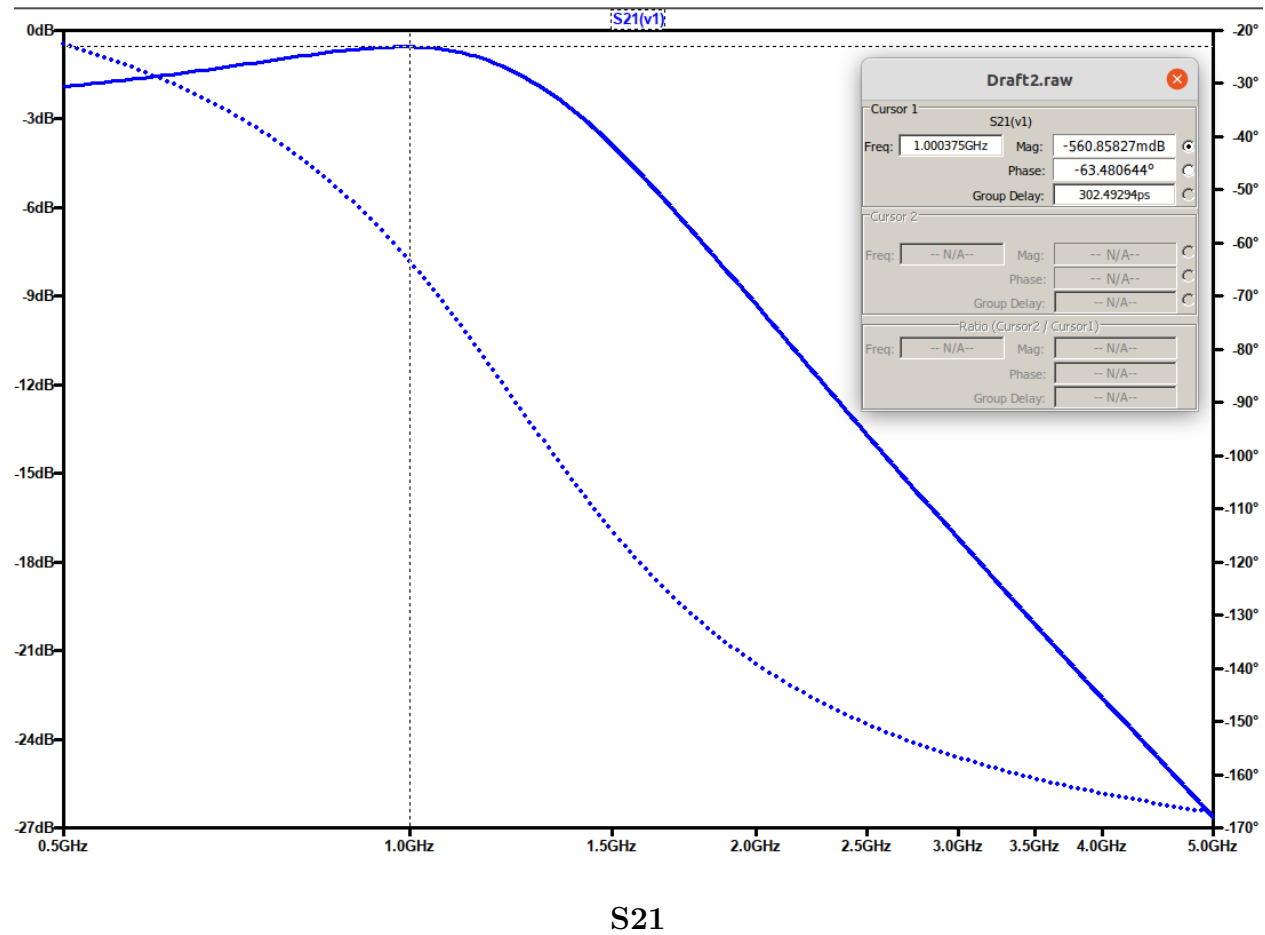
The Return loss at Output Port S22@1GHz = -24.26dB is less than -15dB requirement.

S12 (Insertion loss)



S12

S21 (Insertion loss)



The Insertion loss $S_{12}@1\text{GHz} = S_{21}@1\text{GHz} = -0.560\text{dB}$ is very minimal.

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