EE5192 : Integrated Circuits For Wireless Communication
Mini Project 2

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Contents

1 LNA Design

1.1 Problem Statement

1. Design an LNA to meet the following specifications:

   - Gain $>$ 20 dB
   - Input return loss $>$ 15 dB
   - NF $<$ 2 dB
   - IIP_3 $>$ -30 dBm
   - Centre frequency: 2.5 GHz
   - Load capacitance: 100 fF

   System-level constraints:

   - Supply voltage $<$ 1.1 V
   - Inductors available: Value $<$ 10 nH, Q=15 @ 2.5 GHz.

   Objective is to minimize power consumption while satisfying the above specifications.

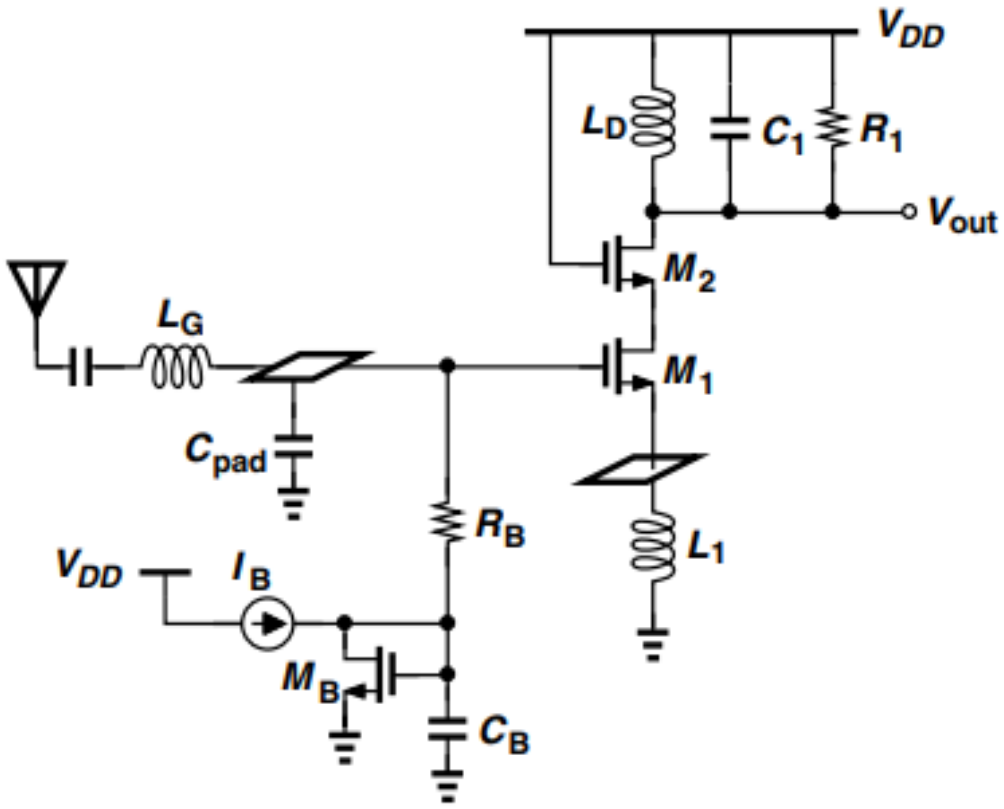
   Submit a report with the following:

   - Brief justification for the choice of LNA topology.
   - Design details.
   - Input return loss plot from 2 GHz to 3 GHz.
   - Gain plot from 2 GHz to 3 GHz.
   - NF plot from 2 GHz to 3 GHz.
   - IIP3 plot.
   - Netlist.

   CAD info:

   - MOS models are from a 65nm CMOS process. Minimum channel length is 65nm. Maximum DC voltage between any two terminals of the MOSFET must not exceed 1.1 V.
   - Use ideal capacitors and resistors. All inductors must have loss modelled by adding a series resistance corresponding to required Q value.

1.2 Design



Inductively-degenerated CS stage with bias network

Here we have used CS LNA over the CG LNA as it provides a lower Noise Figure. L1 is also chosen such that equivalent of L_1 and L_G oscillates with Pad Capacitance and Gate to Source Capacitance. The inductive degeneration helps improve the linearity and increase the input impedance. The Load inductance oscillates with the load capacitance at required frequency acting as a band-pass.

Below are some equations used for different constraints imposed on the design.

Gain

$$\frac{V_{out}}{V_{in}} = \frac{\omega_T}{2\omega_0}\frac{R_1}{R_S}$$
$$= \frac{R_1}{2L_1\omega_0}.$$
$$(g_{m1}/C_{GS1} \approx \omega_T)$$

Input Matching

$$\frac{1}{(L_G + L_1)(C_{GS1} + C_{pad})} = \omega_0^2$$
$$\left(\frac{C_{GS1}}{C_{GS1} + C_{pad}}\right)^2 L_1\omega_T = R_S.$$

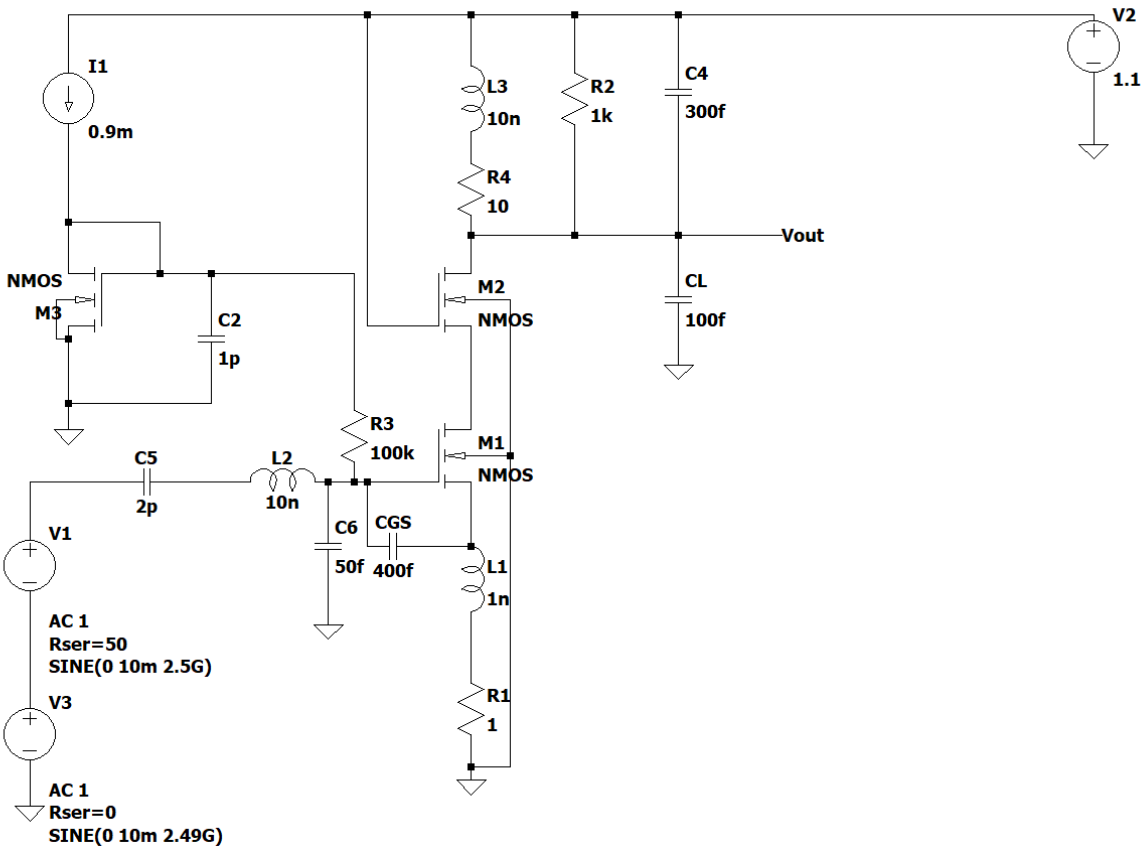
Noise Factor

$$\text{NF} = 1 + g_{m1}R_S\gamma\left(\frac{\omega_0}{\omega_T}\right)^2$$

The bias current of M1 is established by M_B and I_B, and resistor R_B and capacitor C_B isolate the signal path from the noise of I_B and M_B.

1.3 Schematic

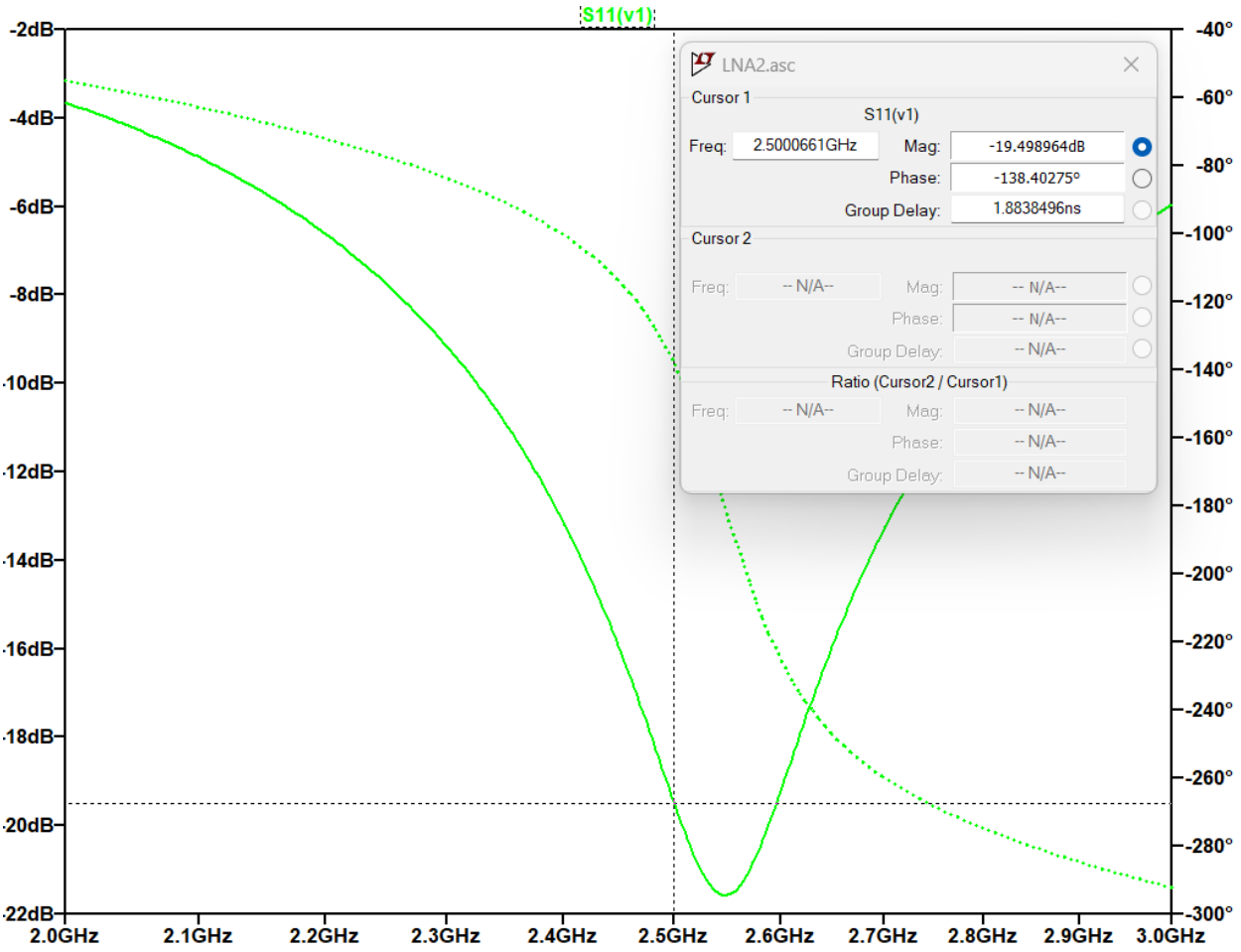
Circuit



LNA schematic

1.4 Input Return Loss

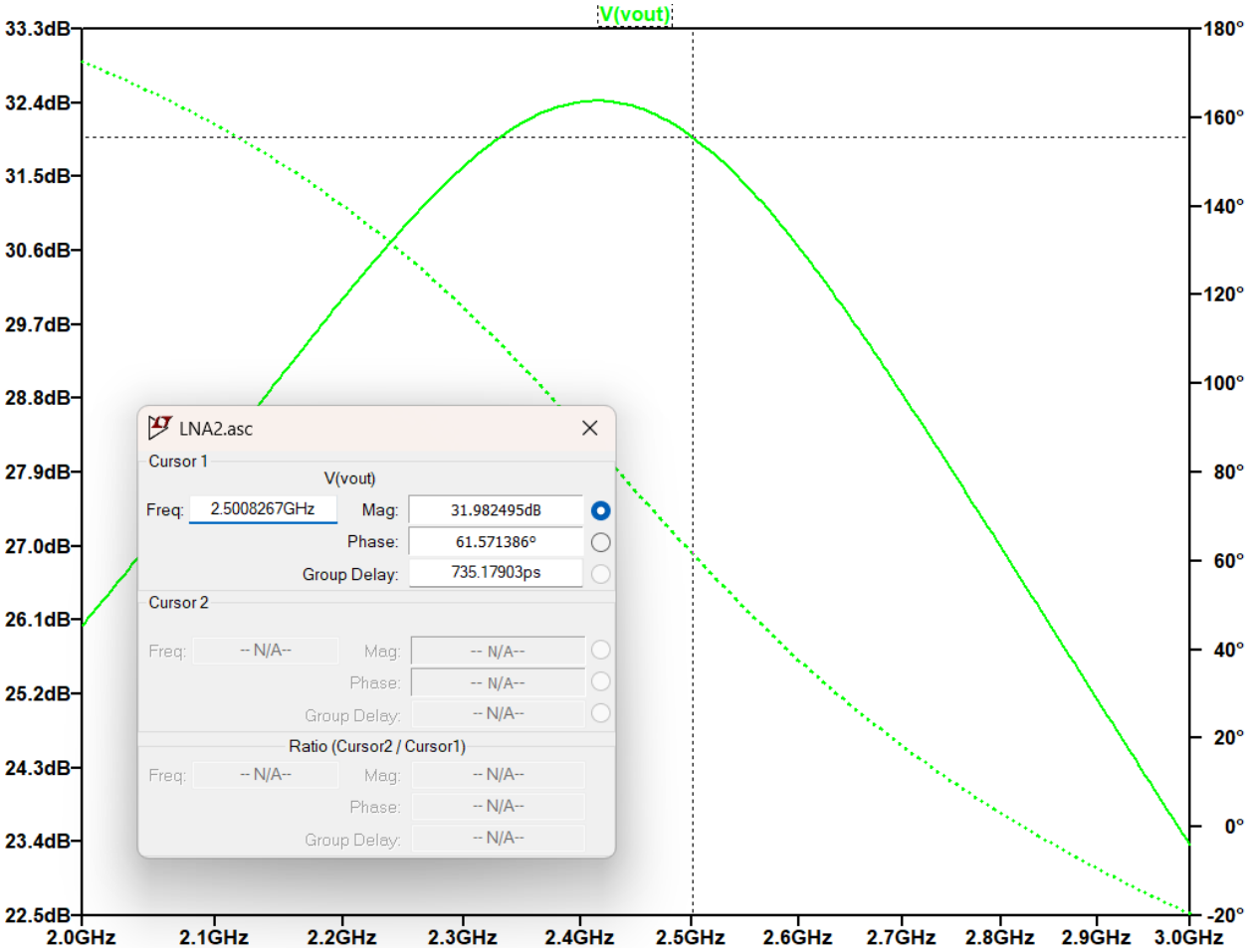
S11 (Return loss)



Input return loss plot from 2 GHz to 3 GHz

The Return loss at Input Port -S11@2.5GHz = 19.5 dB is greater than 15 dB requirement.

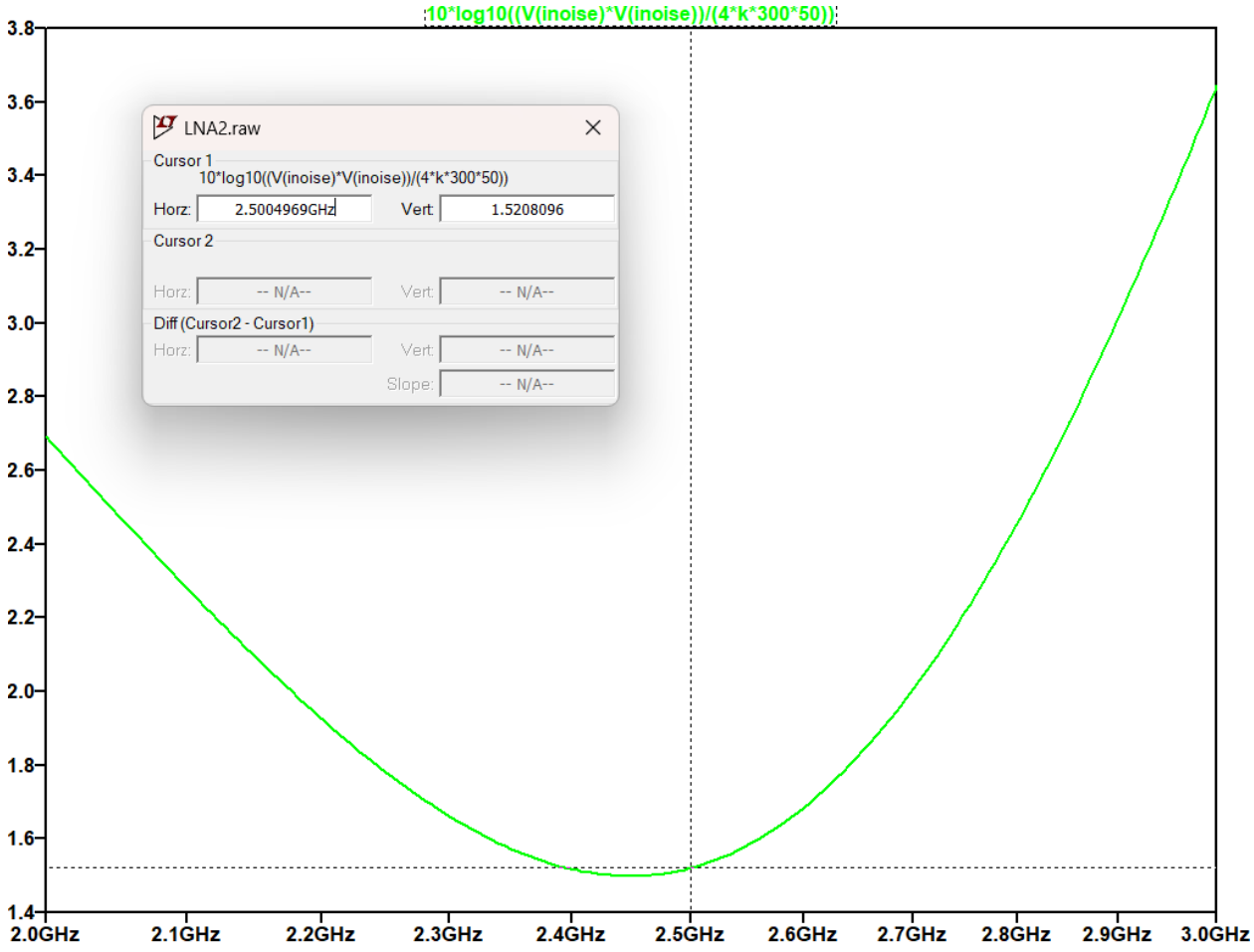
1.5 Gain



Gain plot from 2 GHz to 3 GHz

The Gain @ 2.5GHz = 32 dB is greater than 20 dB requirement.

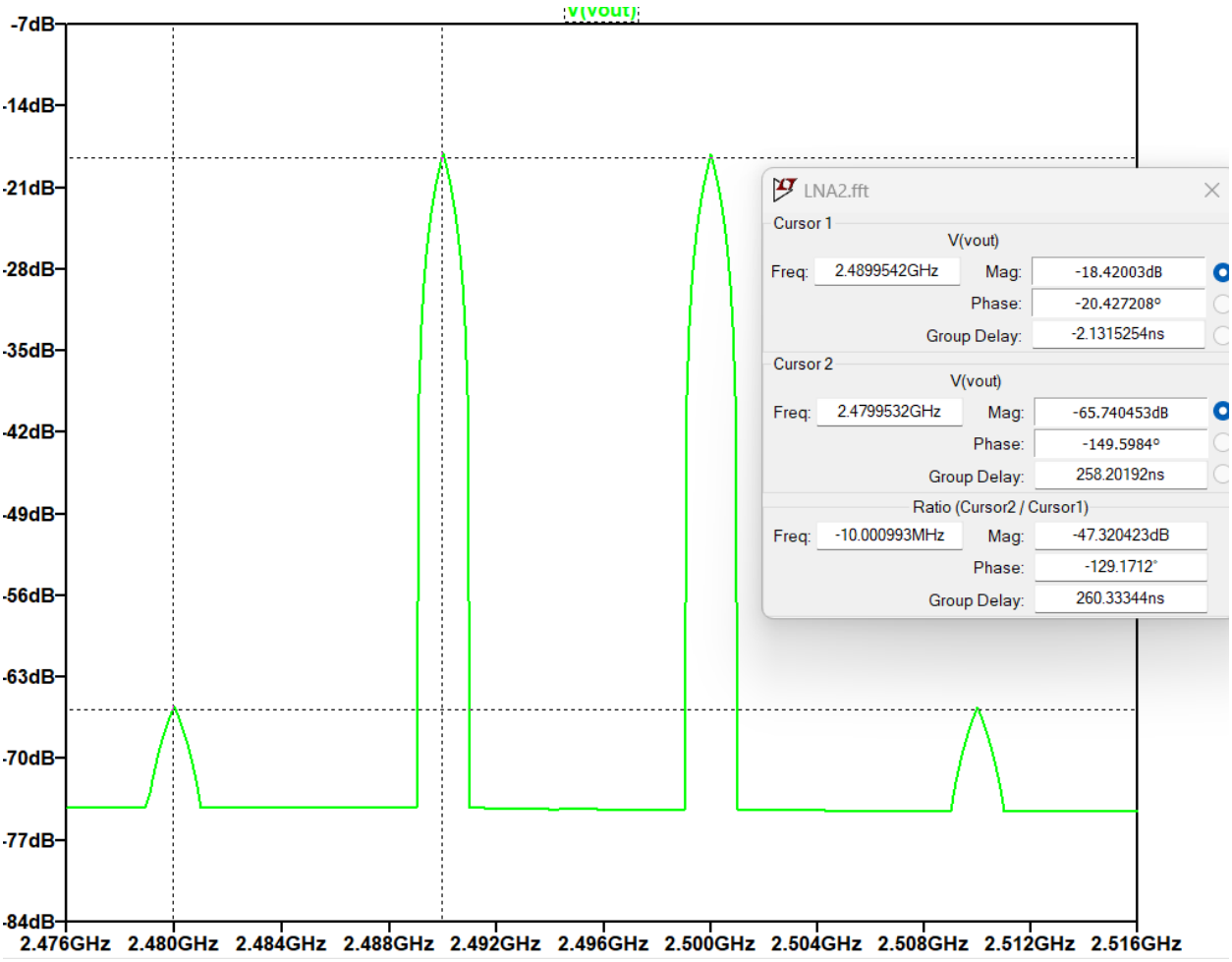
1.6 Noise Figure



NF plot from 2 GHz to 3 GHz

The NF @ 2.5GHz = 1.52 dB is less than 2 dB requirement.

1.7 IIP3



IIP3 plot

$$OIP3 = P_{OUT} + \frac{\Delta P}{2} \tag{1}$$

$$IIP3 = OIP3 - G \tag{2}$$

$$IIP3 = -18 + \frac{47}{2} - 32 = -26.5dB \tag{3}$$

IIP3 = -26.5 dBm is greater than -30 dBm requirement.

1.8 Netlist

```
* C:\Users\sriji\Desktop\Srijith Reddy\Semesters\sem 8\ICWC\mos65nm_models\LNA2.asc
M1 N004 N007 N008 0 NMOS l={L} w={W} ad='2*65n*{W}' as='2*65n*{W}' pd='2*(2*65n+{W})' ps='2*(2*65n+{W})' m={M}
L1 N008 N009 1n
L2 N006 N007 10n
M2 Vout N001 N004 0 NMOS l={L} w={W} ad='2*65n*{W}' as='2*65n*{W}' pd='2*(2*65n+{W})' ps='2*(2*65n+{W})' m={M}
L3 N001 N002 10n
R1 N009 0 1
CGS N008 N007 400f
V1 N005 N010 SINE(0 10m 2.5G) AC 1 Rser=50
CL Vout 0 100f
C4 N001 Vout 300f
M3 0 N003 N003 0 NMOS l={L1} w={W1} ad='2*65n*{W1}' as='2*65n*{W1}' pd='2*(2*65n+{W1})' ps='2*(2*65n+{W1})' m=1
R3 N003 N007 100k
I1 N001 N003 0.9m
R4 N002 Vout 10
C2 N003 0 1p
V2 N001 0 1.1
C5 N006 N005 2p
C6 N007 0 50f
R2 N001 Vout 1k
V3 N010 0 SINE(0 10m 2.49G) AC 1 Rser=0
.model NMOS NMOS
.model PMOS PMOS
.lib C:\Users\sriji\OneDrive\Documents\LTspiceXVII\lib\cmp\standard.mos
.include 65nm_PMOS_bulk.pm
.include 65nm_NMOS_bulk.pm
.param L=65n W=20u M=1 W1=5u L1=65n
.ac dec 1000 2G 3G
;.noise V(Vout) V1 dec 1000 2G 3G
.plot 10*log10((V(inoise)*V(inoise))/(4*k*300*50))
;.net I(RL) V1
;tran 1u
.backanno
.end
```

The Netlist(.net) and schematic(.asc) files are also attached.

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