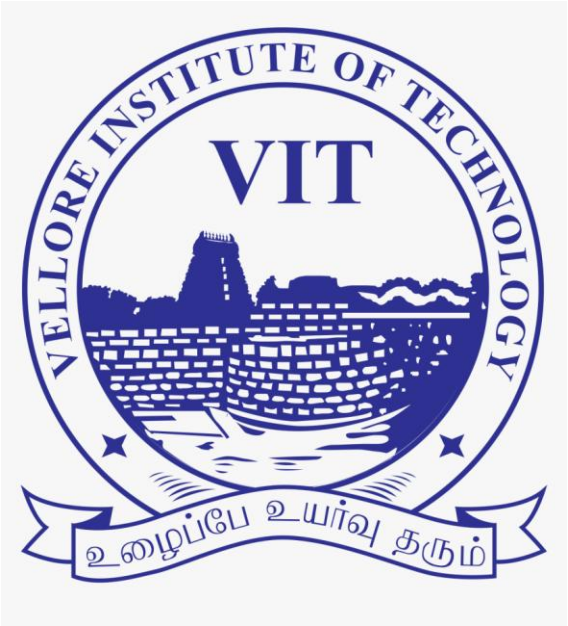
Fall Semester 2024-2025
Digital Design with FPGA Lab Report

Lab Assessment
(Task No.04)
Course Code: MVLD503P
Slot: L51+L52

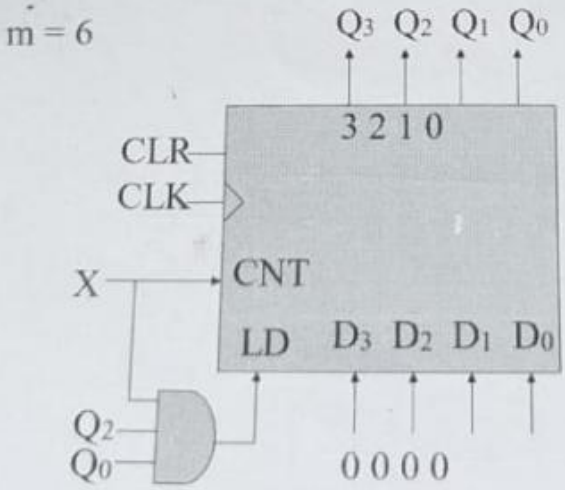


Submitted by: N. SAI SRINIVAS
Reg. No: 24MVD0089
Submitted to: Dr. Jagannadha Naidu K

3) Write the Verilog code and verify the output using the testbench.

Modulo-m Counter (m< n)

Given a mod 16 counter, construct
a mod-m counter ($0 < m < 16$) with AND, OR, NOT gates



Set LD = 1 when X = 1 and $(Q_3Q_2Q_1Q_0) = (0101)$, ie m-1

Verilog Code:

```
module mod_n_counter(clk,clr,x,q);
input clk,clr,x;
output reg [3:0]q;
wire ld;
parameter n=8;

assign ld=(x&&(q==n-1))?1'b1:1'b0;

always @(posedge clk or posedge clr)
begin
if(clr)
q<=4'b0;
```

```
else if(ld)
q<=4'b0;
else
q<=q+1;
end

endmodule
```

Verilog Test Bench:

```
module mod_n_counter_tb;
reg clk,clr,x;
wire[3:0] q;

mod_n_counter n1(clk,clr,x,q);

always #5 clk=~clk;

initial begin
clk=0; clr=1;
#20;
clr=0; x=0;
#50;
x=1;
#100;
$stop;
end
endmodule
```

Simulation Results: