Course Code	UCS20D05J	Course Name	COMPUTER ORGANIZATION AND ARCHITECTURE	Course Category	E	Discipline Specific Elective	L	T	P	C
							4	0	4	6

Pre-requisite Courses	Nil	Co-requisite Courses	Nil	Progressive Courses	Nil
Course Offering Department	Computer Science	Data Book / Codes/Standards	Nil		

Course Learning Rationale (CLR):	*The purpose of learning this course is to:*
CLR-1 :	*Utilize the functional units of a computer*
CLR-2 :	*Analyze the functions of arithmetic Units like adders, multipliers , etc*
CLR-3 :	*Understand the concepts of Pipelining and basic processing units*
CLR-4 :	*Study about parallel processing and performance considerations.*
CLR-5 :	*Have a detailed study on Input-Output organization and Memory Systems.*
CLR-6 :	*Simulate simple fundamental units like half adder, full adder, etc*

Course Learning Outcomes (CLO):	*At the end of this course, learners will be able to:*	Learning			Program Learning Outcomes (PLO)														
		1	2	3	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
		Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)	Fundamental Knowledge	Application of Concepts	Link with Related Disciplines	Procedural Knowledge	Skills in Specialization	Ability to Utilize Knowledge	Skills in Modeling	Analyze, Interpret Data	Investigative Skills	Problem Solving Skills	Communication Skills	Analytical Skills	ICT Skills	Professional Behavior	Life Long Learning
CLO-1 :	*Identify the computer hardware and how software interacts with computer hardware*	3	80	70	L	H	-	H	L	-	-	-	L	L	-	H	-	-	-
CLO-2 :	*Apply Boolean algebra as related to designing computer logic, through simple combinational and sequential logic circuits*	3	85	75	M	H	L	M	L	-	-	-	M	L	-	H	-	-	-
CLO-3 :	*Analyze the detailed operation of Basic Processing units and the performance of pipelining*	3	75	70	M	H	M	H	L	-	-	-	M	L	-	H	-	-	-
CLO-4 :	*Analyze the concepts of parallelism and multi-core processors*	3	85	80	M	H	M	H	L	-	-	-	M	L	-	H	-	-	-
CLO-5 :	*Identify the memory technologies, input-output systems and evaluate the performance of memory system*	3	85	75	H	H	M	H	L	-	-	-	M	L	-	H	-	-	-
CLO-6 :	*Identify the computer hardware, software and its interactions*	3	80	70	L	H	-	H	L	-	-	-	L	L	-	H	-	-	-

Duration (hour)		24	24	24	24	24
S-1	SLO-1	*Functional Units of a computer*	*Addition of Signed numbers*	*Fundamental concepts of basic processing unit*	*Parallelism*	*Memory systems- Basic concepts*
	SLO-2	*Operational concepts*	*Subtraction of Signed numbers*	*Performing ALU operation*	*Need of Parallelism*	*Memory hierarchy*
S-2	SLO-1	*Bus structures*	*Problem Solving*	*Execution of complete instruction*	*Types of Parallelism*	*Memory hierarchy*
	SLO-2	*Bus structures*	*Design of fast adders*	*Branch instruction*	*Applications of Parallelism*	*Memory technologies*
S-3	SLO-1	*Memory locations and addresses*	*Ripple carry adder*	*Multiple bus organization*	*Parallelism in Software*	*RAM*
	SLO-2	*Memory locations and addresses*	*Carry look ahead adder*	*Multiple bus organization*	*Instruction level parallelism*	*Semiconductor RAM*
S-4	SLO-1	*Memory operations*	*Multiplication of positive numbers*	*Hardwired control*	*Instruction level parallelism*	*ROM, Types*
	SLO-2	*Memory operations*	*Problem Solving*	*Generation of control signals*	*Data level parallelism*	*Speed, size cost*
S 5-8	SLO-1	*Laboratory 1: To recognize various components of PC- input Output systems Processing and Memory units*	*Laboratory 4:Study of TASM Addition and Subtraction of 8-bit number*	*Laboratory 7:Design of Half Adder Design of Full Adder*	*Laboratory 10: Study of Array Multiplier Design of Array Multiplier*	*Laboratory 13: Study of Carry Save Multiplication Program to carry out Carry Save Multiplication*
	SLO-2					
S-9	SLO-1	*Instructions*	*Signed operand multiplication*	*Micro-programmed control*	*Challenges in parallel processing*	*Cache memory*
	SLO-2	*Instruction sequencing*	*Problem solving*	*Microinstruction*	*Architectures of parallel Systems*	*Cache memory*
S-10	SLO-1	*Addressing modes*	*Fast multiplication*	*Microinstruction*	*Flynn's Classification*	*Mapping Functions*
	SLO-2	*Problem solving*	*Problem Solving*	*Micro-program Sequencing*	*Flynn's Classification*	*Replacement Algorithms*
S-11	SLO-1	*Introduction to Microprocessor*	*Bit pair recoding of Multipliers*	*Micro instruction with Next address field*	*SISD*	*Replacement Algorithms*
	SLO-2	*Introduction to Assembly language*	*Problem Solving*	*Basic concepts of pipelining*	*SIMD*	*Problem Solving*
S-12	SLO-1	*Writing of assembly language programming*	*Carry Save Addition of summands*	*Pipeline Performance*	*MIMD*	*Virtual Memory*
	SLO-2	*Writing of assembly language programming*	*Problem Solving*	*Pipeline Performance*	*MISD*	*Performance considerations of various memories*
S 13-16	SLO-1	*Laboratory 2: To understand how different components of PC are connected to work properly*	*Laboratory 5: Addition of 16-bit number Subtraction of 16-bit number*	*Laboratory 8: Study of Ripple Carry Adder Design of Ripple Carry Adder*	*Laboratory 11:Study of Booth Algorithm*	*Laboratory 14:Understanding Processing unit*
	SLO-2					

		Assembling of System Components				
S-17	SLO-1	*ARM Processor: The thumb instruction set*	*Integer division*	*Pipeline Hazards*	*Uni-Processor*	*Input Output Organization*
	SLO-2	*Processor and CPU cores*	*Restoring Division*	*Data hazards*	*Multiprocessors*	*Input Output Organization*
S-18	SLO-1	*Processor and CPU cores*	*Solving Problems*	*Methods to overcome Data hazards*	*Multi-core processors*	*Need for input output devices*
	SLO-2	*Instruction Encoding format*	*Non Restoring Division*	*Instruction Hazards*	*Multi-core processors*	*Memory mapped IO*
S-19	SLO-1	*Memory Load and Store in ARM*	*Solving Problems*	*Hazards on conditional and Unconditional Branching*	*Memory in Multiprocessor Systems*	*Program controlled IO*
	SLO-2	*Memory Load and Store in ARM*	*Floating point numbers*	*Control hazards*	*Memory in Multiprocessor Systems*	*Interrupts - Hardware*
S-20	SLO-1	*Basics of IO operations*	*Operations*	*Control hazards*	*Cache Coherency in Multiprocessor Systems*	*Enabling and Disabling interrupts*
	SLO-2	*Basics of IO operations*	*Solving Problems*	*Influence of hazards on instruction sets*	*Cache Coherency in Multiprocessor Systems*	*Handling multiple Devices*
S 21-24	SLO-1 SLO-2	*Laboratory 3: To understand how different components of PC are connected to work properly* *Disassembling of System Components*	*Laboratory 6: Multiplication of 8-bit number* *Factorial of a given number*	*Laboratory 9: Study of Carry Look-ahead Adder* *Design of Carry Look-ahead Adder*	*Laboratory 12: Programs to carry out Booth Algorithm*	*Lab 15:Design of primitive processing unit*

Learning Resources	1. *Carl Hamacher, ZvonkpVranesie, SahwatZaky, (2015), " Computer Organisataion", 5th Edition McGraw-Hill* 2. *Kai Hwang, Faye A.Briggs, (2016), "Computer Architecture and Parallel Processing", 3rd Edition, McGraw Hill, 2016* 3. *Ghost T.K, (2011), "Computer Oraganization and Architecture", 3rd Edition, Tata McGraw-Hill* 4. *P.Hayes, (2015), "Computer Architecture and Organization", 3rd Edition, McGraw Hill*	5. *William Stallings, (2015), "Computer Organization and Architecture-Designing for Performance", 10th Edition, Pearson Education* 6. *David A. Patterson and John L Hennessy, (2014), "Computer Organization and Design- A Hardware Software Interface", 5th Edition, Morgan Kaufman,*

Learning Assessment											
Bloom's Level of Thinking		Continous Learning Assessment(50% Weightage)								Final Examination (50% weightage)	
		CLA – 1 (10%)		CLA – 2 (10%)		CLA – 3 (20%)		CLA – 4# (10%)			
		Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice
Level 1	Remember	20%	20%	15%	15%	15%	15%	15%	15%	15%	15%

	Understand										
Level 2	Apply	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%
	Analyze										
Level 3	Evaluate	10%	10%	15%	15%	15%	15%	15%	15%	15%	15%
	Create										
	Total	100 %		100 %		100 %		100 %		100%	

CLA – 4 can be from any combination of these: Assignments, Seminars, Tech Talks, Mini-Projects, Case-Studies, Self-Study, MOOCs, Certifications, Conf. Paper etc

Course Designers		
Experts from Industry	**Experts from Higher Technical Institutions**	**Internal Experts**
Mr. S. Karthik, IT Analyst, Tata Consultancy Services	Dr. Neelanarayanan,, Professor, School of Computer Science and Engineering, VIT Chennai	Mrs.A.Pavithra
		Mr.M.R.Vinodh

Course Code	UCS20D06J	Course Name	ARTIFICIAL INTELLIGENCE	Course Category	E	Discipline Specific Elective	L	T	P	C
							4	0	4	6

Pre-requisiteCourses	Nil	Co-requisiteCourses	Nil	ProgressiveCourses	Nil
Course OfferingDepartment	Computer Science	Data Book / Codes/Standards	Nil		

Course Learning Rationale (CLR):	The purpose of learning this course is to:	Learning		
		1	2	3
CLR-1 :	Discover problems that are agreeable to solution by AI methods.	Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)
CLR-2 :	Study the basics of designing intelligent agents that can solve general purpose problems			
CLR-3 :	Discover appropriate AI methods to solve a given problem			
CLR-4 :	Perform intellectual task as decision making, problem solving, perception, understanding			
CLR-5 :	Formalize a given problem using different AI methods			
CLR-6 :	Provides adaptive learning			

Course Learning Outcomes (CLO):	At the end of this course, learners will be able to:	Learning		
		1	2	3
CLO-1 :	Demonstrate fundamental understanding of the history of artificial intelligence and its	3	80	70

Program Learning Outcomes (PLO)														
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Fundamental Knowledge	Application of Concepts	Link with Related Disciplines	Procedural Knowledge	Skills in Specialization	Ability to Utilize Knowledge	Skills in Modeling	Analyze, Interpret Data	Investigative Skills	Problem Solving Skills	Communication Skills	Analytical Skills	ICT Skills	Professional Behavior	Life Long Learning
L	H	-	H	L	-	-	-	L	L	-	H	-	-	-