Learning Assessment											
Bloom's Level of Thinking		Continous Learning Assessment(50% Weightage)								Final Examination (50% weightage)	
		CLA – 1 (10%)		CLA – 2 (10%)		CLA – 3 (20%)		CLA – 4# (10%)			
		Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice	Theory	Practice
Level 1	Remember	20%	20%	15%	15%	15%	15%	15%	15%	15%	15%
	Understand										
Level 2	Apply	20%	20%	20%	20%	20%	20%	20%	20%	20%	20%
	Analyze										
Level 3	Evaluate	10%	10%	15%	15%	15%	15%	15%	15%	15%	15%
	Create										
	Total	100 %		100 %		100 %		100 %		100%	

CLA – 4 can be from any combination of these: Assignments, Seminars, Short Talks, Mini-Projects, Case-Studies, Self-Study, MOOCs, Certifications, Conf. Paper etc

.,**Course Designers**		
Experts from Industry	**Experts from Higher Technical Institutions**	**Internal Experts**
Mr. S. Karthik, IT Analyst, Tata Consultancy Services	Dr. Neelanarayanan,, Professor, School of Computer Science and Engineering, VIT Chennai	1.Mrs. S. Usha, SRMIST 2.Dr. P.J.Arul Leena Rose 3. Dr.J.Padmavathi

Courrse Code	**USA20102J**	Course Name	**DIGITAL LOGIC FUNDAMENTALS**	Course Category	**C**	**Professional Core**	L	T	P	C
							4	0	2	5

Pre-requisite Courses	Nil	Co-requisite Courses	Nil	Progressive Courses	Nil
Course Offering Department	Computer Science	Data Book / Codes/Standards	Nil		

Course Learning Rationale (CLR):	The purpose of learning this course is to:
CLR-1 :	To learn the concepts of basics of Digital Logics
CLR-2 :	To impart in-depth knowledge of Logic Gates
CLR-3 :	Understand the principles of Boolean algebra
CLR-4 :	Basic knowledge of Combinational circuits and it applications
CLR-5 :	Basic knowledge of sequential circuits and it applications
CLR-6 :	Design principles of counters

Course Learning Outcomes (CLO):	At the end of this course, learners will be able to:	Learning		
		1	2	3
		Level of Thinking (Bloom)	Expected Proficiency (%)	Expected Attainment (%)
CLO-1 :	Have a thorough Understanding of Fundamentals of Digital Logic and IT Fundamentals	3	80	70
CLO-2 :	Understand the concepts of logic gates and its uses	3	85	75
CLO-3 :	Real time applications of Boolean algebra	3	75	70
CLO-4 :	Design and implementation knowledge of Combinational circuits	3	85	80
CLO-5 :	Design and implementation knowledge of sequential circuits	3	85	75
CLO-6 :	Real time application of Counters	3	80	70

Program Learning Outcomes (PLO)														
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Engineering Knowledge	Problem Analysis	Design & Development	Analysis, Design, Research	Modern Tool Usage	Society & Culture	Environment & Sustainability	Ethics	Individual & Team Work	Communication	Project Mgt. & Finance	Life Long Learning	PSO - 1	PSO - 2	PSO – 3
H	H	M	-	-	-	-	-	H	H	-	-	M	H	H
H	H	H	H	H	-	M	-	H	H	-	-	M	H	H
H	H	M	H	H	-	M	-	H	H	-	-	M	H	H
H	H	H	-	-	-	-	-	H	M	-	-	M	H	H
H	M	M	M	M	M	M	-	H	H	-	M	M	H	H
H	H	M	-	-	-	-	-	H	H	-	-	M	H	H

Duration (Hour)		18	18	18	18	18
S-1	SLO-1	Number System and its types	Minterms and Maxterms	Combinational Logic - Introduction	Sequential Circuit - Introduction	Counters - Introduction
	SLO-2	Base conversions	Sum of Products	Designing of a Logic Circuit Diagram	Latches	A Basic Design Counter
S-2	SLO-1	Binary codes and its types	Product of Sums methods	Adders : Quarter, Half and Full Adders	Flip Flops - Introduction	Classification of Counters
	SLO-2	Code conversions	Conversions of SOP to POS	Subtractors:Half, Full Subtractors	RS Flip Flop	Asynchronous Counters
S-3	SLO-1	Basics of Logic Gates and Derived Gates	Simplifying Boolean Expressions using theorems	Design of Adder Circuits	JK Flip Flop	Synchronous Counters
	SLO-2					
S-4	SLO-1	Truth Tables	Derivation of a Boolean Functions	Design of Subtractor Circuits	D Flip Flop	SynVsAsyn Counters
	SLO-2					
S 5-6	SLO-1	Laboratory1 : Verification of Basic Gates and Derived	Laboratory 4: Verifications of Distributive Law	Laboratory 7: Half Adder and Full Adder	Laboratory 10: Implementation of DeMultiplexer	Laboratory 13: Ring Counters
	SLO-2					

		Gates				
S-7	SLO-1	Universality of NAND Gate	Karnaugh Map - Introduction and its uses	Multiplexer	T - Flip Flop	Ripple Counters
	SLO-2	Universality of NOR Gate	Types of K-Map	Implementation of a Boolean expression using a Multiplexer	Edge Triggered	MOD Counters
S-8	SLO-1	Duality of Logic Gate Representation	Rules for constructing K-Map	De Multiplexer	Master Slave Flip Flop	UP DOWN Counters
	SLO-2					
S-9	SLO-1	Boolean Algebra - Introduction	Two and Three Variable K-Map	Encoder	Registers Architecture	Ring Counter
	SLO-2					
S-10	SLO-1	Logical Operations AND OR NOT	Four Variable K-Map	Decoder	Shift Registers	Shift Counters
	SLO-2					
S 11-12	SLO-1	Laboratory2:NAND as Universal Gate	Laboratory 5-Simplifying Boolean Expressions using theorems	Laboratory 8:Half Subtractor and Full Subtractor	Laboratory 11: Implementation of Shift Registers and Serial Transfer	Laboratory 14: Implementation of DOWN Counter
	SLO-2	NOR as Universal Gate				
S-13	SLO-1	Evaluating Logic Circuits	Don't Care conditions	Parity Generator	Four-bit Serial in Serial Out Shift register	Memory - Introduction
	SLO-2	Implementing Circuits from Boolean Expressions	Determination Prime Implicant Method	Parity Checker	Shift Registers Operations	Basic terms and ideas
S-14	SLO-1	Boolean Functions	Boolean Arithmetic - Introduction	Checksum	Serial-to-Parallel Shift Register	Magnetic Memories
	SLO-2	Duality Principle, Complements	Binary Addition	Code Conversions	Design of Serial to Parallel	Memory Addressing
S-15	SLO-1	Laws and Theorems	Binary Subtractions	Programmable Array Logic	Parallel-to-Serial Shift Register	Types of ROM
	SLO-2					
S-16	SLO-1	Laws of Intersection, Union, Absorption, Involution, Demargan's Theorems	Various Representation of Binary Numbers	Programmable Logic Array	Design of Parallel to serial	Types of RAM
	SLO-2					
S 17-18	SLO-1	Laboratory 3:Laws of Boolean Expressions	Laboratory 6: Implementation fo Binary Addition and Subtraction	Laboratory 9: Implementation of Multiplexer	Laboratory 12: Four Bit Binary Shift Counters	Laboratory 15: Implementation of DOWN Counter
	SLO-2					

Learning Resources	1. AnanthiSheshasaayee, J.G. Sheshasaayee,(2005),"Digital Logic Fundamentals", Margham Publications 2. Vijayendran. V, (2003), "Digital Fundamentals", S.V. Publishers	3. Leach.D.P and Malvino.A.P, (2002), "Digital Principles and Applications", 5th Edition, TM. 4. MorisMano.M,(2001),"Digital Logic and Computer Design", 4th Edition

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