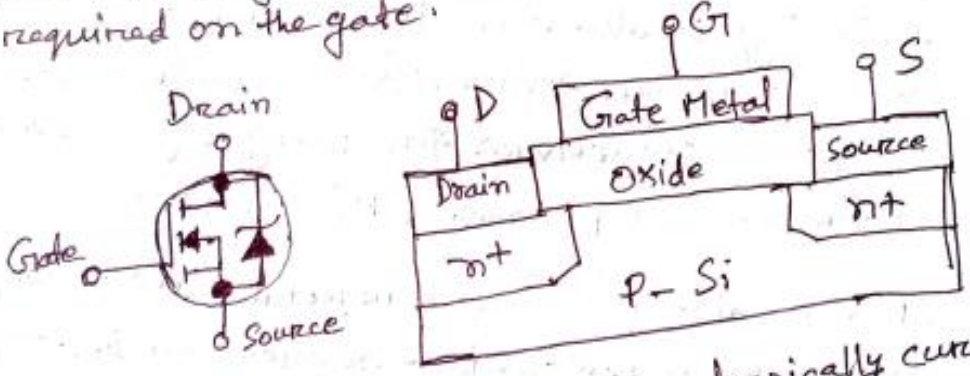
Title: Construction of MOSFET Logic Gates.

Introduction:

Technical Info: Mosfets come in four different types. They may be enhancement or depletion mode, and they may be n-channel or p-channel. For this application we are only interested in n-channel enhancement mode mosfets, and these will be the only ones talked about from now on. There are also logic-level mosfets and normal mosfets. The only difference between these is the voltage level required on the gate.



Unlike bipolar transistors that are basically current driven device. If no positive voltage is applied between gate and source the mosfet is always non-conducting. If we apply a positive voltage USG to the gate we'll set up an electric field between it and the rest of the transistor. The positive gate voltage will push away the holes inside the p-type substrate and attracts the moveable electronic in n-type region under the source and drain electrodes. The positive gate voltage therefore creates a channel in the top layer of material between oxide and p-Si. As a result the size of the channel we've made increases with the size of the gate voltage and enhances or increases the amount of current which can go from source to drain

this is why this kind of transistor is called an enhancement mode device. Hence the operation of a p-channel MOSFET is just the opposite of an n-channel MOSFET.

CMOS:

Complementary metal-oxide-semiconductor (CMOS) is a technology for contructing integrated circuits. CMOS technology is used in microprocessor, microcontroller, static RAM, and other digital logic circuits. CMOS technology is also used for several analog circuits such as image sensors, data converters, and highly integrated transceivers for many types of communication. Frank Wanlass patented CMOS in 1963.

CMOS is also sometimes refferred to as complementary symmetry metal-oxide-semiconductor. The words "complementary-symmetry" refer to the fact that the typical digital design style with CMOS users complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistors for logic functions.

Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Since one transistor of the pair is always off, the series combination draws significant power only momentarily during switching between on and

off states. Consequently, CMOS device do not produce as much waste heat as other forms of logic, for example transistor-transistor Logic (TTL) or NMOS logic, which normally have some standing current even when not changing state. CMOS also allows a high density of logic function on a chip. It was primarily for this reason that CMOS became the most used technology to be implemented in VLSI chip.

Some advantages of CMOS ove TTL are:

- CMOS gate inputs draw far less current than TTL inputs, because MOSFETs are voltage-controlled, not current-controlled, devices.
- CMOS gates are able to operate on a much wider range of power supply voltage than TTL: typically 3 to 15 volts versus 4.75 to 5.25 volts for TTL
- CMOS transistors are smaller in size and provide less power dissipation that NMOS transistors.

In this experiment, we will first look at some logic circuit design using NMOS. Then we will implement the same logic circuits using CMOS and try to identify the potential design advantages of CMOS over NMOS.

Theory and Methodology:

NMOS Inverter with ohmic/Resistive Load:

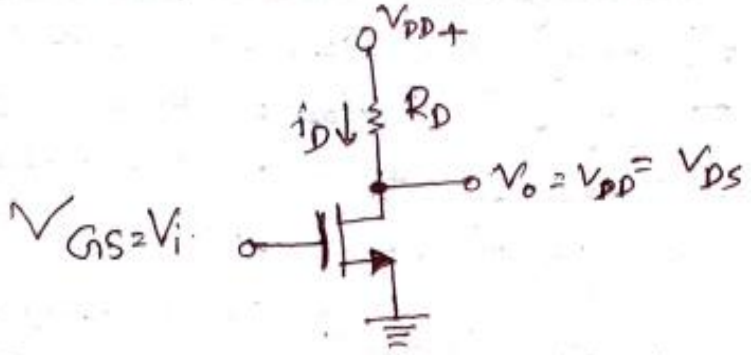


Fig.1: NMOS Inverter with ohmic/Resistive Load.

NMOS Inverter with NMOS Enhancement Transistors load:

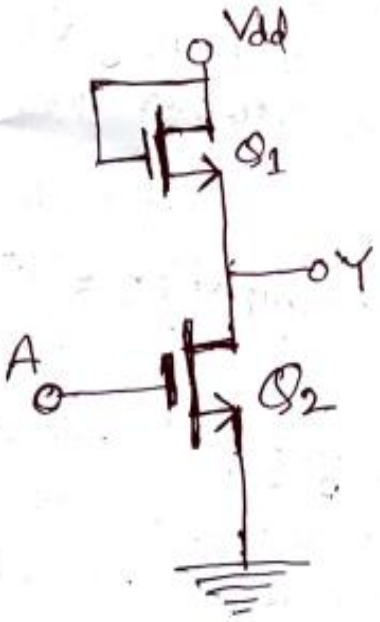


Fig.2: NMOS Inverter with NMOS Load.

NMOS NAND Gate:

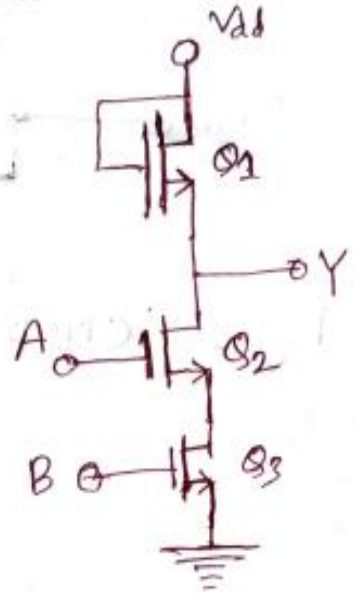


Fig. 3: NMOS NAND Gate.

NMOS NOR Gate:

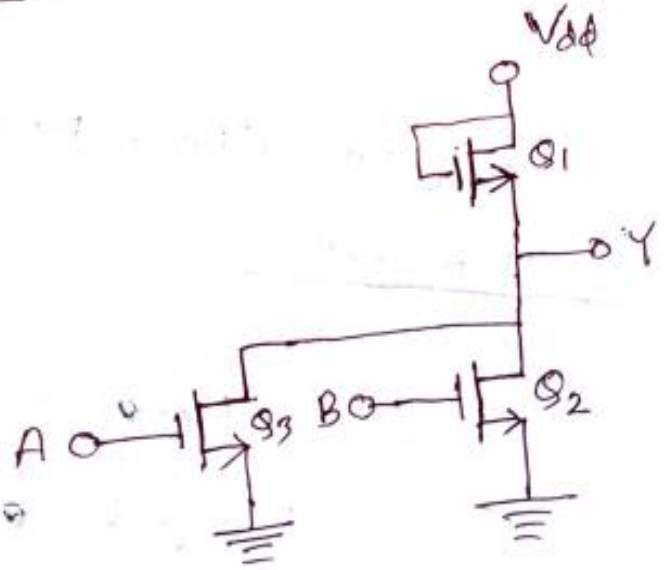


Fig. 4: NMOS NOR Gate.

CMOS Inverter :

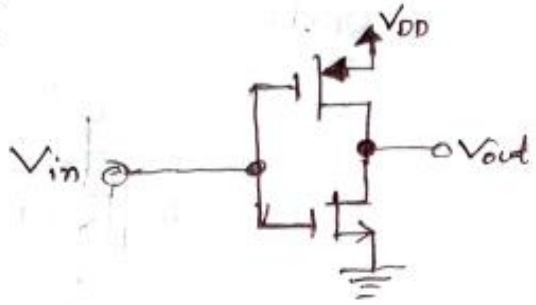


Fig. 5 : CMOS Inverter.

CMOS NAND Gate :

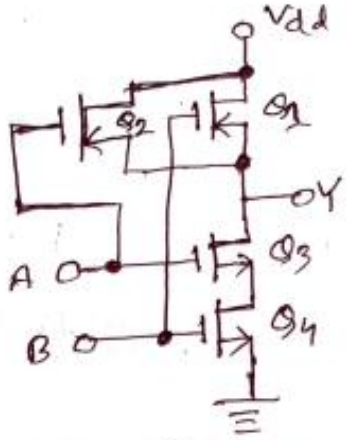


Fig. 6 : CMOS NAND Gate.

CMOS NOR Gate :

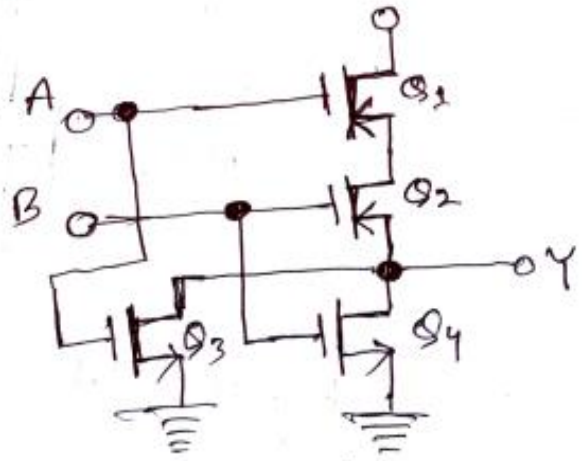


Fig. 7 : CMOS NOR Gate.

BLOCK DIAGRAM:

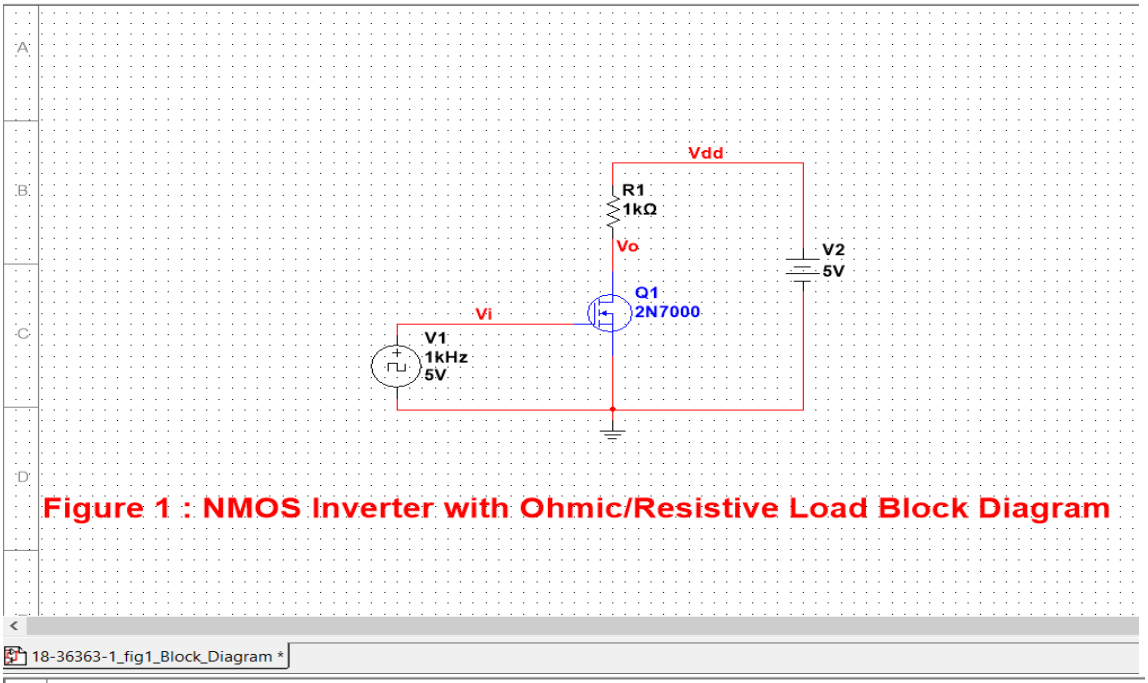


Figure 1 : NMOS Inverter with Ohmic/Resistive Load Block Diagram

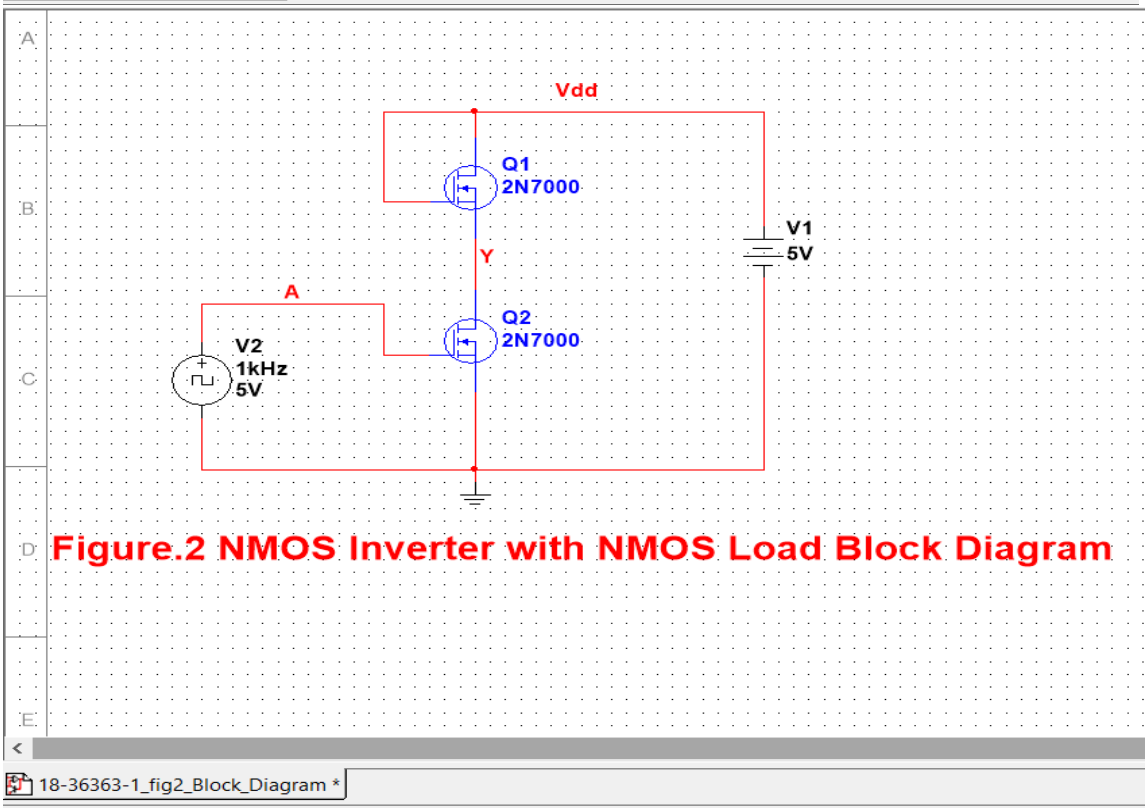


Figure.2 NMOS Inverter with NMOS Load Block Diagram

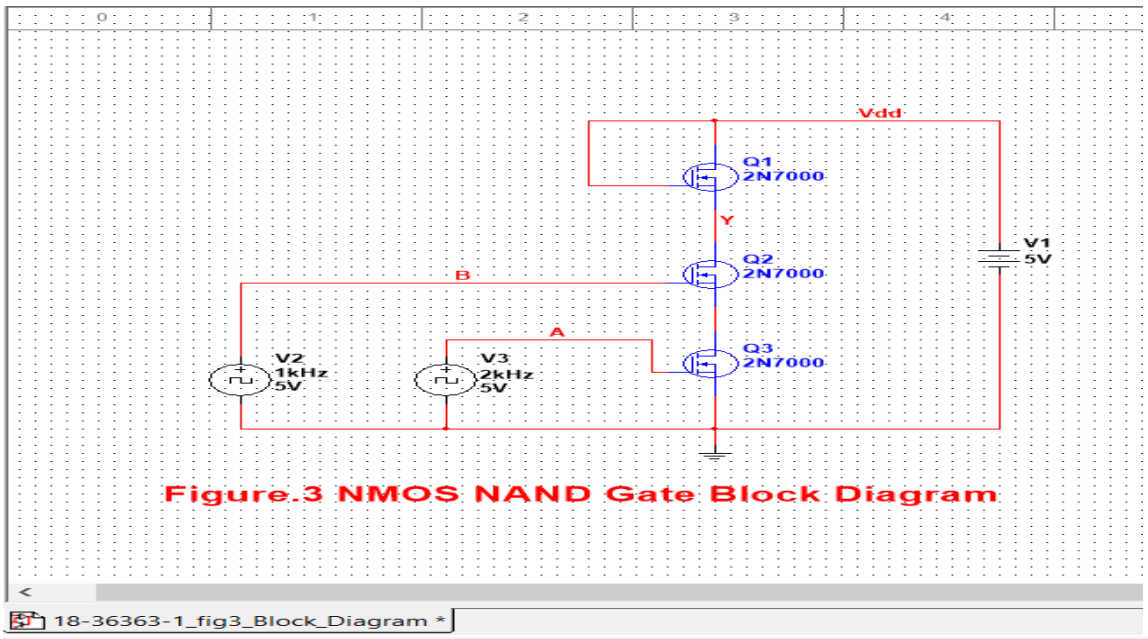


Figure.3 NMOS NAND Gate Block Diagram

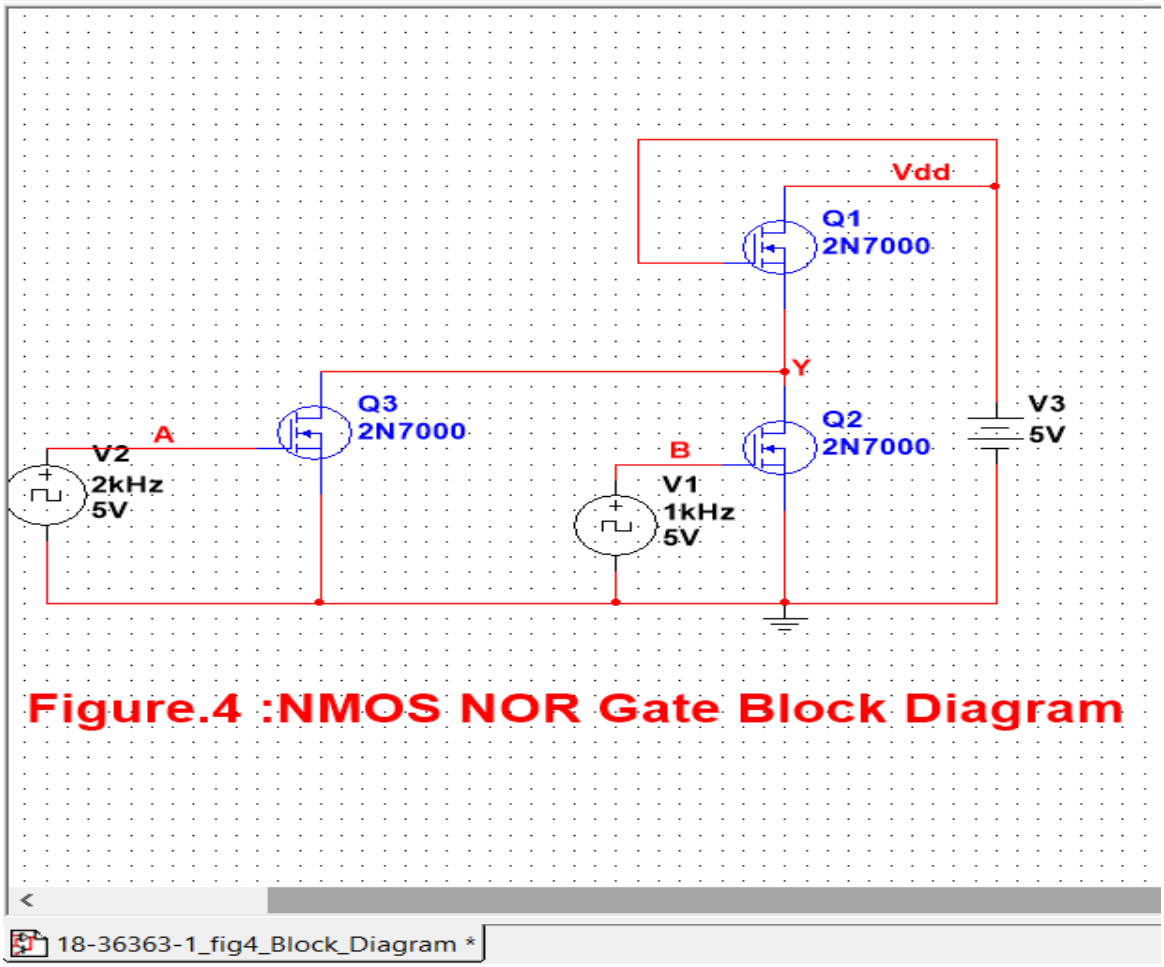


Figure.4 :NMOS NOR Gate Block Diagram

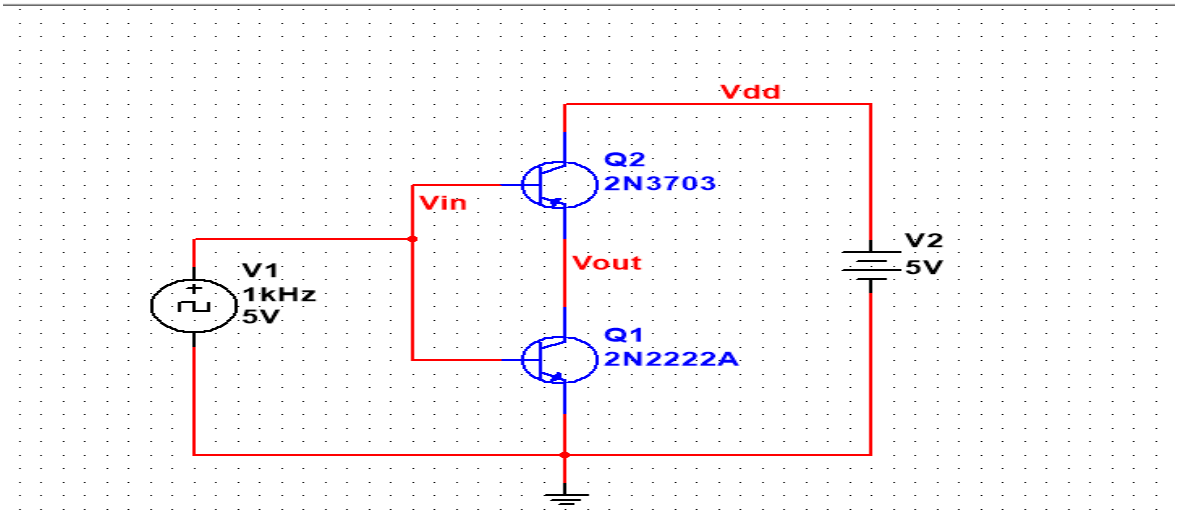


Figure 5 : CMOS Inverter Block Diagram

18-36363-1_fig5_Block_Diagram *

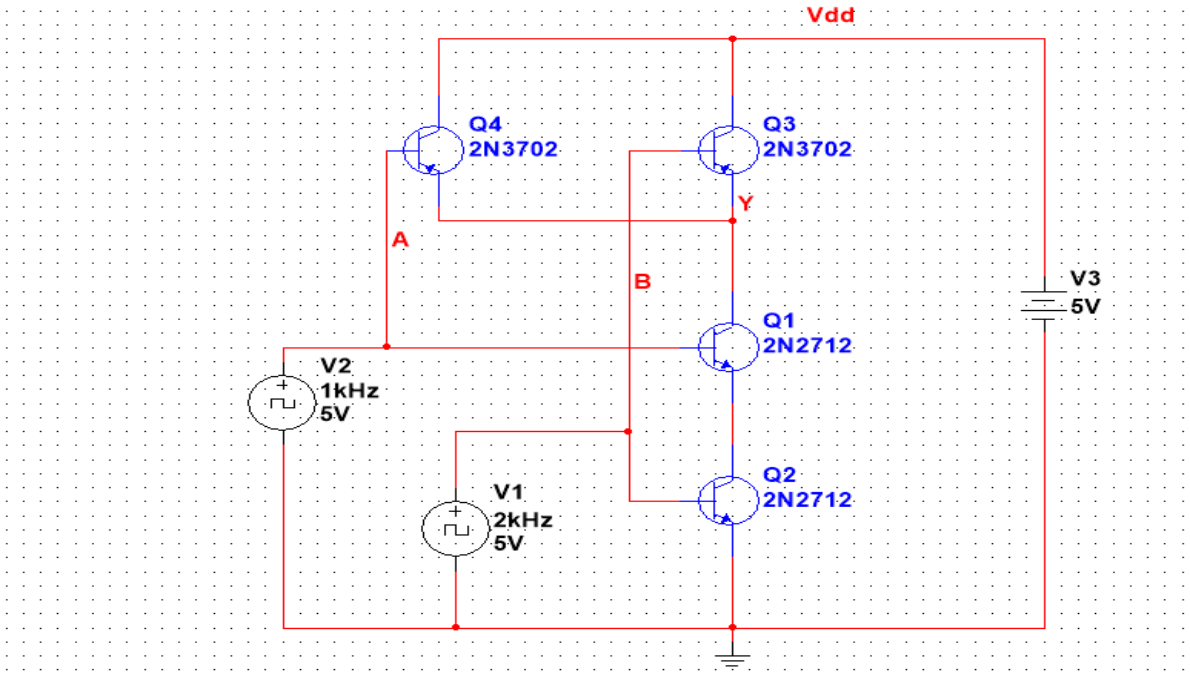


Figure.6 : CMOS NAND Gate Block Diagram

18-36363-1_fig6_Block_Diagram *

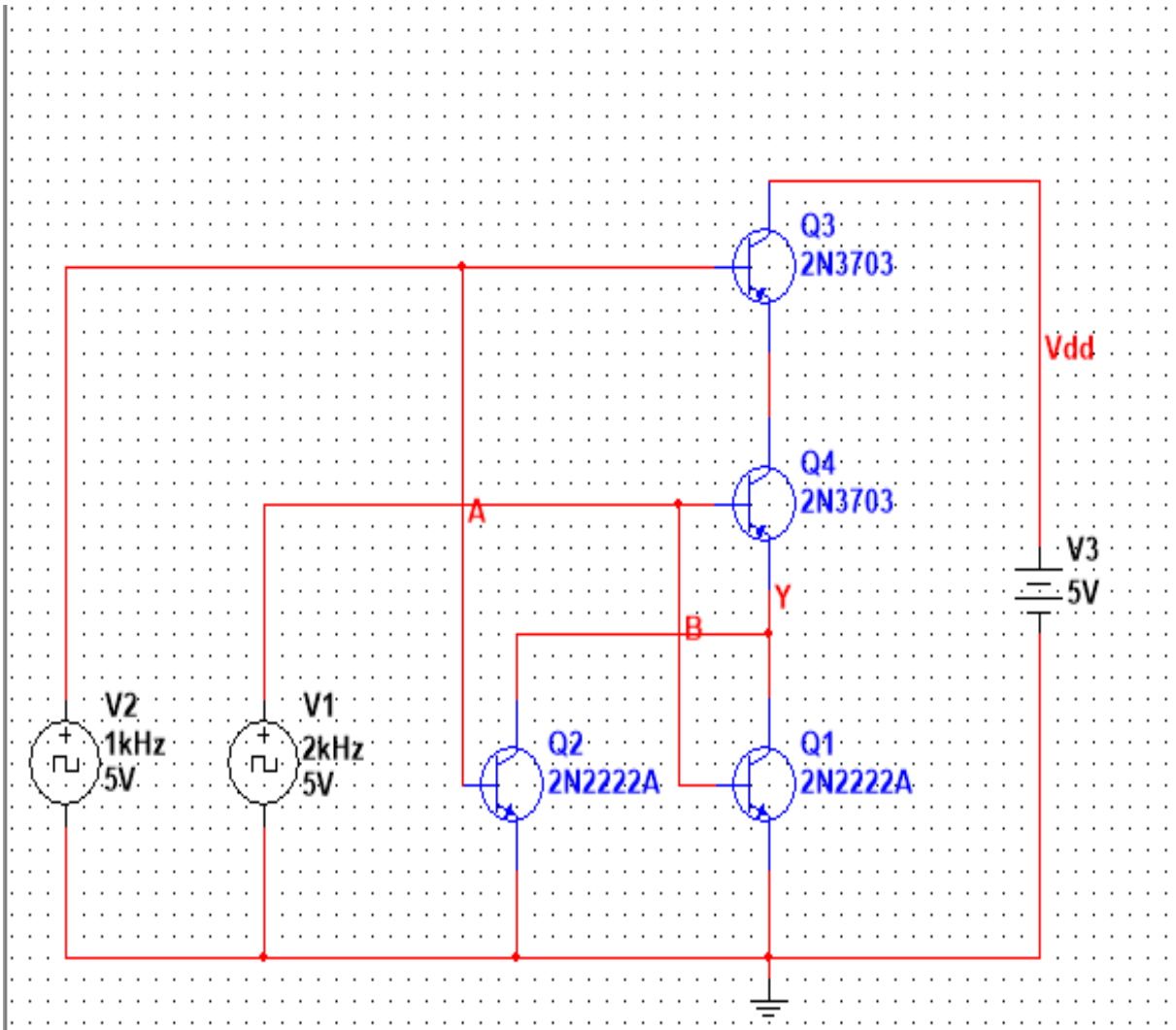


Figure 7 : CMOS NOR Gate Block Diagram

Graph:

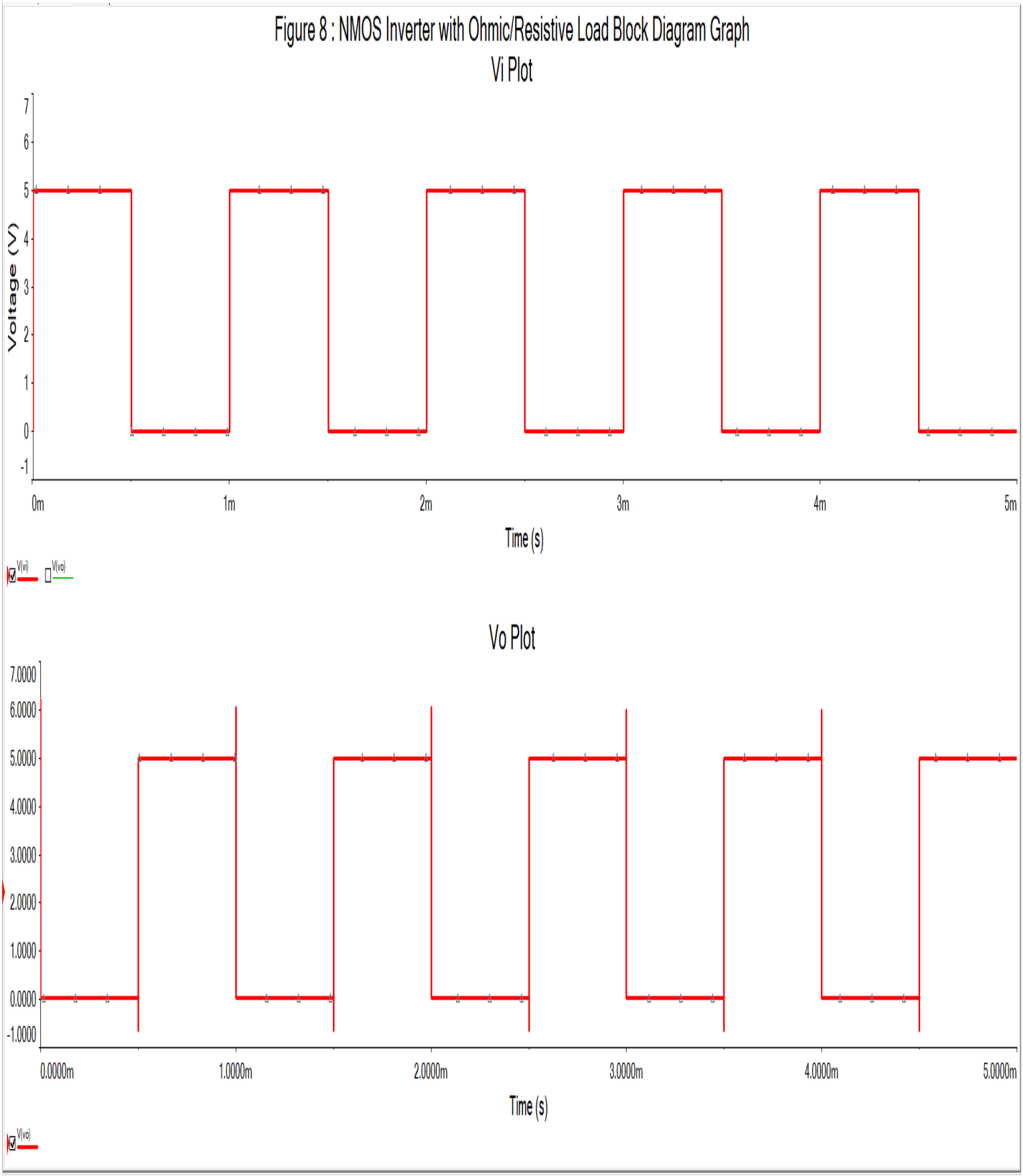
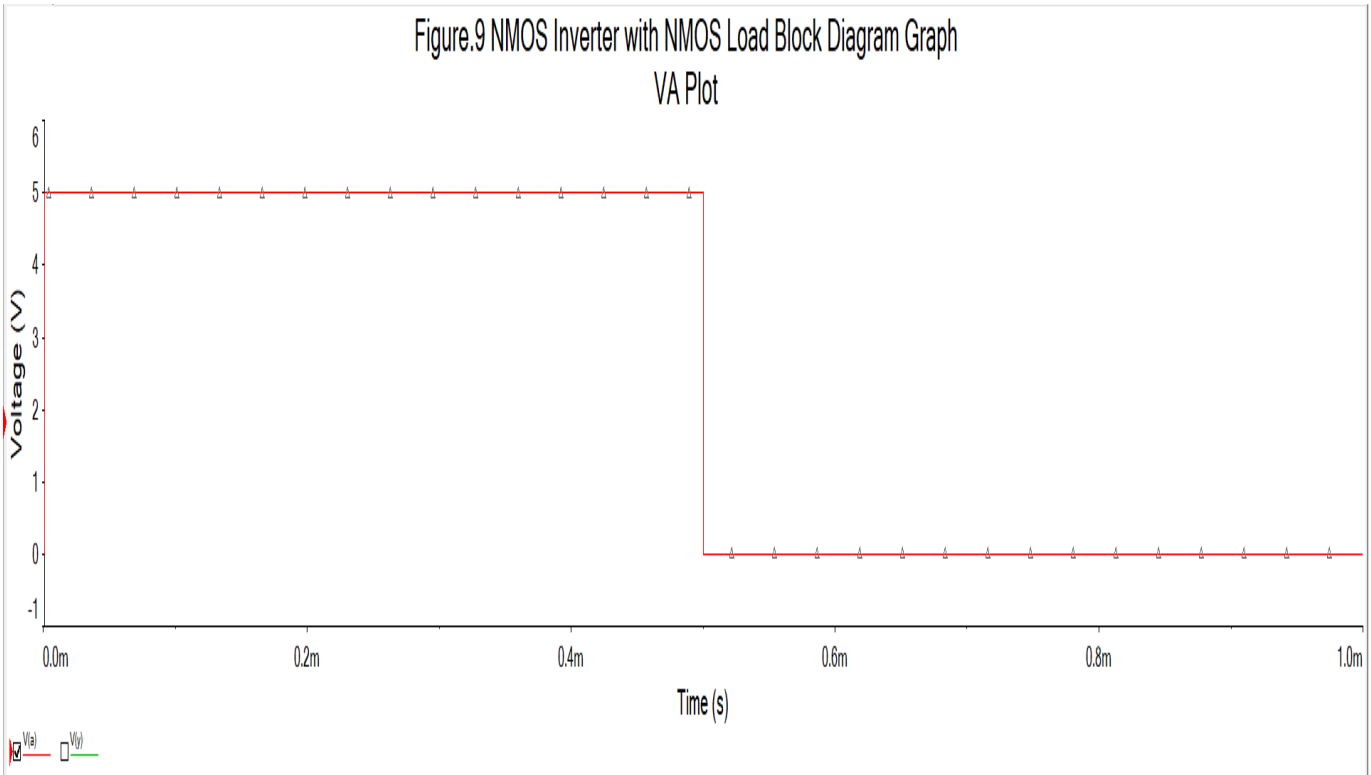


Figure 8 : NMOS Inverter with Ohmic/Resistive Load Block Diagram Graph
Vi Plot
Voltage (V)
7
6
5
4
3
2
1
0
-1
0m
1m
2m
3m
4m
5m
Time (s)
V(vi)
V(vo)
Vo Plot
7.0000
6.0000
5.0000
4.0000
3.0000
2.0000
1.0000
0.0000
-1.0000
0.0000m
1.0000m
2.0000m
3.0000m
4.0000m
5.0000m
Time (s)
V(vo)

Figure.9 NMOS Inverter with NMOS Load Block Diagram Graph



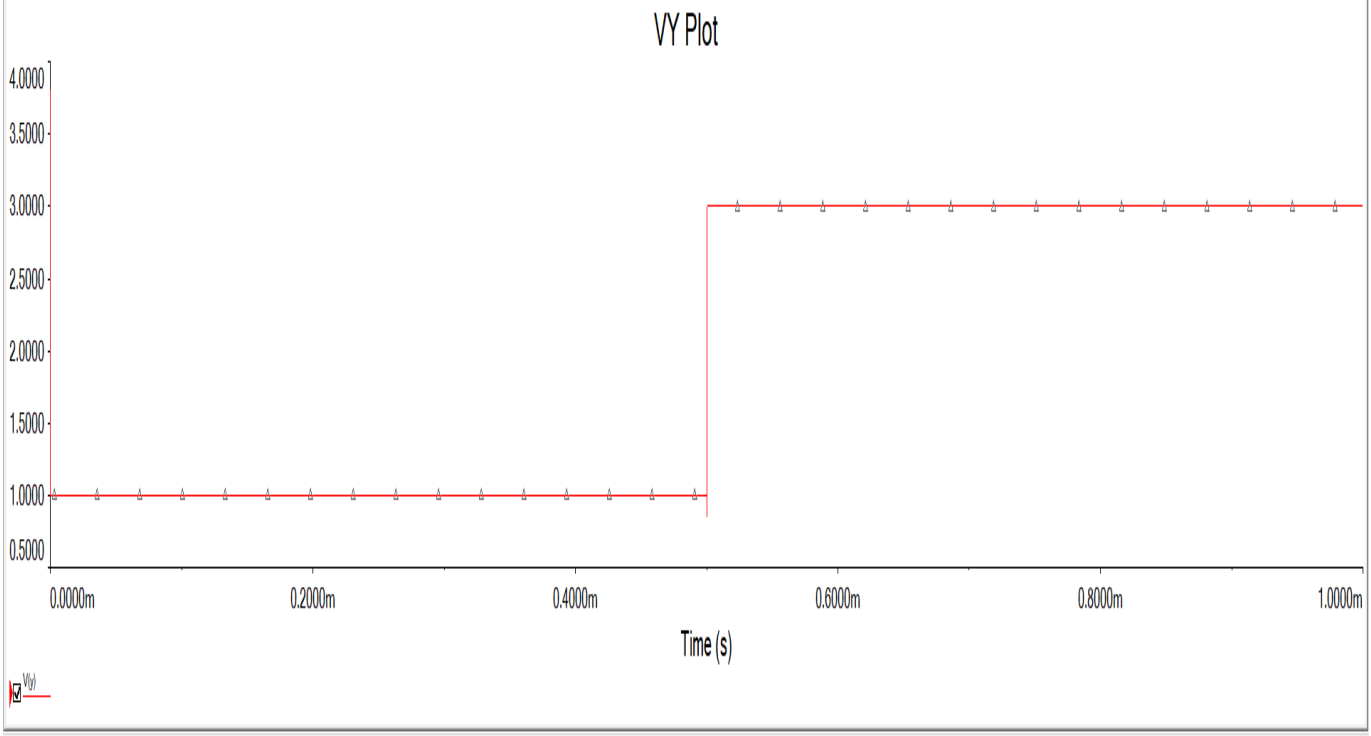


Figure.10: NMOS NAND Gate Block Diagram Graph

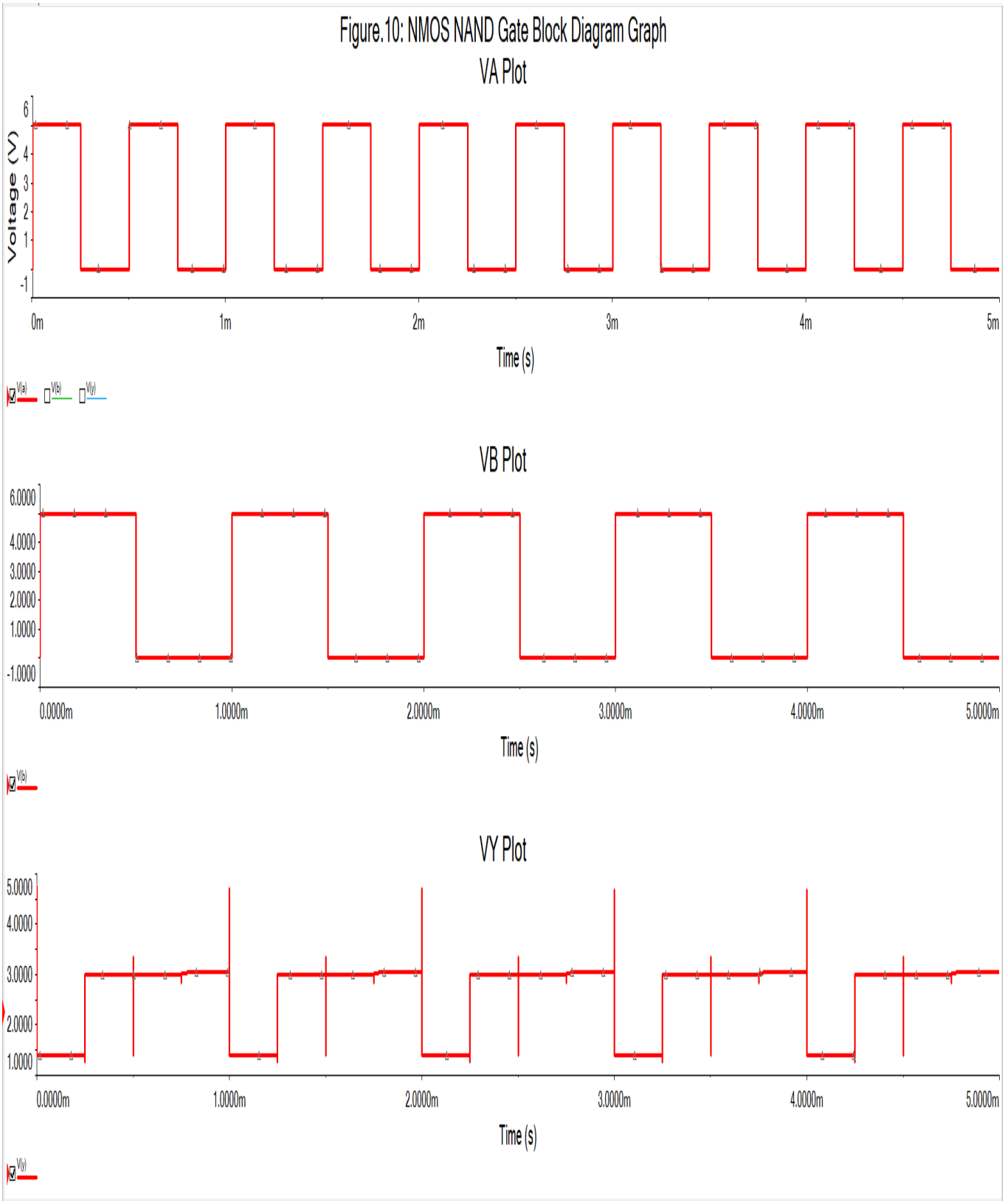


Figure.11 :NMOS NOR Gate Block Diagram Graph

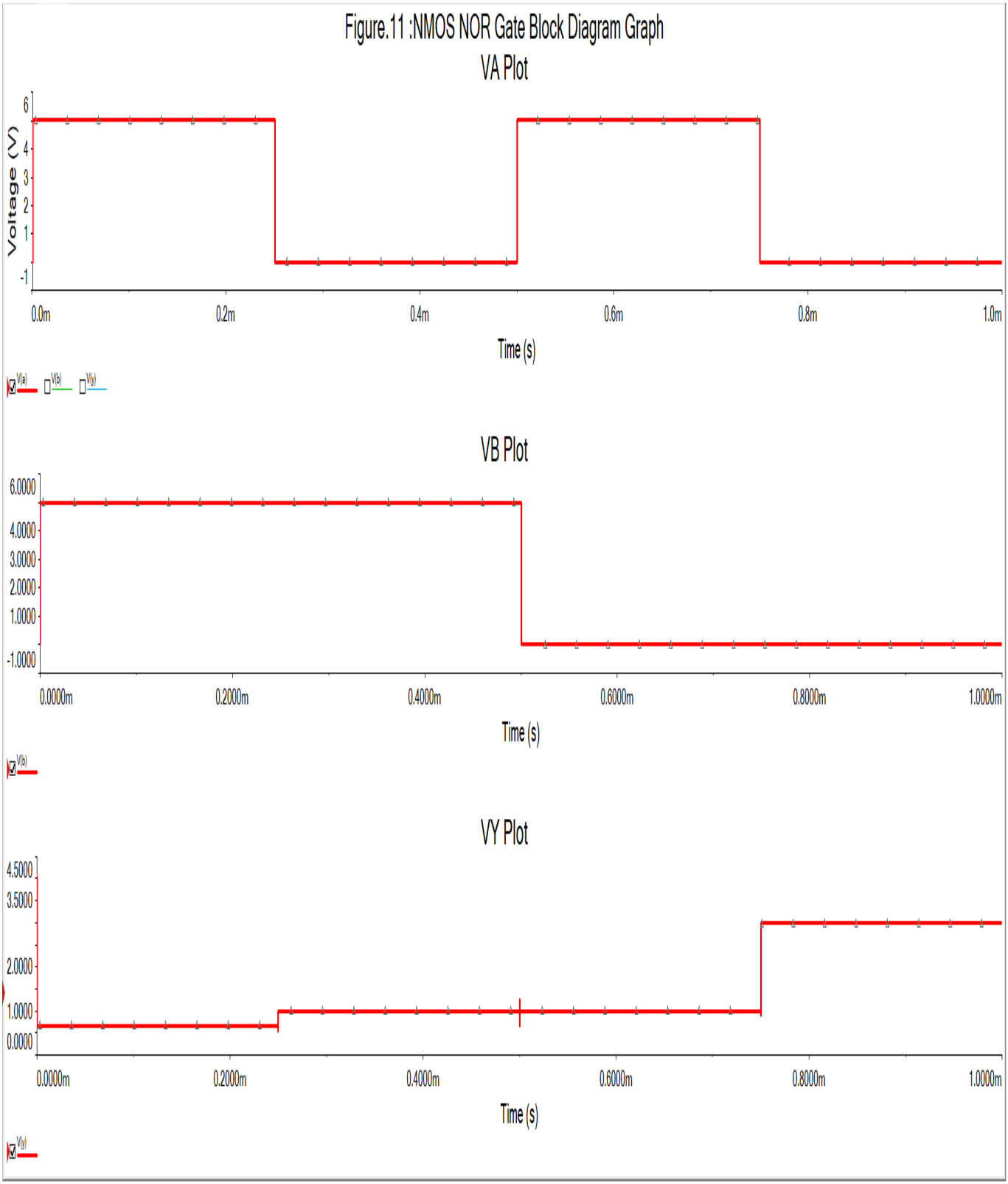


Figure 12 : CMOS Inverter Block Diagram Graph

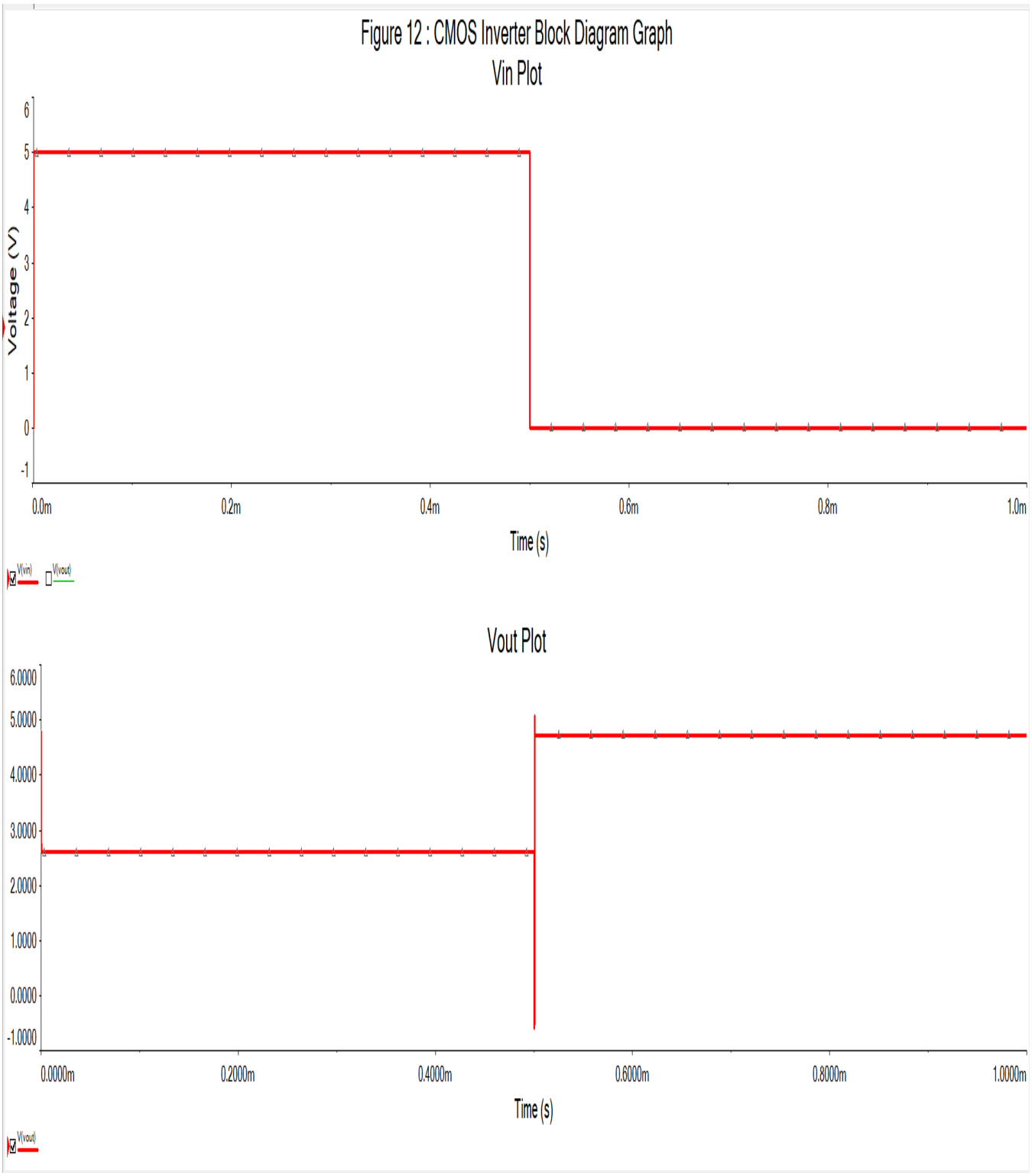


Figure.13 : CMOS NAND Gate Block Diagram Graph

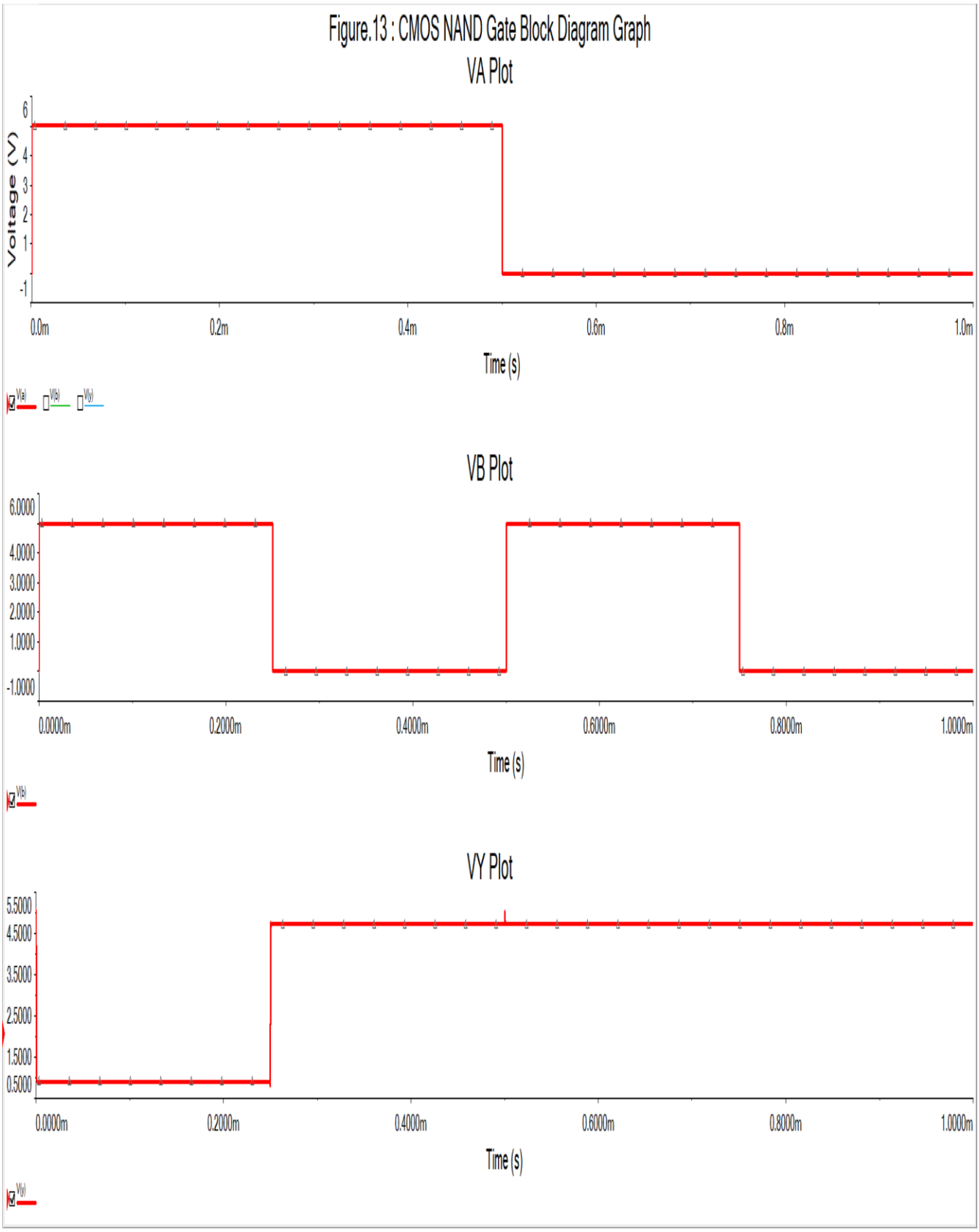
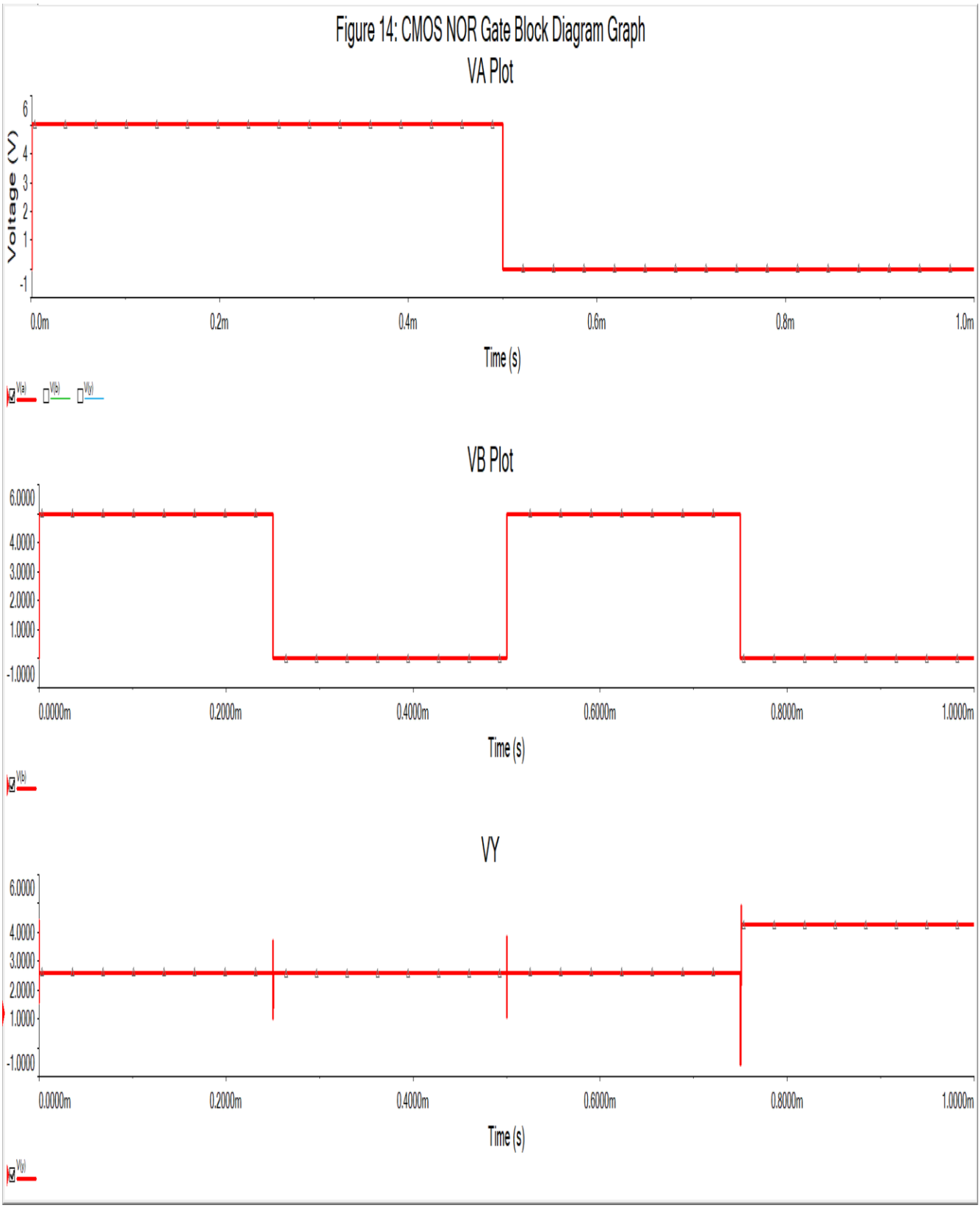


Figure 14: CMOS NOR Gate Block Diagram Graph



Truth Table:

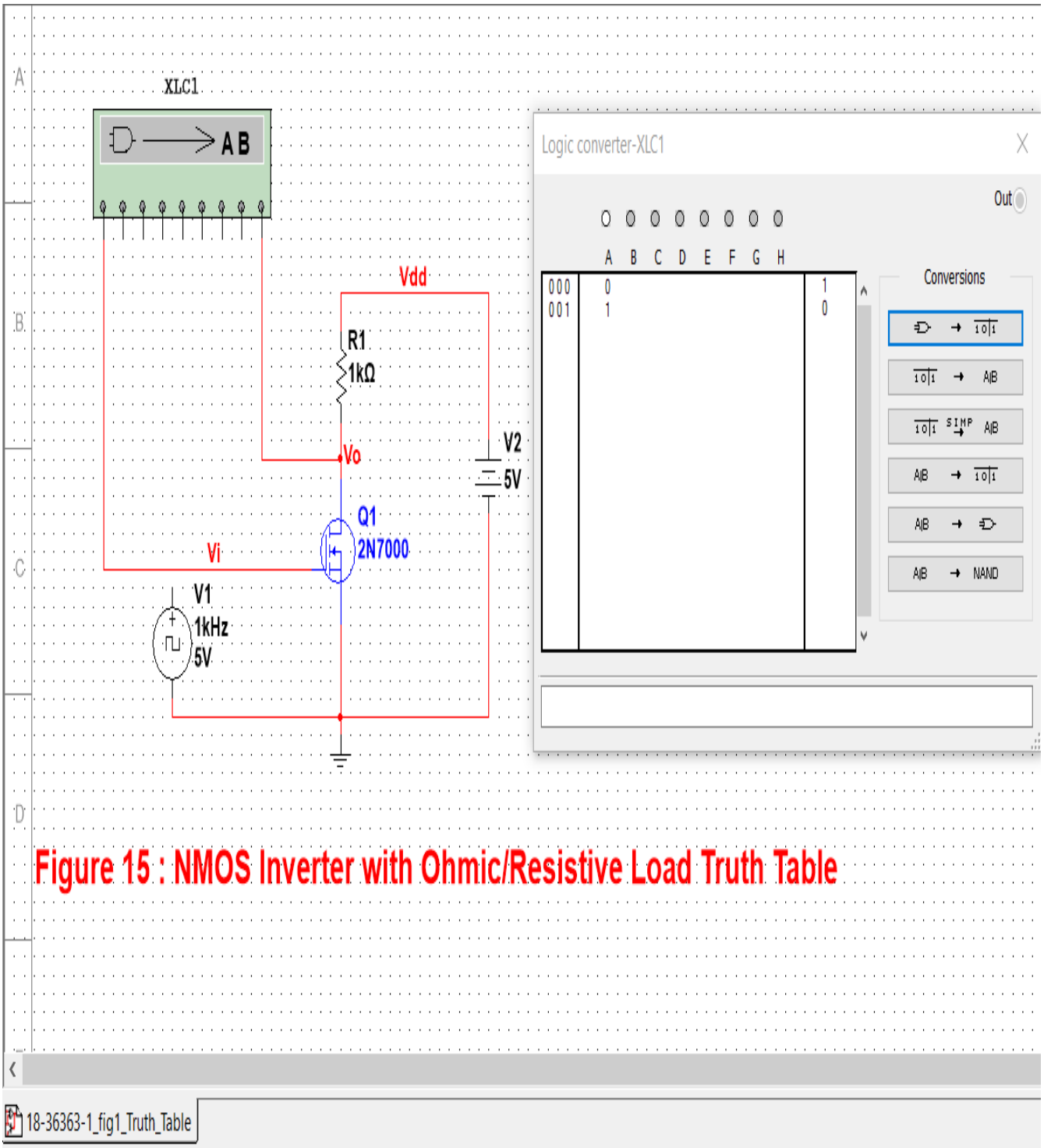


Figure 15 : NMOS Inverter with Ohmic/Resistive Load Truth Table

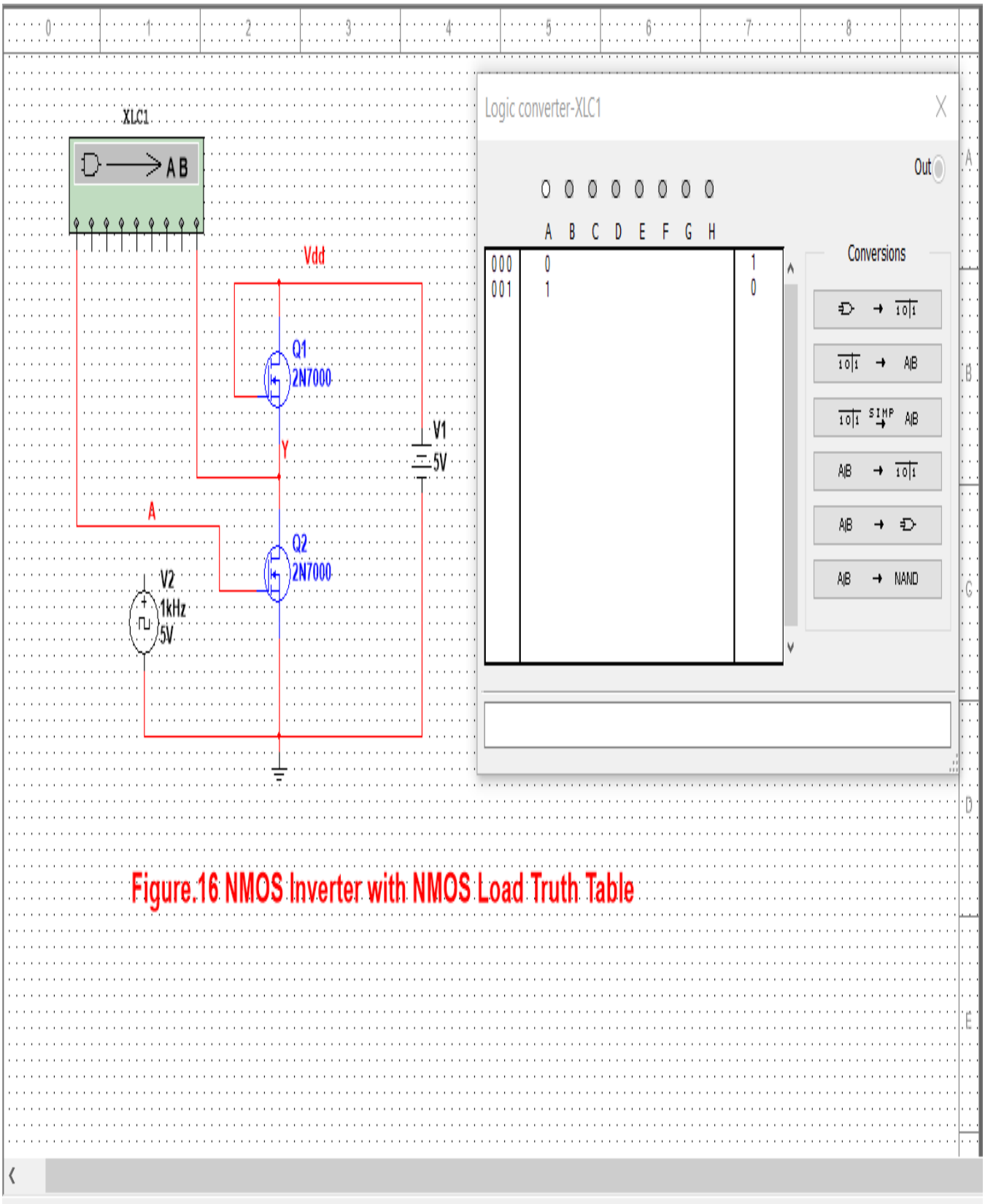


Figure.16 NMOS Inverter with NMOS Load Truth Table

18-36363-1_fig2_Truth_Table

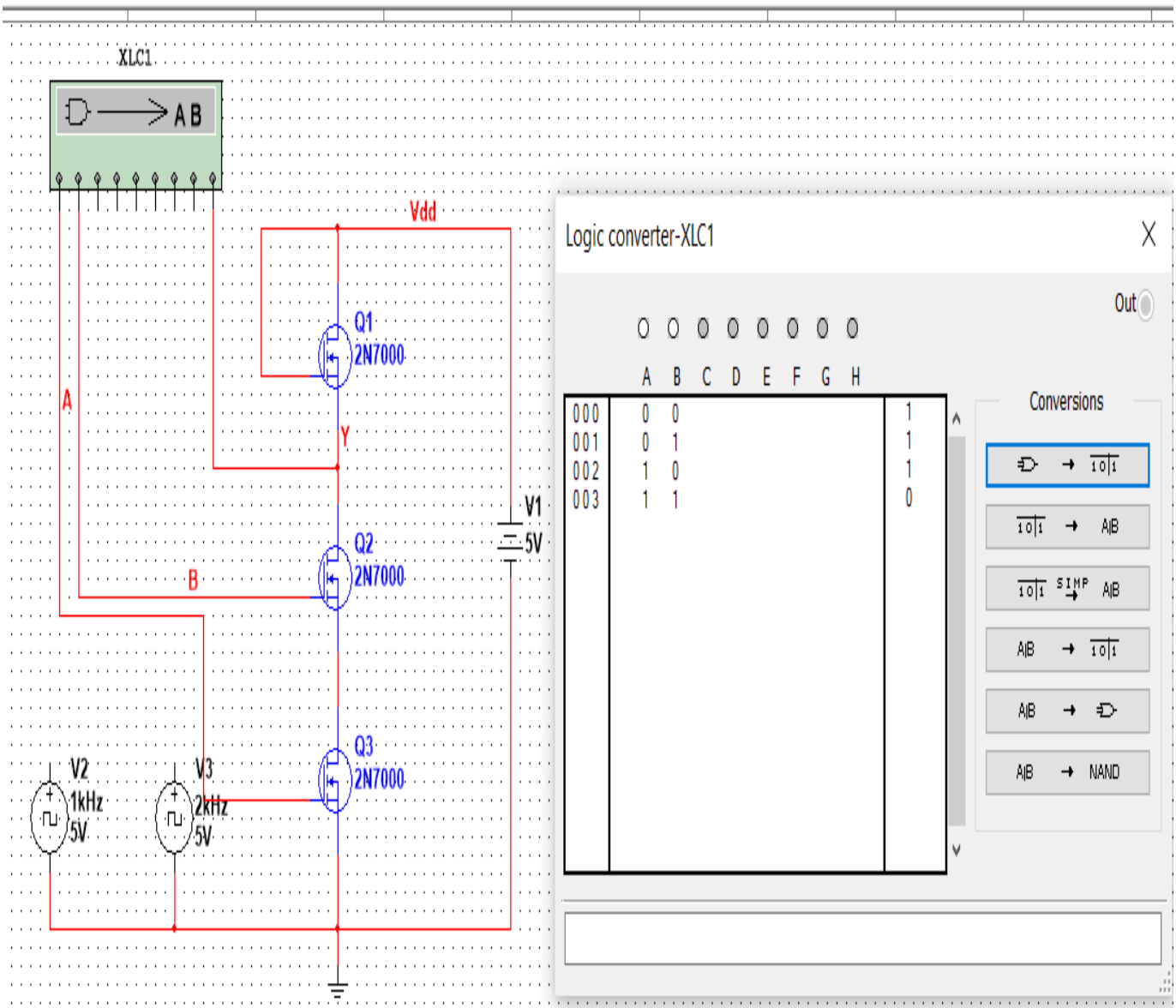


Figure.17 NMOS NAND Gate Truth Table

18-36363-1_fig3_Truth_Table *

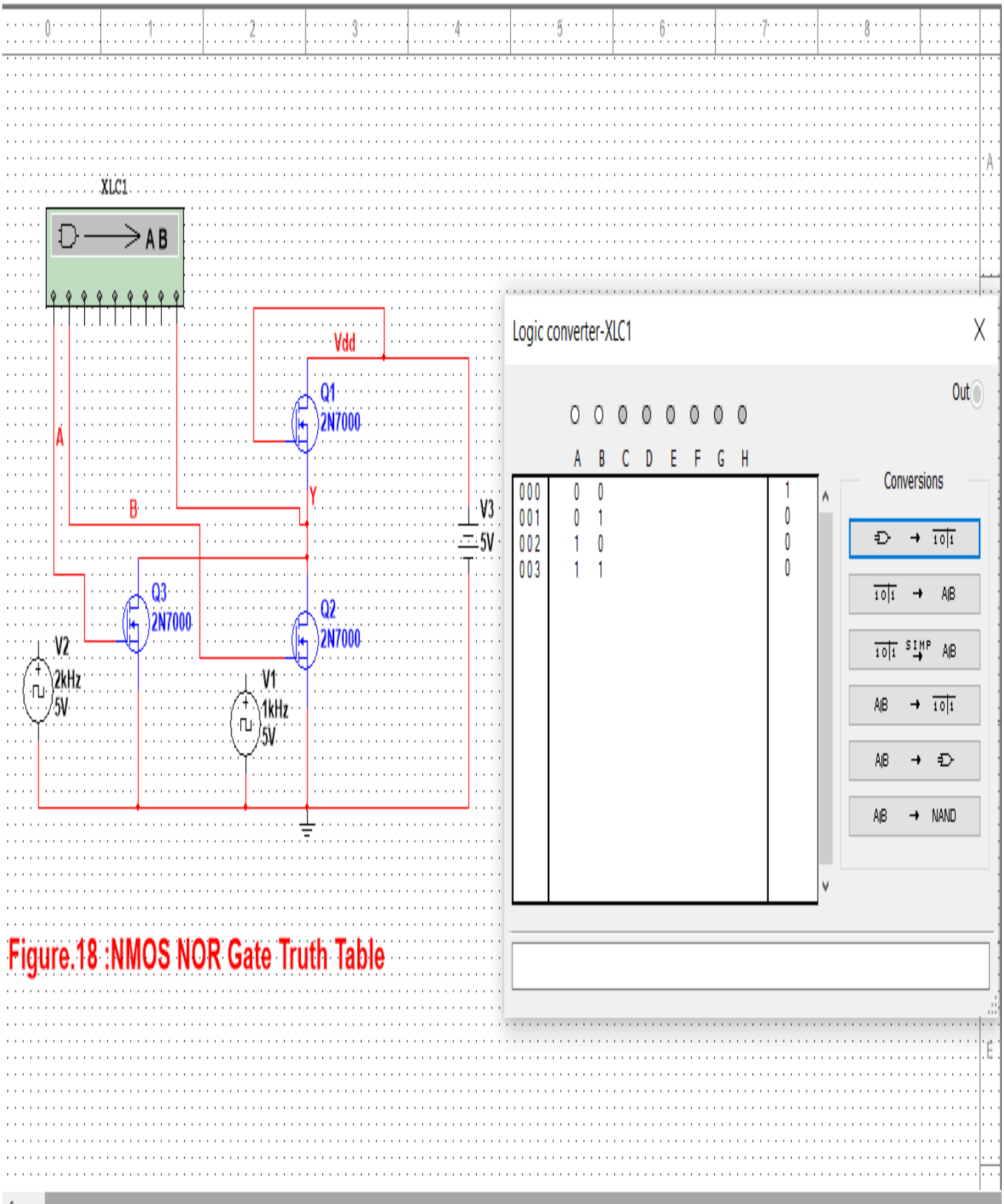


Figure.18 :NMOS NOR Gate Truth Table

18-36363-1_fig4_Truth_Table *

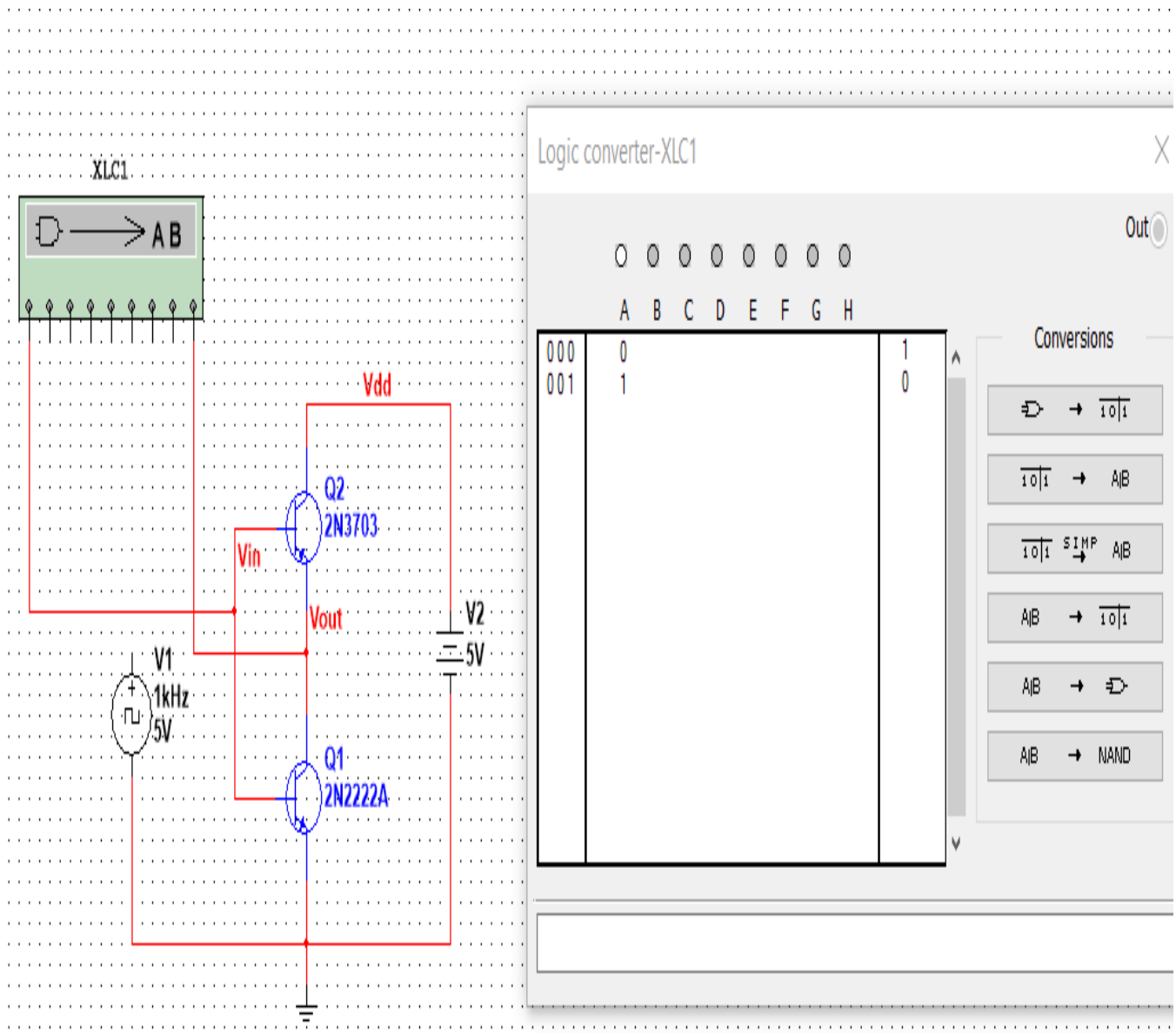


Figure 19 : CMOS Inverter Truth Table

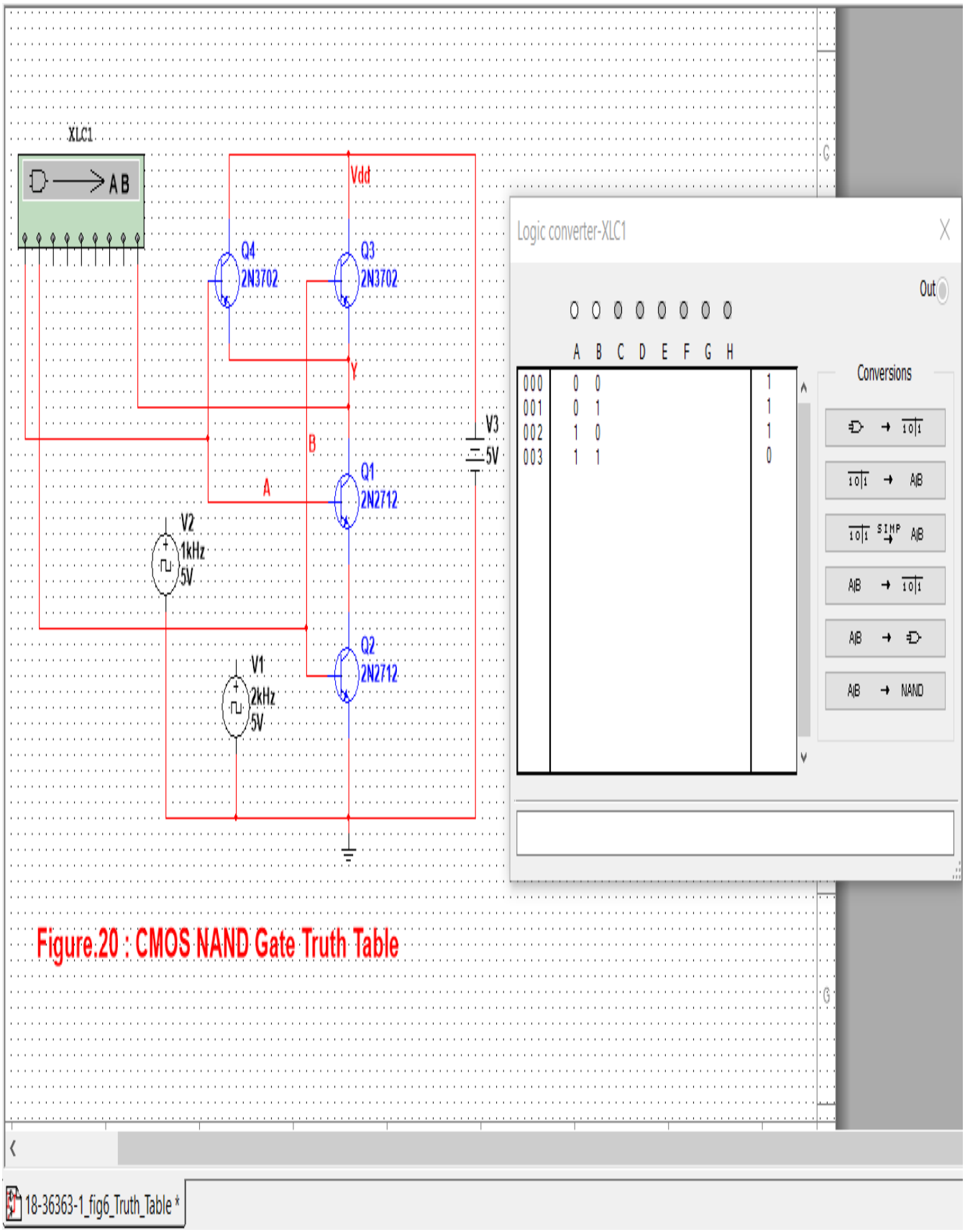


Figure.20 : CMOS NAND Gate Truth Table

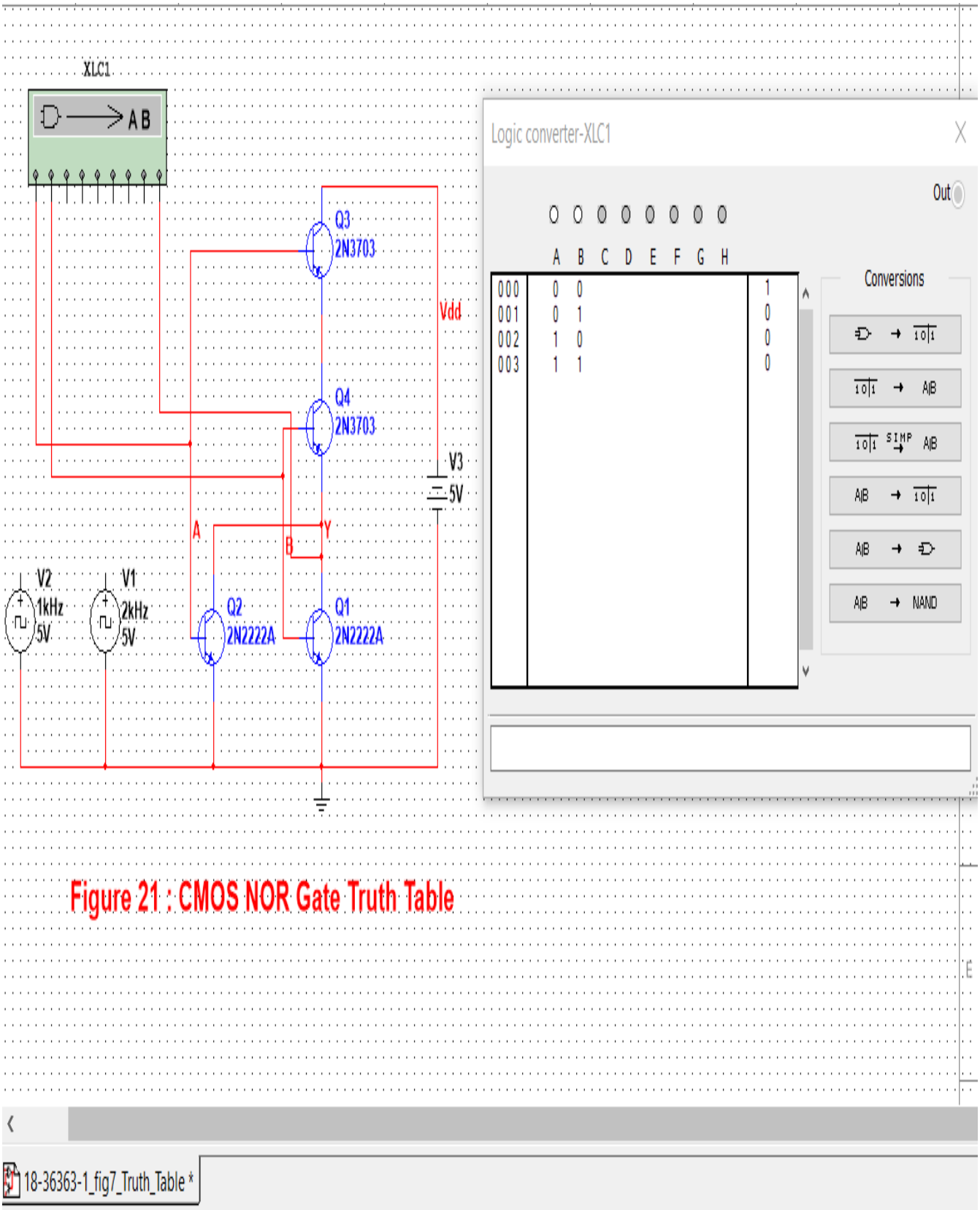


Figure 21 : CMOS NOR Gate Truth Table