American International University- Bangladesh
Department of Electrical and Electronic Engineering
EEE2206 Digital Logic Design Laboratory

Title: Implementation of shift registers using flip-flops.

Introduction:

A flip-flop stores one bit of information. When a set of n-flip-flops is used to store n-bits of information, such as an n-bit number, we refer to these flip-flops as a register. A common clock is used for each flip-flop in a register, and each flip-flop operates as described in the previous sections. The term register is merely a convenience for referring ton-bit structures consisting of flip-flops.
The objective of this experiment is designing of the following Shift Registers using J-K Flip-Flops (IC 74LS76)

1. Serial In/ Serial Out (SISO) Shift Register
2. Serial In / Parallel Out (SIPO) Shift Register
3. Parallel In / Serial Out (PISO) Shift Register
4. Parallel In / Parallel Out (PIPO) Shift Register
5. Bidirectional Shift Registers

Theory and Methodology:

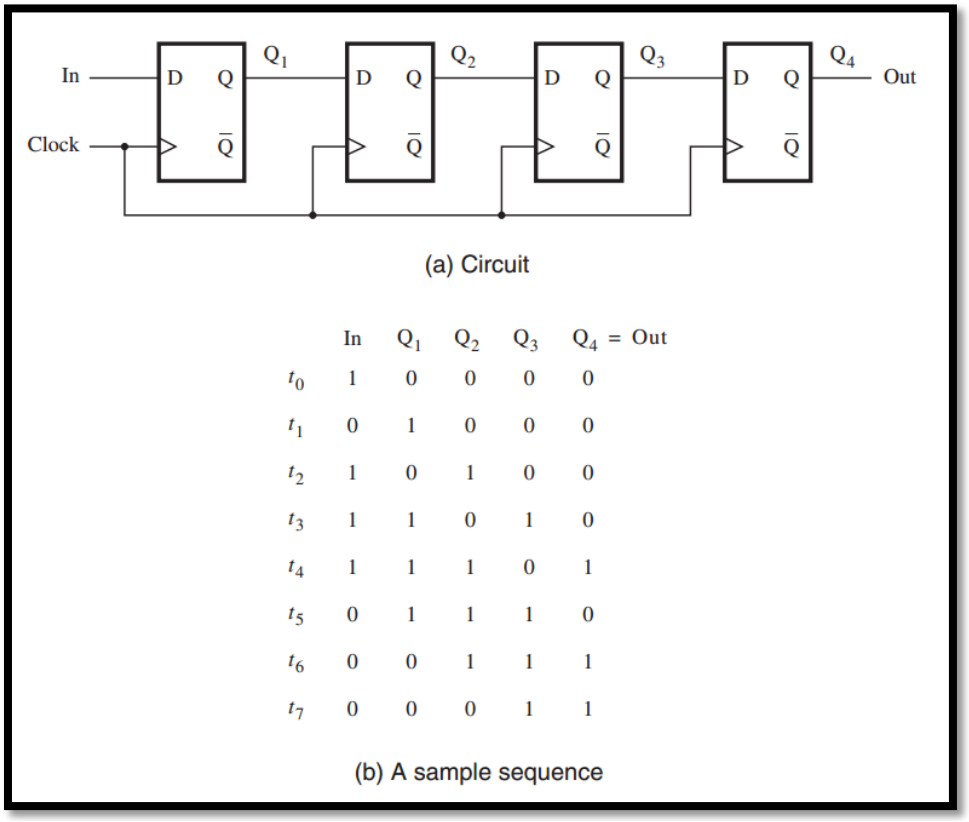
Shift Registers

In digital circuits, a **shift register** is a cascade of flip flops, sharing the same clock, in which the output of each flip-flop is connected to the "data" input of the next flip-flop in the chain, resulting in a circuit that shifts by one position the "bit array" stored in it, *shifting in* the data present at its input and *shifting out* the last bit in the array, at each transition of the clock input. More generally, a **shift register** may be multidimensional, such that its "data in" and stage outputs are themselves bit arrays: this is implemented simply by running several shift registers of the same bit-length in parallel.

Shift registers can have both parallel and serial inputs and outputs. These are often configured as **serial-in, parallel-out** (SIPO) or as **parallel-in, serial-out** (PISO). There are also types that have both serial and parallel input and types with serial and parallel output. There are also **bi-directional** shift registers which allow shifting in both directions: L→R or R→L. The serial input and last output of a shift register can also be connected to create a **circular shift register**. The operations of these different types of shift registers are explained below.

Serial In/ Serial Out (SISO) Shift Register

Figure 10.1(a) shows a four-bit shift register that is used to shift its contents one bit-position to the right. The data bits are loaded into the shift register in a serial fashion using the In input. The contents of each flip-flop are transferred to the next flip-flop at each positive edge of the clock. An illustration of the transfer is given in Figure 10.1(b), which shows what happens when the signal values at *In* during eight consecutive clock cycles are 1, 0, 1, 1, 1, 0, 0, and 0, assuming that the initial state of all flip-flops is 0.



(a) Circuit

	In	Q_1	Q_2	Q_3	Q_4 = Out
t_0	1	0	0	0	0
t_1	0	1	0	0	0
t_2	1	0	1	0	0
t_3	1	1	0	1	0
t_4	1	1	1	0	1
t_5	0	1	1	1	0
t_6	0	0	1	1	1
t_7	0	0	0	1	1

(b) A sample sequence

Figure 10.1: Serial In/ Serial Out (SISO) Shift Register

Serial In / Parallel Out (SIPO) Shift Register

In this type of Shift register, data bits are entered serially in the same manner as discussed in SISO but the output is taken from each stage as show in the diagram below.

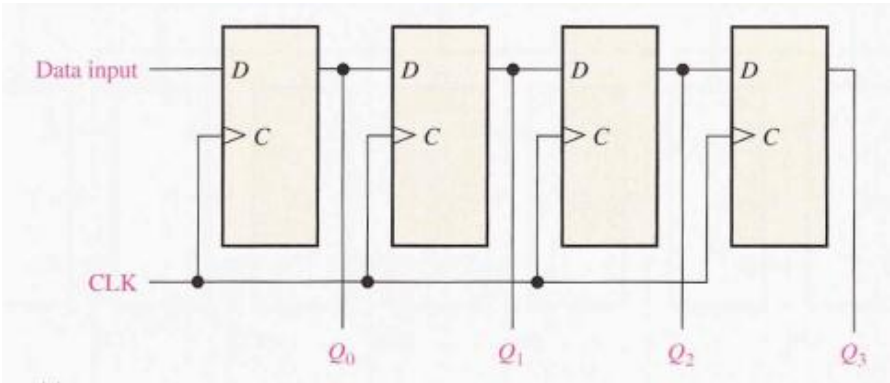


Figure 10.2(a): Serial In / Parallel Out (SIPO) Shift Register

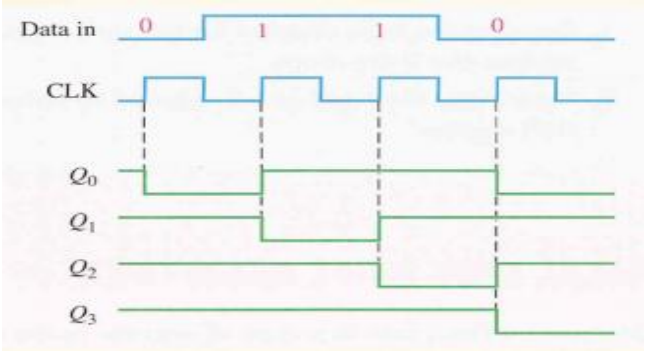


Figure 10.2(b): Timing Diagram of Serial In / Parallel Out (SIPO) Shift Register

Parallel In / Parallel Out (PIPO) Shift Register

In this type of shift register, data bits are entered simultaneously in all the flip-flops and the bits appear on the parallel outputs as shown in the figure below.

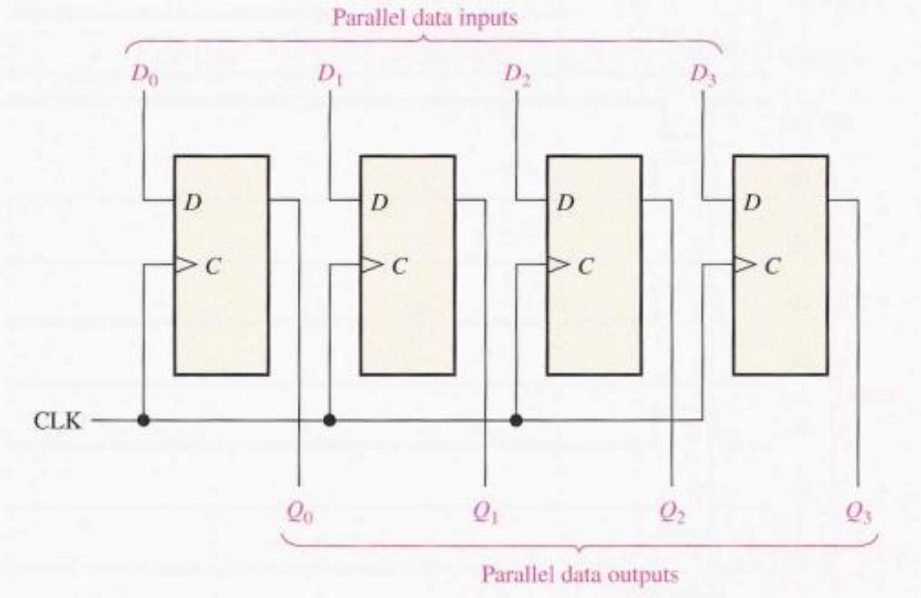


Figure 10.3: Parallel In / Parallel Out Shift Register

Parallel In / Serial Out (PISO) Shift Register

In computer systems it is often necessary to transfer n-bit data items. Transmitting all bits at once using n separate wires, in which case we say that the transfer is performed in parallel, may do this. But it is also possible to transfer all bits using a single wire, by performing the transfer one bit at a time, in n consecutive clock cycles. We refer to this scheme as serial transfer. To transfer an n-bit data item serially, we can use a shift register that can be loaded with all n bits in parallel (in one clock cycle). Then during the next n clock cycles, the contents of the register can be shifted out for serial transfer. The reverse operation is also needed. If bits are received serially, then after n clock cycles the contents of the register can be accessed in parallel as an n-bit item.

Figure 10.4 shows a four-bit shift register that allows the parallel access. Instead of using the normal shift register connection; the D input of each flip-flop is connected to two different sources. One source is the preceding flip-flop, which is needed for the shift-register operation. The other source is the external input that corresponds to the bit that is to be loaded into the flip-flop as a part of the parallel-load operation. The control signal Shift/Load is used to select the mode of operation. If Shift/Load=0, then the circuit operates as a shift register. If Shift/Load=1, then the parallel input data are loaded into the register. In both cases the action takes place on the positive edge of the clock.

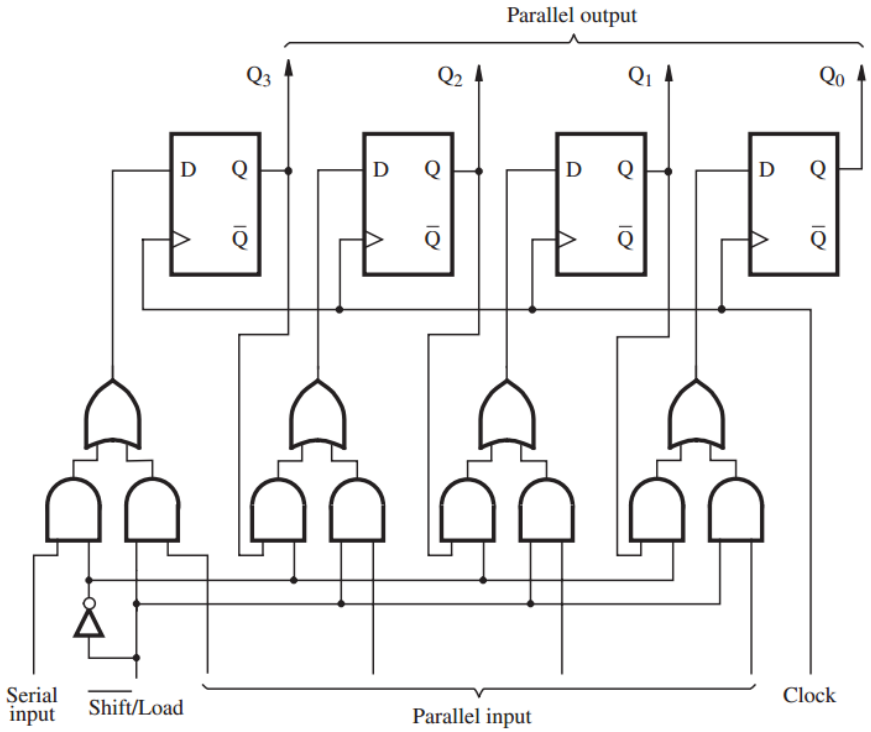


Figure 10.4: Parallel In / Serial Out (PISO) Shift Register

Bidirectional Shift Registers

A bidirectional shift register is one in which the data can be shifted either left or right as shown in Figure 10.5(a). A High on the $RIGHT/\overline{LEFT}$ control input allows data bits inside the register to be shifted to the right and a Low enables data bits inside the register to be shifted to the left. When the $RIGHT/\overline{LEFT}$ control input is HIGH, gates G1 through G4 are enabled and the state of the Q output of each flip-flop is passed through to the D input of the ***following*** flip flop. When a clock pulse occurs, the data bits are shifted one place to the *right*. When the $RIGHT/\overline{LEFT}$ control input is LOW, gates G5 through G8 are enabled and the state of the Q output of each flip-flop is passed through to the D input of the ***preceding*** flip flop. When a clock pulse occurs, the data bits are shifted one place to the *left*.

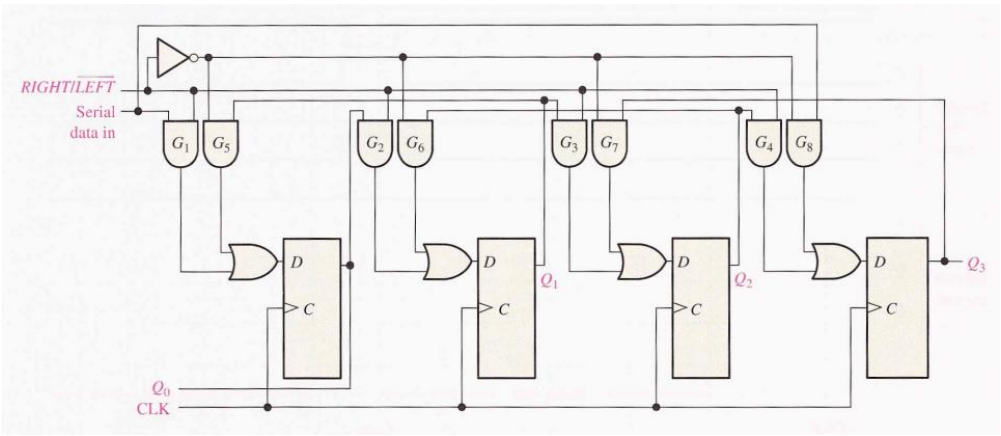


Figure 10.5(a): Bidirectional Shift Registers

Pin Configuration of 74LS76

There are 2 J-K Flip Flops in one IC. Here is the pin configuration of the IC 74LS76:

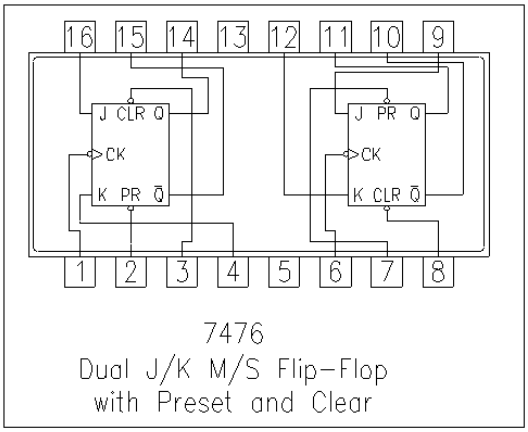


Figure 10.6(a): IC 74LS76

Pin Configuration of 7432 and 7408

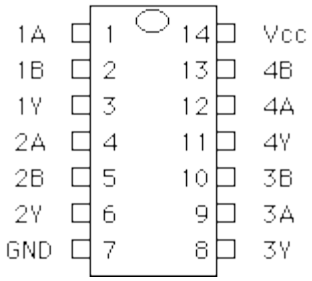


Figure 10.6(b): IC 7432(OR Gate)

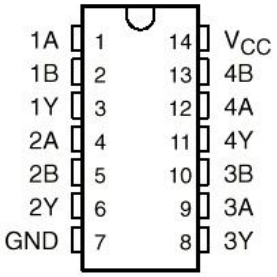


Figure 10.6(c): IC 7408(AND Gate)

Pre-Lab Homework:

- Write down in details the operation of **D Flip Flops** mentioning its circuit diagram, truth table and timing diagram (also mention about the asynchronous inputs).

Apparatus:

- IC 74LS76 (JK Flip Flop)
- IC 7408 and 7432
- LED Lamps or Display
- Trainer Board
- Oscilloscope
- Connecting Wires

Precautions:

- Before preparing the circuits, check all the ICs(74LS76 & 7408 & 7432) to make sure they are all working properly.
- Careful about the biasing of JK Flip Flops.
- Make sure you connected the preset and clear pins with Vcc.
- Try to use as less wire as possible. Make sure there is no loose connection.

- For Clock pulse, the trainer board's analog signal generator is a good choice. Use lower frequencies so that the change is slow enough to observe the outputs and take readings.

Experimental Procedure:

1. Design all the five types of shift registers that is explained above.
2. Setup the circuits as shown in the above figures.
3. Take different input data bits.
4. Record your data in a truth table or draw a timing diagram where applicable.

Simulation and Measurement:

Compare the simulation results with your experimental data/ wave shapes and comment on the differences (if any).

Discussion and conclusion:

1. Prepare all the truth table and draw the output wave shapes of all the shift registers that you have designed in the lab.
2. Attach some clear pictures of the results you found in the lab.

Reference(s):

i) Thomas L. Floyd, "Digital Fundamentals", Ninth Edition.

Teaching Tips

- Check all the ICs before setting up the main circuit.
- Check the outputs of each stage before going to the next one.
- The experiment is very lengthy so explain the operations of all the shift registers but either implement any 3 or 4, preferably SISO, PISO and Bidirectional, or tell different groups to implement the different ones.
- Use different input signals for data inputs.