Experiment No : 2 : Construction of Bipolar Transistor Logic Gate.

Introduction: A bipolar transistor is a three terminal semiconductor device. Under the control of one of the terminals, called the base, current can flow selectively from the collector terminal of the emitter terminal.

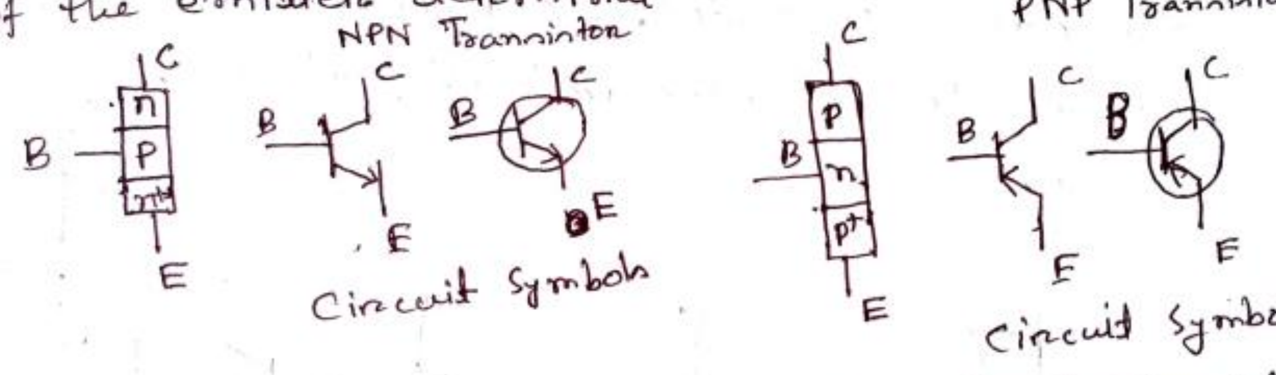


Fig 2.1: Bipolar junction transistor circuit symbols.

In this experiment we examine how to build logic gates from bipolar transistor using the RTL, DTL and TTL deg design.

Theory and Methodology: Register-Transistor Logic (RTL): Register Transistor Logic (RTL) is a large step beyond Diode Logic (DL). Basically, RTL replaces the diode switch with a transistor switch. If a +5V signal (logic 1) is applied to the base of the transistor, the transistor turns fully on and grounds the output signal.

If the input is grounded, the transistor is off and the output signal is allowed to rise to +5 volts. In this way, the transistor not only inverts the logic sense of the signal, but it also ensures that the output voltage will always be a valid logic level under all circumstances. Because of this, RTL circuits can be cascaded indefinitely, where DL circuits can not be cascaded reliably at all.

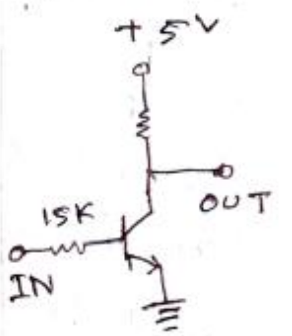


Fig. 2.2: RTL Inverter

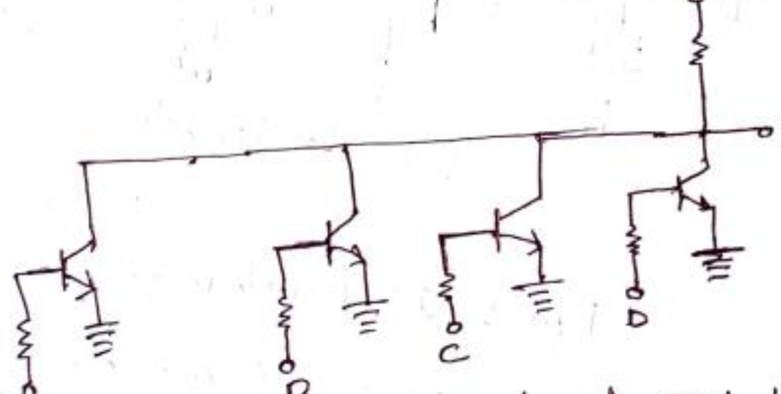


Fig 2.3: 4-input RTL inverter

Diode-Transistor Logic (DTL): Diode transistor Logic (DTL) is a class of digital circuits built from bipolar junction transistors (BJT), diodes and resistors; it is the direct ancestor of transistor-transistor Logic (TTL).

DTL offers better noise margins and greater fan outs than RTL, but suffers from low speed.

RTL allows the construction of NOR gate easily, but NAND gates are relatively more difficult to get from RTL. DTL, however, allows the construction of simple NAND gates from a single transistor, with the help of several diodes and resistors.

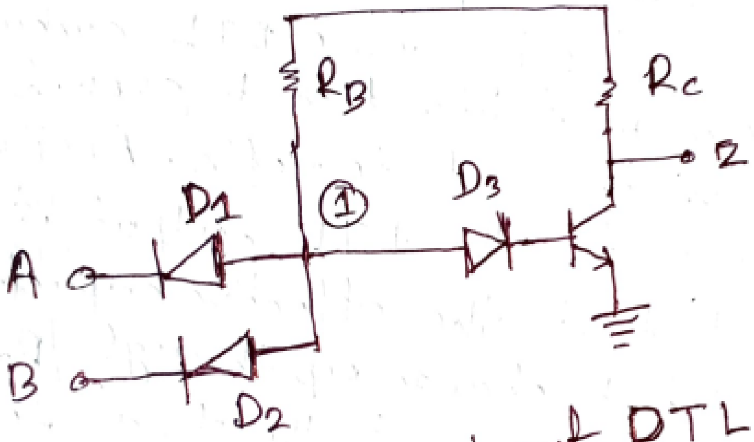


Fig 2.4: 2-input DTL NAND Gate.

<u>Transistor-Transistor Logic</u>: We can think of a bipolar transistor as two diodes placed very close together, with the point between the diodes being the transistor base. Thus, we can use transistors in place of diodes to obtain logic gates that can be implemented with transistors and resistors only: this is called transistor-transistor logic (TTL).

One problem that DTL doesnot solve its low speed, especially when the transistor is being turned off. Turning off a saturated transistor in a DTL gate requires it to first pass through the active region before going into cut-off. Cutt off, however, will not be reached until the stored charge in its base has been removed. The dissipation of the base charge takes time if there is no available path from the base to ground. This is why some DTL circuits have a base resistor that is tied to ground, but even this requires some trade-offs. Another problem with turning off the DTL output transistor is the fact that the effective capacitance of the output need to charge up through R_c before the output voltage rises to the final logic '1' level, which also consumes a relatively large amount of time. TTL, however, solves the speed problem of DTL elegantly.

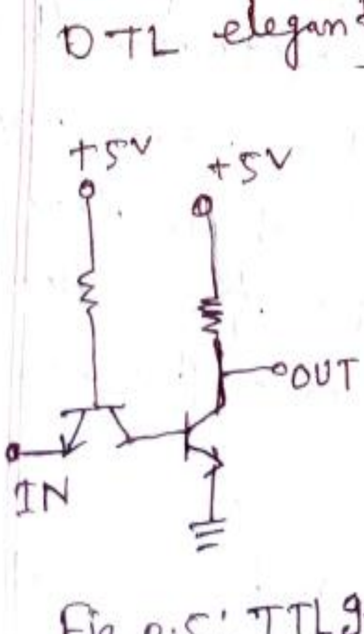


Fig 2.5: TTL Inverter

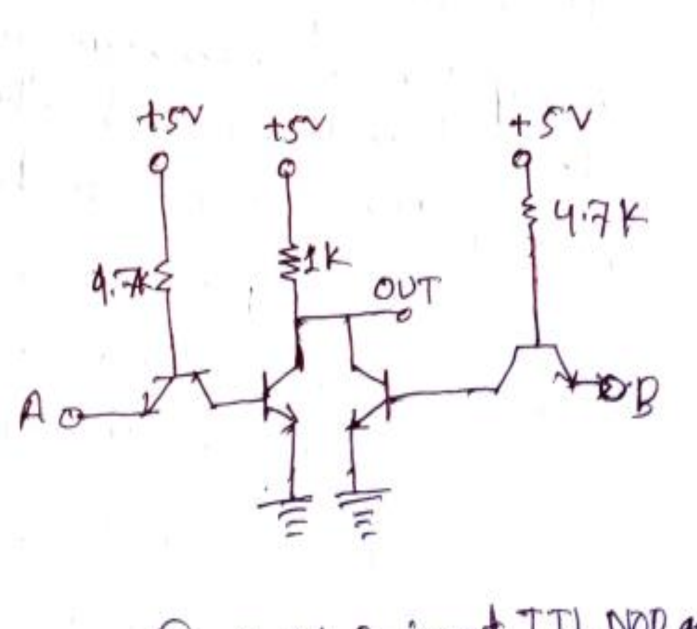


Fig 2.6: 2-input TTL NOR gate.

Block Diagrams:

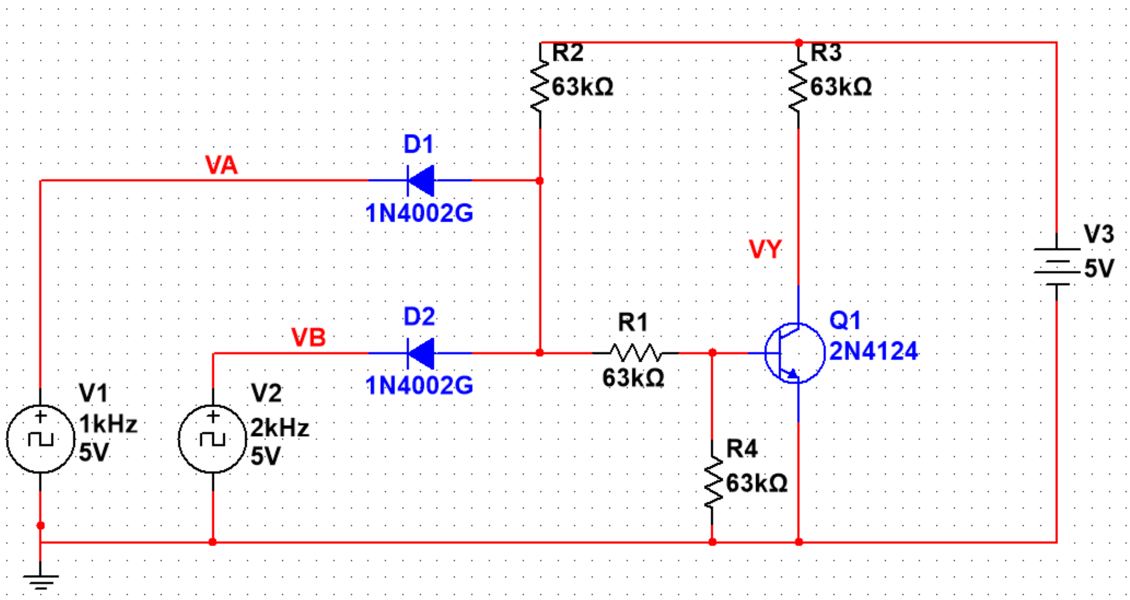


Fig 1: 2 Input DTL NAND Block Diagram.

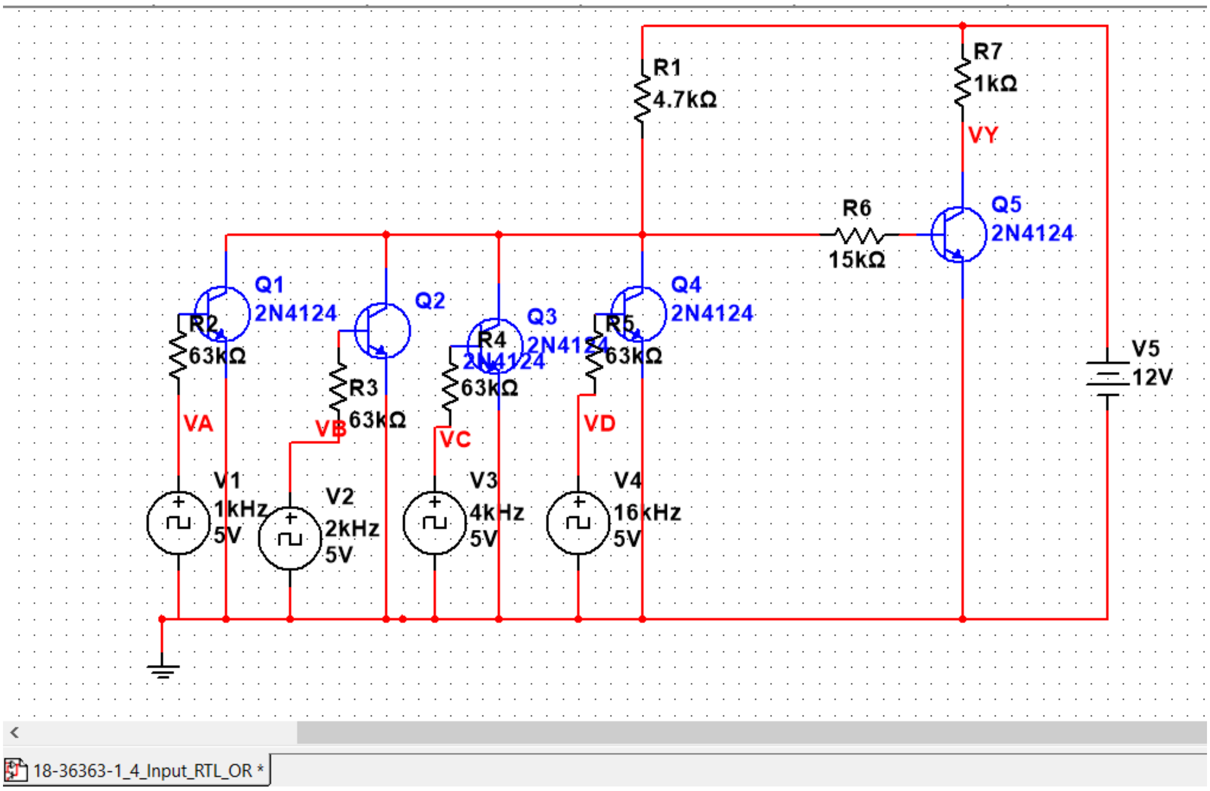


Fig 2: 4 Input RTL OR Block Diagram.

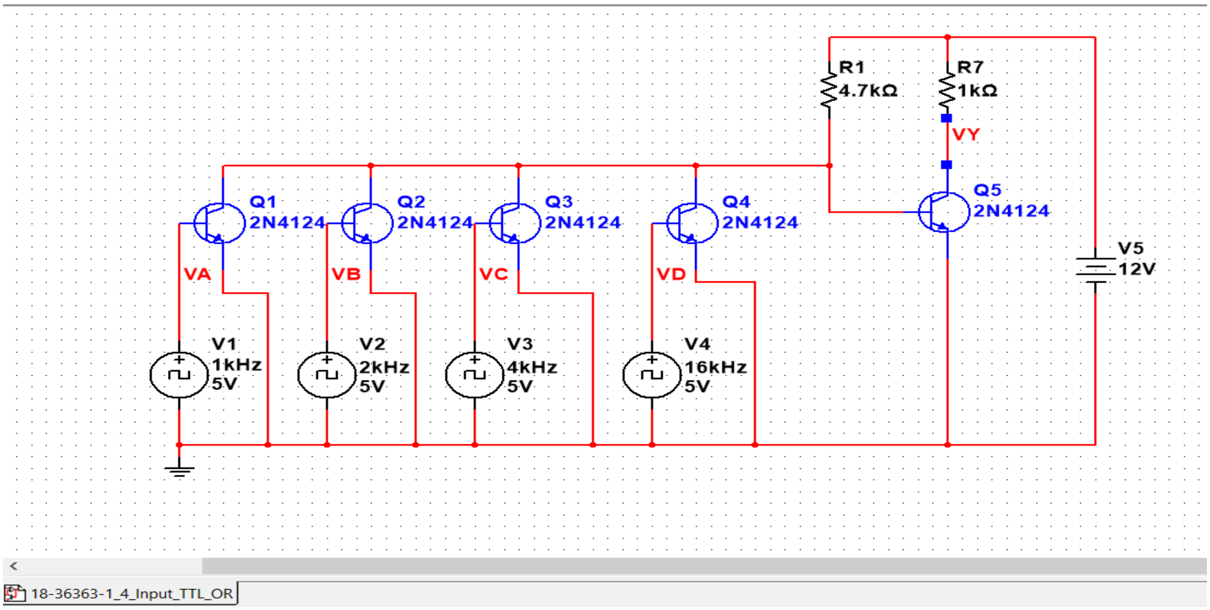


Fig 3: 4 Input TTL OR Block Diagram.

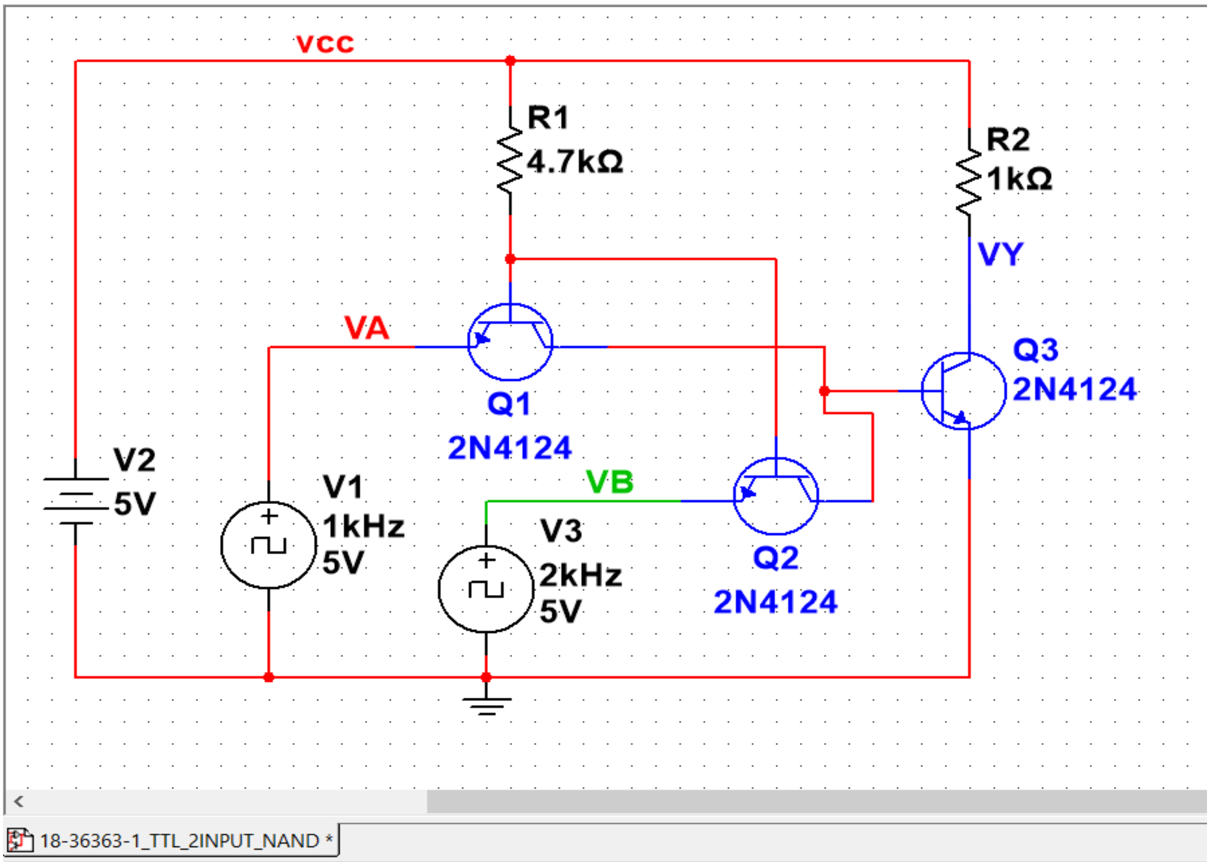


Fig 4: 2 Input TTL NAND Block Diagram.

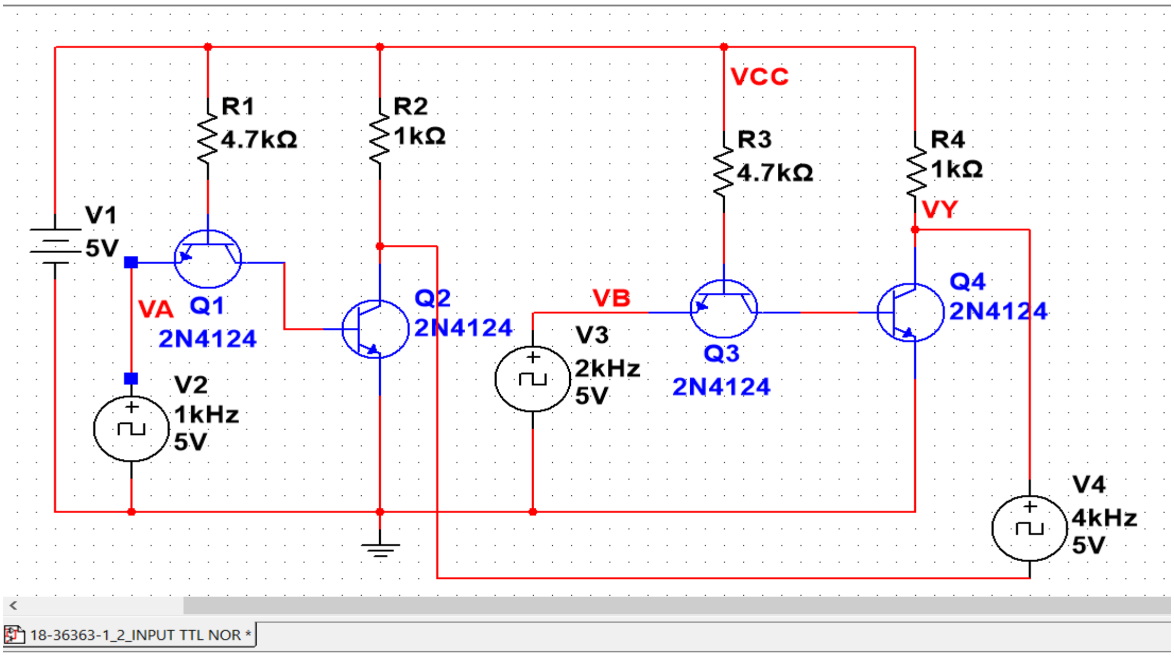


Fig 5: 2 Input TTL NOR Block Diagram.

Graphs:

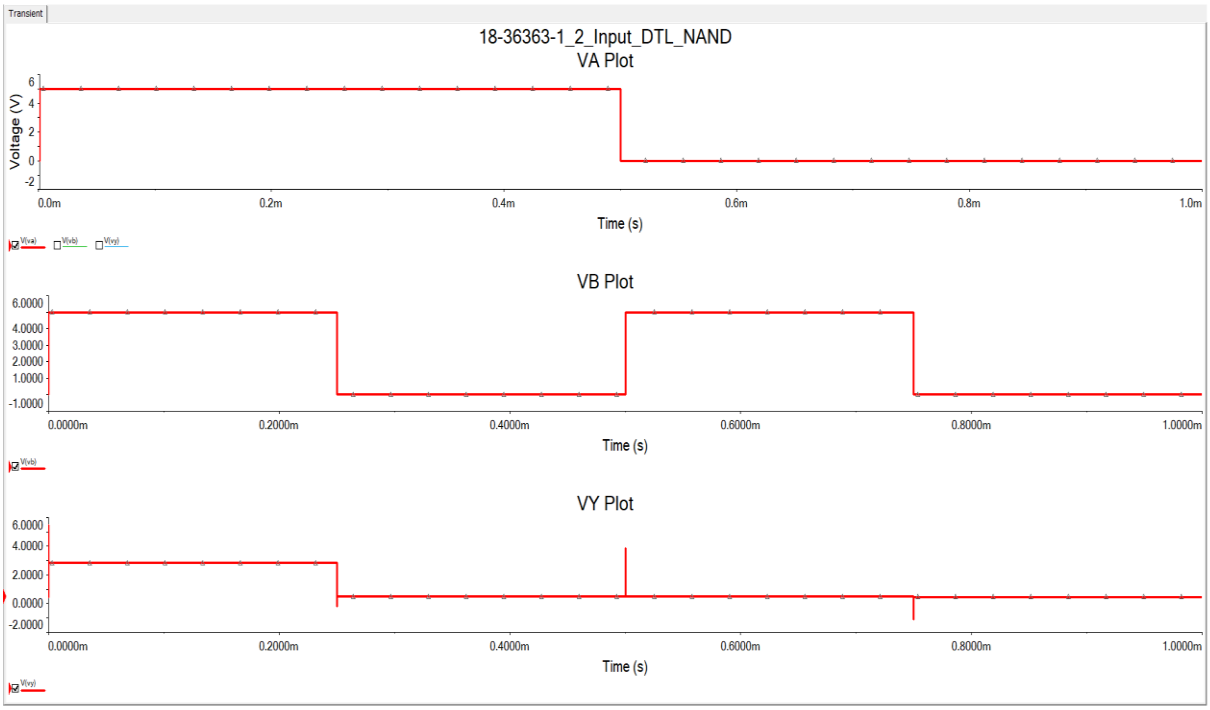


Fig 6: 2 Input DTL NAND Graph.

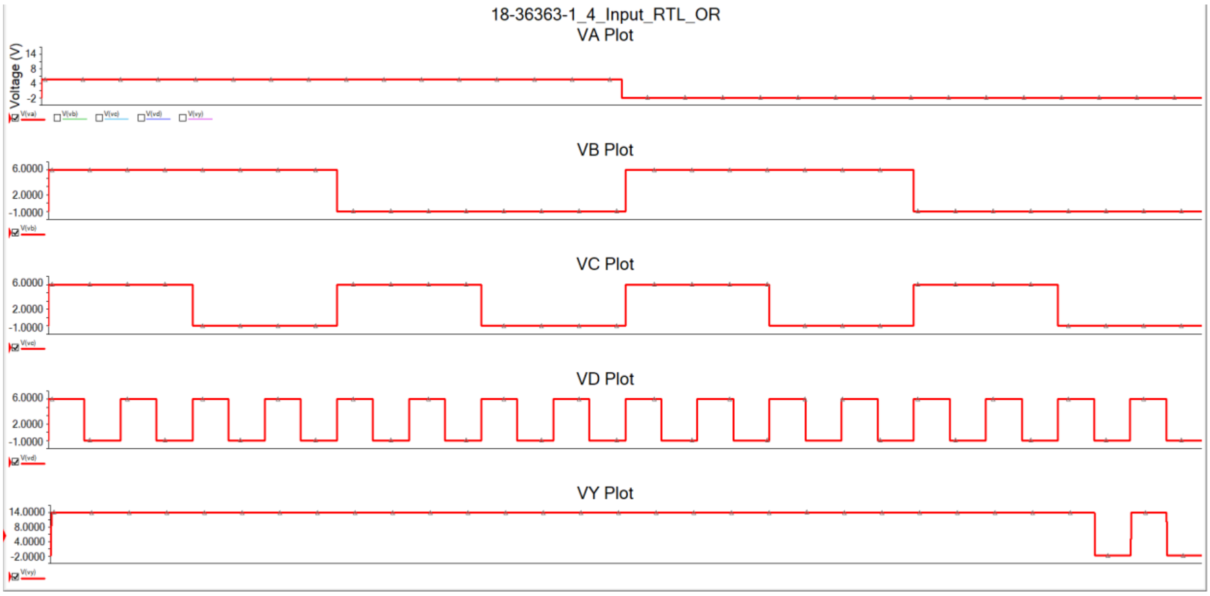


Fig 7: 4 Input RTL OR Graph.

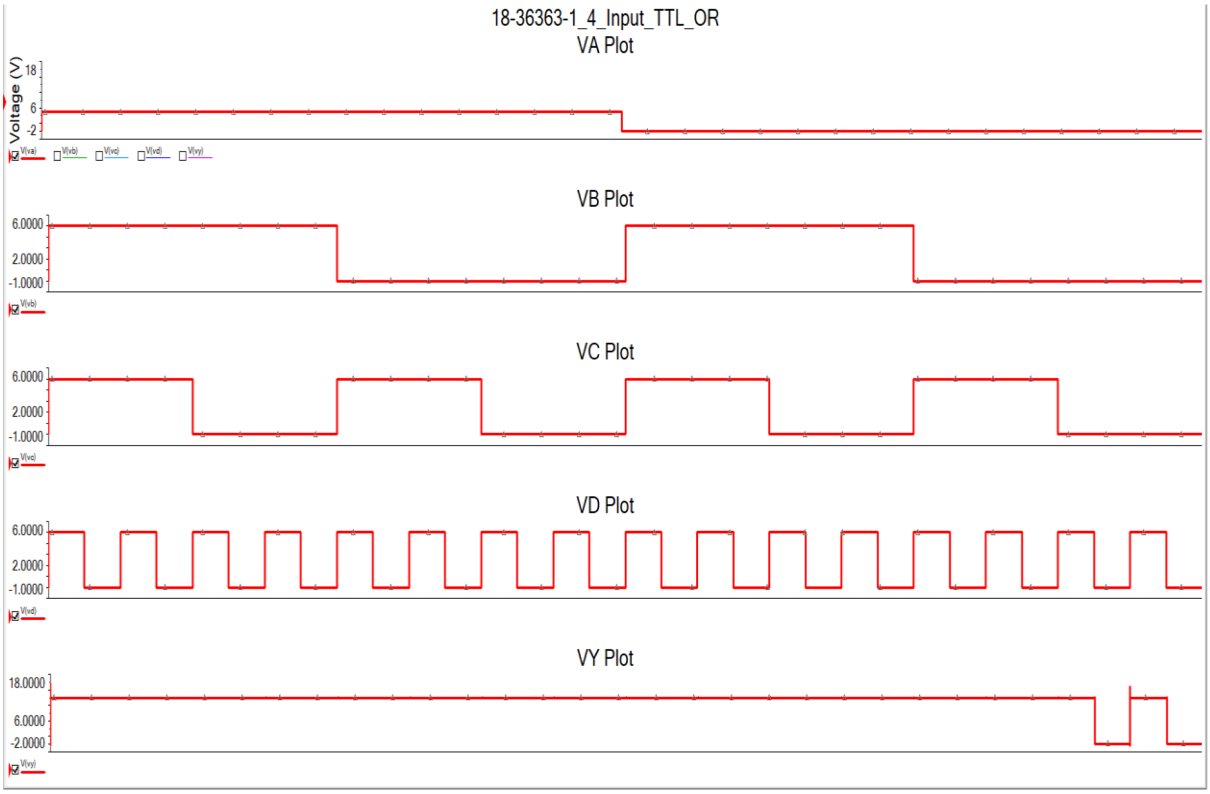


Fig 8: 4 Input TTL OR Graph.

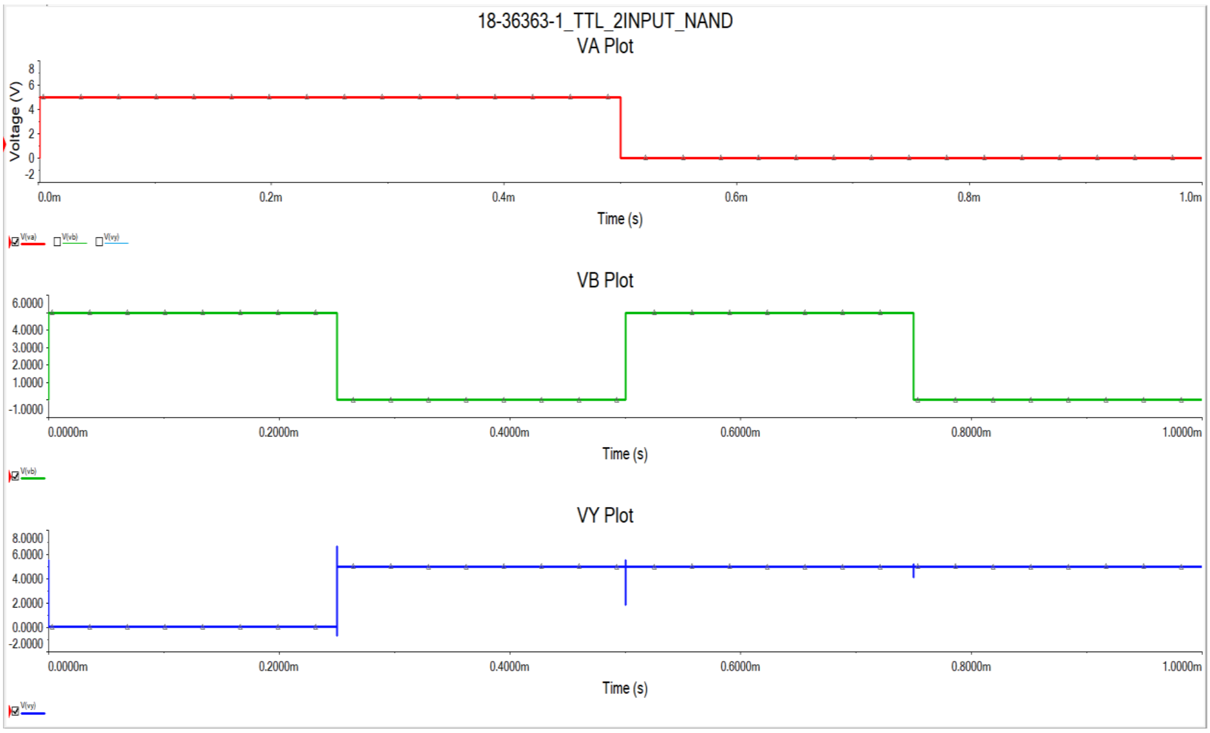


Fig 9: 2 Input TTL NAND Graph.

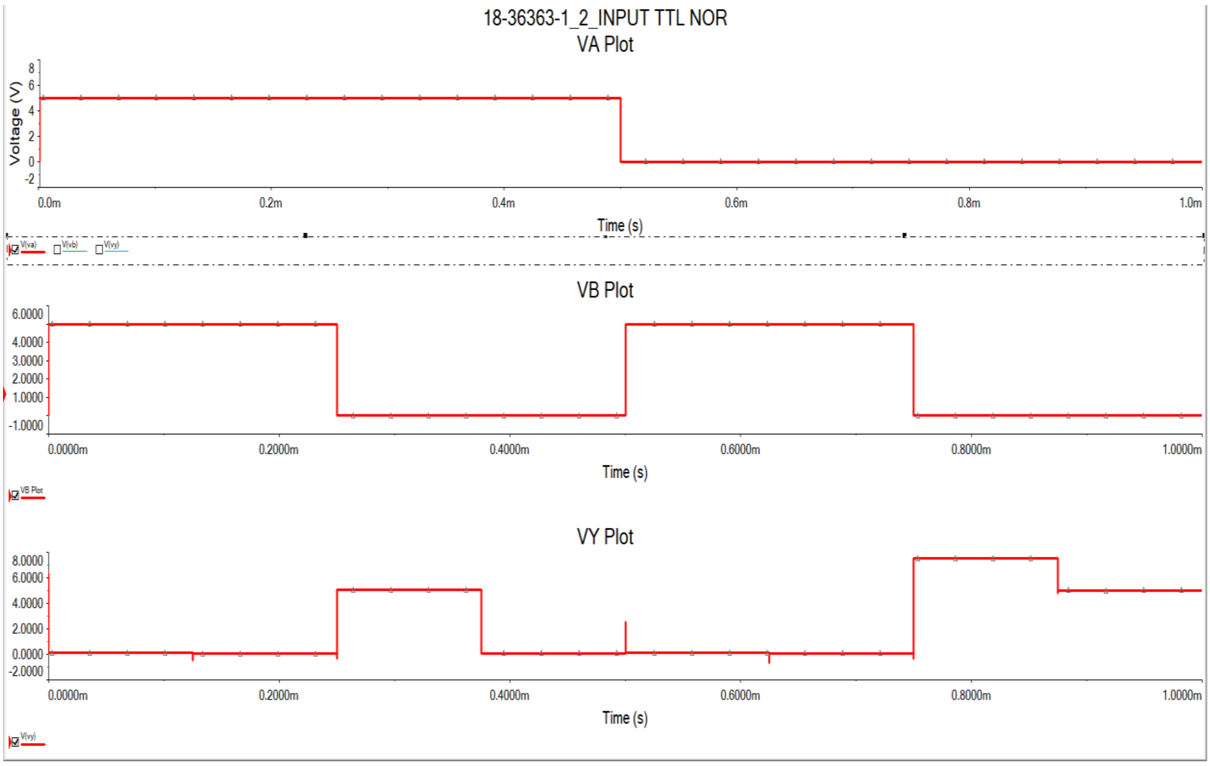


Fig 10: 2 Input TTL NOR Graph.

Truth Tables:

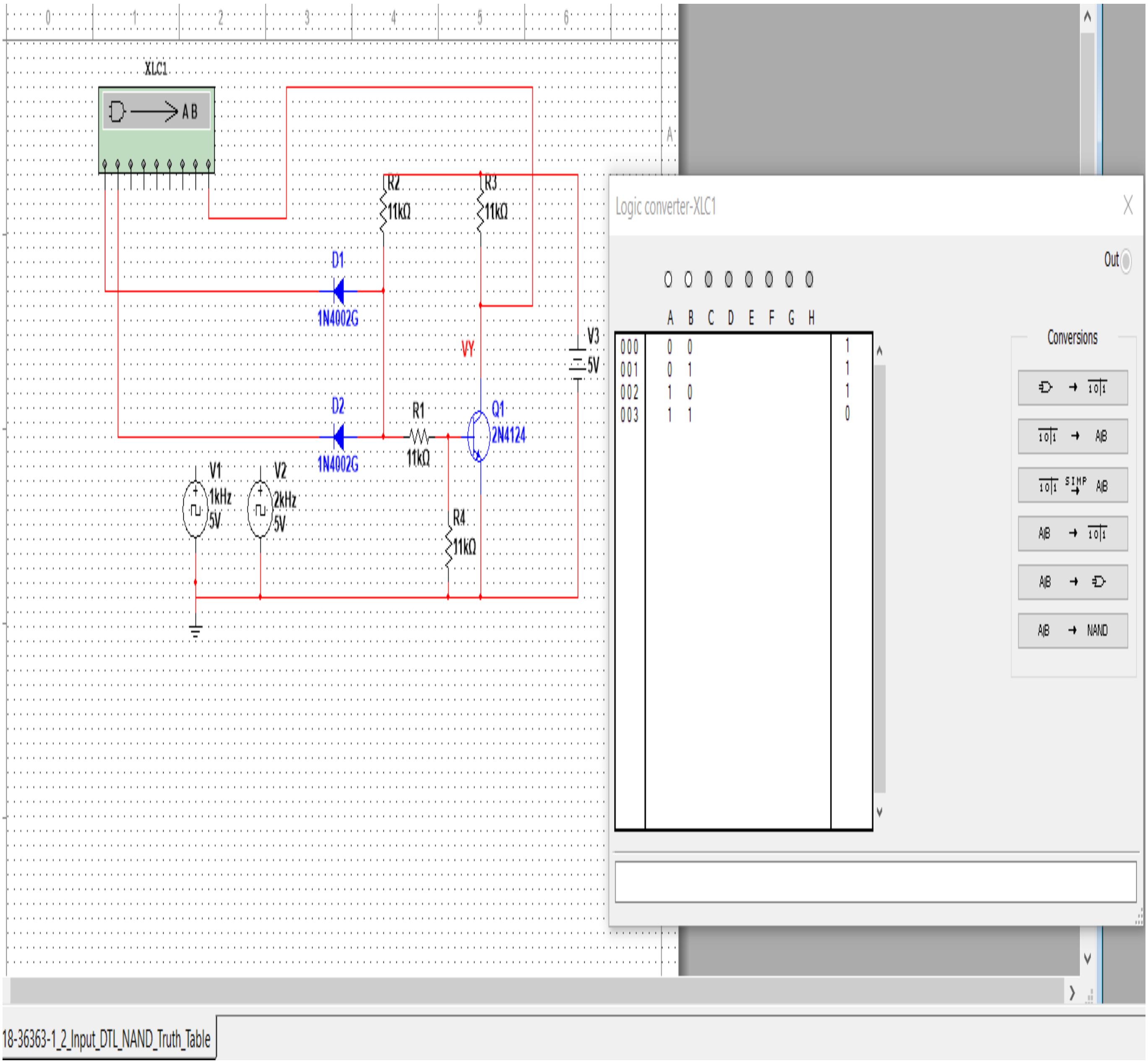
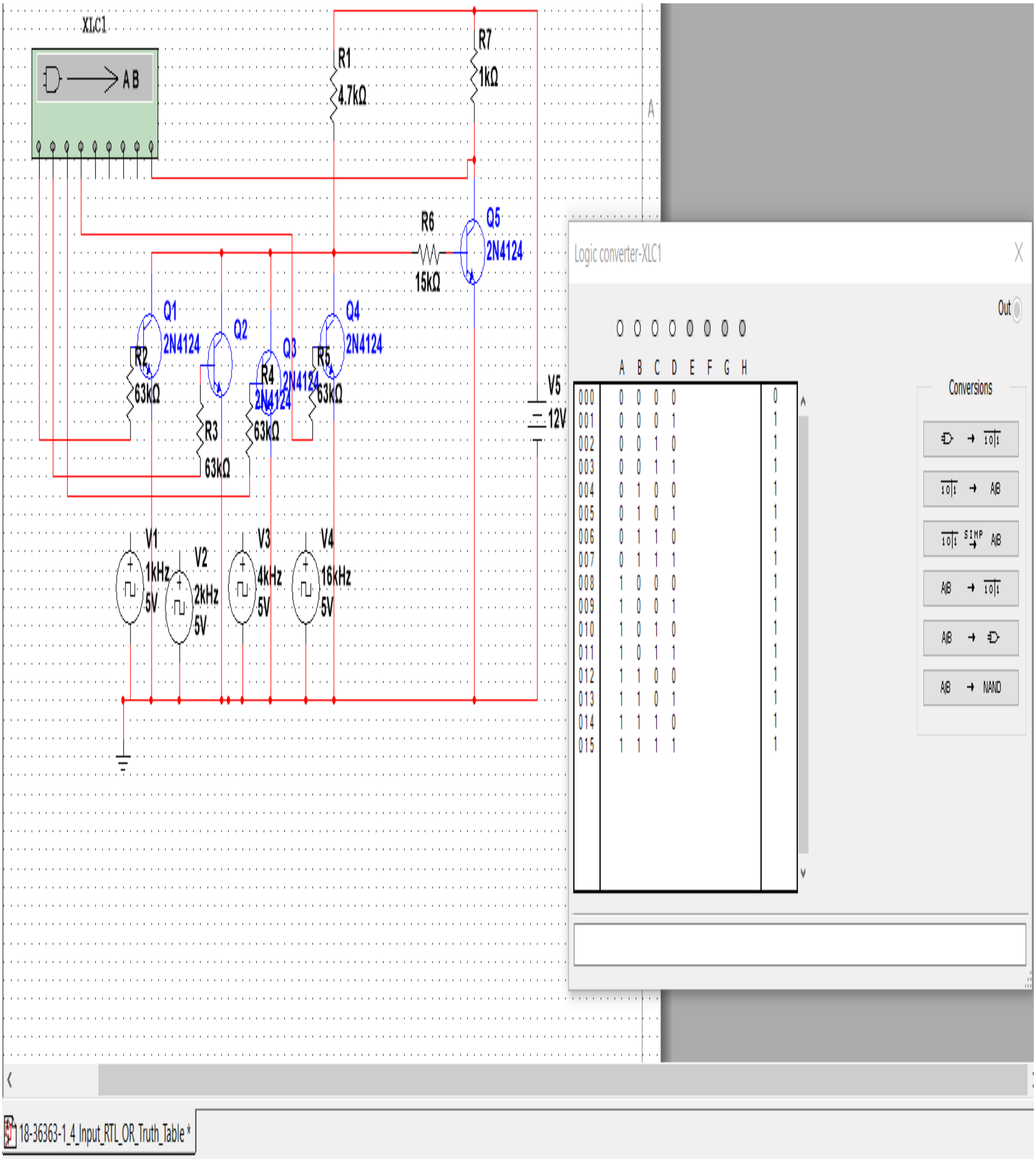


Fig 11: 2 Input DTL NAND Truth Table.



	A	B	C	D	Out
000	0	0	0	0	0
001	0	0	0	1	1
002	0	0	1	0	1
003	0	0	1	1	1
004	0	1	0	0	1
005	0	1	0	1	1
006	0	1	1	0	1
007	0	1	1	1	1
008	1	0	0	0	1
009	1	0	0	1	1
010	1	0	1	0	1
011	1	0	1	1	1
012	1	1	0	0	1
013	1	1	0	1	1
014	1	1	1	0	1
015	1	1	1	1	1

Fig 12: 2 Input RTL OR Truth Table.

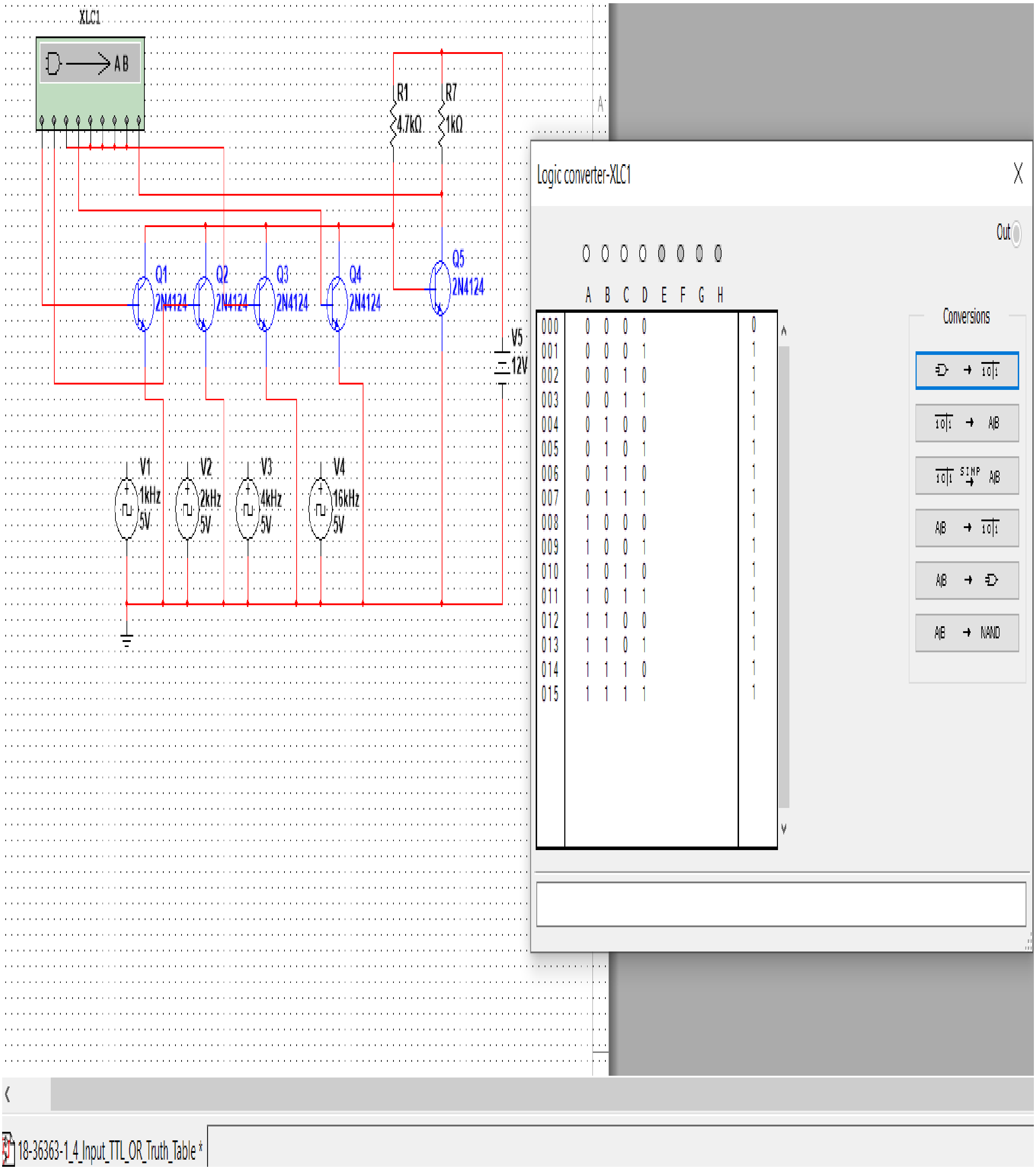


Fig 13: 4 Input TTL OR Truth Table.

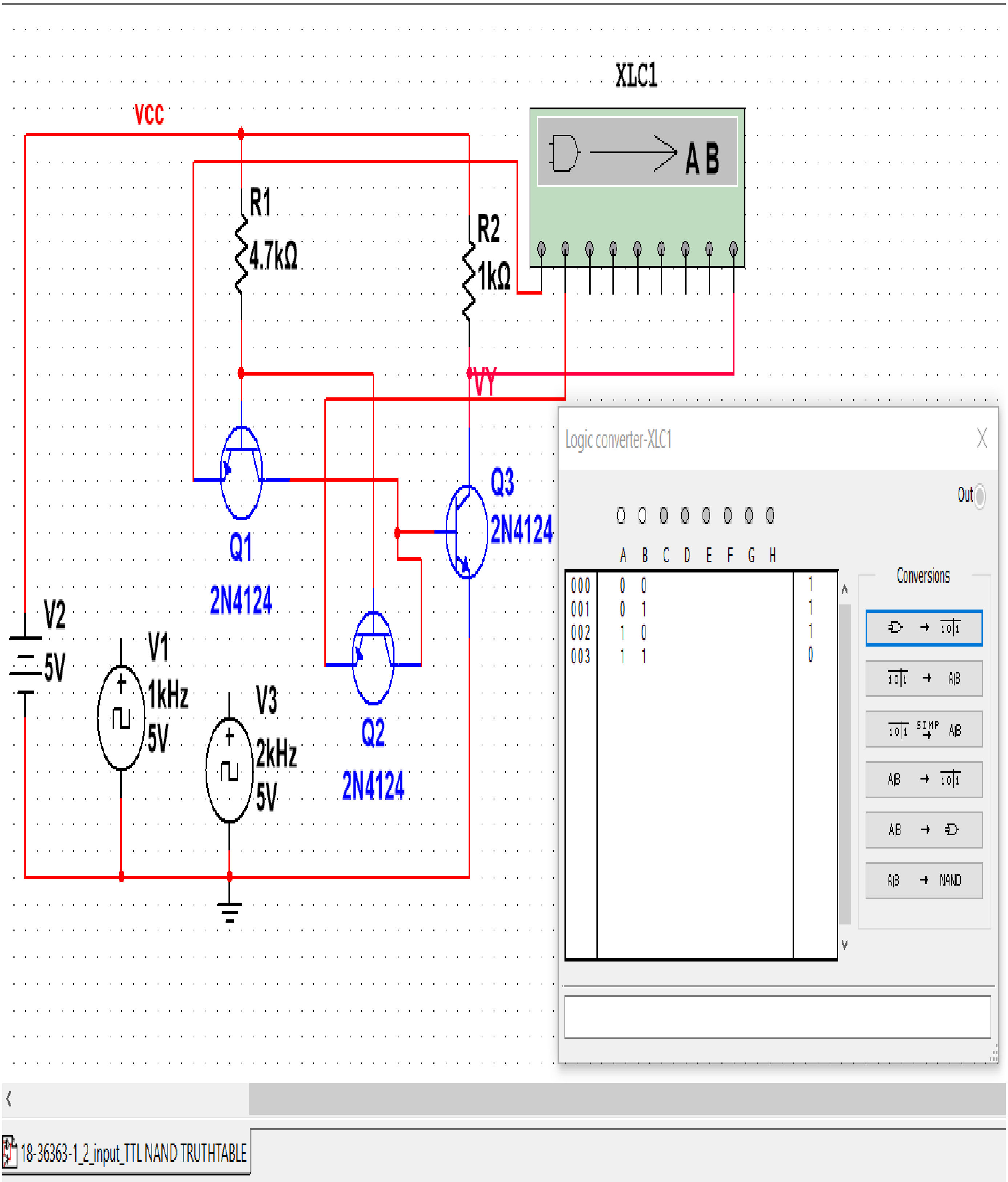


Fig 14: 2 Input TTL NAND Truth Table.

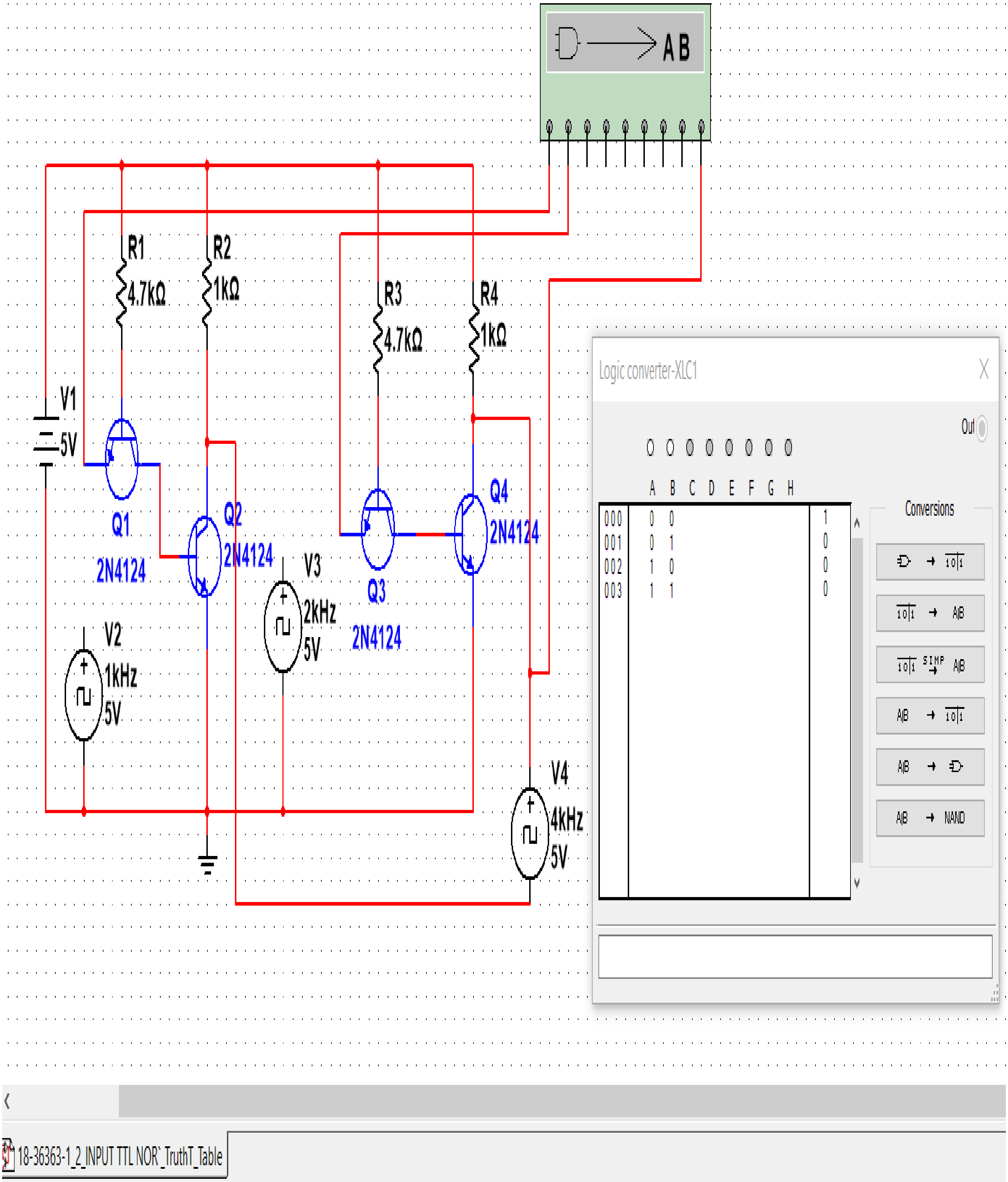


Fig 15: 2 Input TTL NOR Truth Table.