American International University- Bangladesh
Faculty of Engineering (EEE)
Digital Electronics Laboratory

Title: **Designing a Half Adder using CMOS.**

Introduction:
ADDER:

In electronics, an **adder** or **summer** is a digital circuit that performs addition of numbers. In many computers and other kinds of processors, adders are used not only in the arithmetic logic unit(s), but also in other parts of the processor, where they are used to calculate addresses, table indices, and similar operations.

Although adders can be constructed for many numerical representations, such as binary-coded decimal or excess-3, the most common adders operate on binary numbers. In cases where two's complement or ones' complement is being used to represent negative numbers, it is trivial to modify an adder into an adder–subtractor. Other signed number representations require a more complex adder.

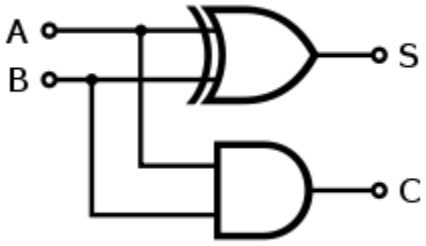

Fig-1 Half adder logic diagram

The **half adder** adds two single binary digits *A* and *B*. It has two outputs, sum (*S*) and carry (*C*). The carry signal represents an overflow into the next digit of a multi-digit addition. The value of the sum is 2*C* + *S*. The simplest half-adder design, pictured above, incorporates an XOR gate for *S* and an AND gate for *C*. With the addition of an OR gate to combine their carry outputs, two half adders can be combined to make a full adder.

The half-adder adds two input bits and generate carry and sum which are the two outputs of half-adder. The input variables of a Half adder are called the Augend and addend bits. The output variables are the Sum and Carry. The

Truth table and equations for the Half adder are :

$$\mathrm{S} = A \oplus B$$

$$\mathrm{C} = AB$$

A	B	A+B	S	C
0	0	0	0	0
0	1	1	1	0
1	0	1	1	0
1	1	2	0	1

This experiment is to help the student in understanding the design at the transistor level.

Theory and Methodology:

To design any logic circuit first the truth table is needed to be established using different combinations of logic '0' and '1' to get the desired output. After that the gate level design is found from which transistor level design is done using desired transistors. Here CMOS is used for the transistor level design of the Half Adder. The whole process is given step wise below:

Half Adder:

Gate Level Design:

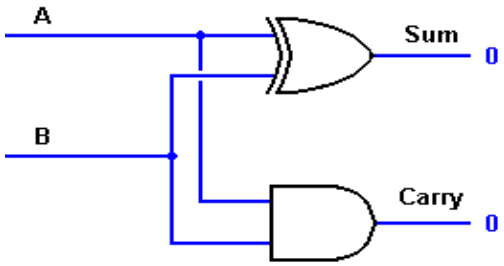

Fig-2 Logic diagram of a Half Adder.

Equation of Sum = A (XOR) B

$$= A\bar{B} + \bar{A}B$$

This equation can be rewritten as = $\overline{\overline{A\bar{B}} + \overline{\bar{A}B}}$

$$= \overline{AB + \bar{A}\bar{B}}$$

Equation of Carry= AB

Pre-Lab Homework:

1. Develop the Truth table for a half adder.
2. Develop the truth table for a full adder along with circuit diagram and equations. Explain the equations.

Students must install PSpice/LTSpice/ Psim software and MUST present the simulation results using transistors to the instructor before the start of the experiment.

Apparatus:

1. PMOS,
2. NMOS,
3. IC 7404(Inverter).
4. Connecting wires.
5. Trainer Board

Precautions:

Have your instructor check all your connections after you are done setting up the circuit and make sure that you apply only enough voltage (within V_{DD}) to turn on the transistors and/or chip, otherwise it may get damaged.

Experimental Procedure:

Construct the Half adder circuit using CMOS on your breadboard based on provided expression and truth table. At first draw the schematic circuit diagram for the SUM and CARRY then show to the Instructor. After that record the values in the table below.

Input A	Input B	Carry Out	Sum
0 V	0 V		
0 V	5 V		
5 V	0 V		
5 V	5 V		

Results and Discussion:

Students will summarize the experiment and discuss it as a whole. Interpret the data/findings and determine the extent to which the experiment was successful in complying with the goal that was initially set. Discuss any mistake you might have made while conducting the investigation and describe ways the study could have been improved.

Report:

1. Document the data acquired from the hardware, from simulation as well as the expected values for the CarryOut and Sum of the Half Adder.

2. Draw the circuit diagram of a Full Adder using CMOS.

Reference(s):

1. Thomas L. Floyd, *Digital Fundamentals*, 9th Edition, 2006, Prentice Hall.