

2)

$S_U \overline{E_P} \overline{L_M} E_I$
0 0 1 0
2

$\overline{L_I} \overline{L_A} E_A \overline{C_E}$
1 1 0 1
D

$E_U \overline{L_B} \overline{L_O} C_P$
0 1 1 0
6

Control Rom:

Address	CON	Active Pin	Routine
0H	4D6H	$E_P, \overline{L_M}$ (T_1)	Fetch
1H	2D7H	C_P (T_2)	
2H	246H	$\overline{C_E}, \overline{L_I}$ (T_3)	
3H	1D6H	$E_I, \overline{L_M}$ (T_4)	LDA
4H	286H	$\overline{C_E}, \overline{L_A}$ (T_5)	
5H	2D6H	None (T_6)	
6H	1D6H	$E_I, \overline{L_M}$ (T_4)	ADD
7H	2C2H	$\overline{C_E}, \overline{L_B}$ (T_5)	
8H	29EH	$E_U, \overline{L_A}$ (T_6)	
9H	1D6H	$E_I, \overline{L_M}$ (T_4)	SUB
AH	2C2H	$\overline{C_E}, \overline{L_B}$ (T_5)	
BH	A9EH	$E_U, S_U, \overline{L_A}$ (T_6)	
CH	2F4H	$E_A, \overline{L_O}$ (T_4)	OUT
DH	2D6H	None (T_5)	
EH	2D6H	None (T_6)	
FH	X	X	NOT USED

a) Consider the following control word and op-codes.

$S_U \overline{E_P} \overline{L_M} E_I$

$\overline{L_I} \overline{L_A} E_A \overline{C_E}$

$E_U \overline{L_B} \overline{L_O} C_P$

Design SAP-1 address ROM and

SAP-1 control ROM.

MNEMONIC	OP CODE
LDA	0011
ADD	0000
SUB	0010
OUT	1100
HLT	1111

Address Rom:

Address	Content	Routine
0000	0110	ADD
0001	X	None
0010	1001	SUB
0011	0011	LDA
0100	X	None
0101	X	None
0110	X	None
0111	X	None
1000	X	None
1001	X	None
1010	X	None
1011	X	None
1100	1100	OUT
1101	X	None
1110	X	None
1111	X	None

(b) Write object code for following operation, $out = 3^2$ In a SAP-1 processor. Also show the contents of the registers for each operation in different time cycles. Consider the op-code from problem (a).

$$3^2 = 3 + 3 + 3$$

Source Code		Object Code	
Address	Data	Address	Data
0H	LDA 9H	0H	39H
1H	ADD AH	1H	0AH
2H	ADD BH	2H	0BH
3H	OUT	3H	CXH
4H	HLT	4H	FXH
5H	FFH	5H	FFH
6H	FFH	6H	FFH
7H	FFH	7H	FFH
8H	FFH	8H	FFH
9H	03H	9H	03H
AH	03H	AH	03H
BH	03H	BH	03H
CH	FFH	CH	FFH
DH	FFH	DH	FFH
EH	FFH	EH	FFH
FH	FFH	FH	FFH

LDA 9H

	T1	T2	T3	T4	T5	T6
PC (4 Bit)	0H	1H	1H	1H	1H	1H
MAR (4 Bit)	0H	0H	0H	9H	9H	9H
IR (8 Bit)			39H	39H	39H	39H
A (8 Bit)					03H	03H
B (8 Bit)						
O/P R (8 Bit)						

ADD AH

	T1	T2	T3	T4	T5	T6
PC	1H	2H	2H	2H	2H	2H
MAR	1H	1H	1H	AH	AH	AH
IR	39H	39H	0AH	0AH	0AH	0AH
A	03H	03H	03H	03H	03H	06H
B					03H	03H
O/P R						

ADD BH

	T1	T2	T3	T4	T5	T6
PC	2H	3H	3H	3H	3H	3H
MAR	2H	2H	2H	BH	BH	BH
IR	0AH	0AH	0BH	0BH	0BH	0BH
A	06H	06H	06H	06H	06H	09H
B	03H	03H	03H	03H	03H	03H
O/P R						

OUT

	T1	T2	T3	T4	T5	T6
PC	3H	4H	4H	4H	4H	4H
MAR	3H	3H	3H	3H	3H	3H
IR	0BH	0BH	CXH	CXH	CXH	CXH
A	09H	09H	09H	09H	09H	09H
B	03H	03H	03H	03H	03H	03H
O/P R				09H	09H	09H