Winter Semicondutor School (WSS) Semiconductor Fabrication 101

Assignment 2

Student Name: _____

Roll Number: _____

December 19, 2025

Instructions

- Write your answers clearly and concisely.

- Drive links will be asked in Google Form.

- Submit as a PDF before the deadline, which is 23 Dec, which contains answers for ques 1,2,3,5

- Tentative weightage of this assignment is 20 + 10 per cent.

Problem 1 (1.5)

If the size of the unit cell of silicon is 0.54 nm, how realistic is your prediction of the size reduction? In short, when do you predict the breakdown of Moore's law?

Problem 2 (2)

Distinguish between Czochralski and float zone technique processes. Why do you think the float zone technique is harder to implement for larger wafers?

Problem 3 (1.5)

Distinguish, using chemical reactions, the two types of oxidation processes. Which one do you think would have the faster rate and why?

Problem 4: Simulation exercise (15)

Participants are required to record videos for any TWO semiconductor fabrication processes of their choice in **vfablab**, which is the last module in the Purdue course, adhering to the guidelines below.

Maximum duration: 3 minutes per video (You can extend if required)

Submission mode: 2 drive links of your screen recording.

Videos should be recorded in assessment mode not in training mode, which will be penalized as per below(see evaluation criteria below).

Audio narration while recording and doing steps in **vfalab**. You must continuously explain:

- The process steps you are performing

- The underlying theory and purpose of the process

- Relevant physical concepts and expected outcomes

The explanation should be clear, technical, and elaborative, not just a procedural walkthrough.
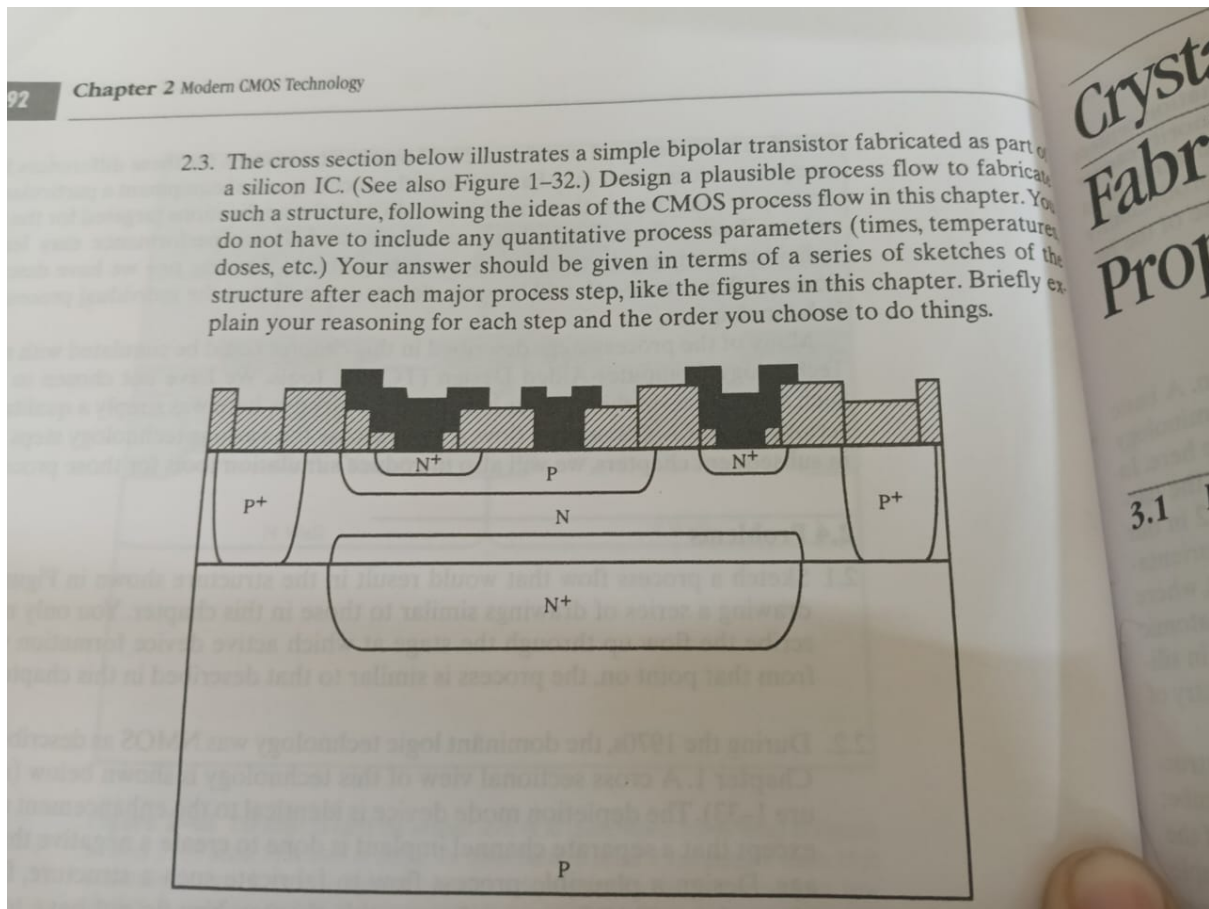
Evaluation Criteria
Hands-on implementation: 50%
Theoretical explanation: 50%
Important Penalty Rule
If the hands-on work is done in training mode, 50% marks will be deducted from the hands-on component, seperate to theory explanation.

Problem 5 (10 points) BONUS

2.3. The cross section below illustrates a simple bipolar transistor fabricated as part of a silicon IC. (See also Figure 1–32.) Design a plausible process flow to fabricate such a structure, following the ideas of the CMOS process flow in this chapter. You do not have to include any quantitative process parameters (times, temperatures, doses, etc.) Your answer should be given in terms of a series of sketches of the structure after each major process step, like the figures in this chapter. Briefly explain your reasoning for each step and the order you choose to do things.

Please refer to the reference book PDF provided in the GitHub repository.
   silicon-vlsi-technology.pdf
   This question is taken from the exercise section of the Chapter 2 in that book. You may consult the book for background theory and context while attempting the question.

References

- Plummer, Deal, Griffin, *Silicon VLSI Technology.*

- Semiconductor Fabrication 101 (Purdue Univ.)

- NPTEL Lectures by Prof. Parasuraman