DAY-76
#100DAYSOFRTL

AIM:--- IMPLEMENTATION OF 4-BIT PARALLE IN PARALLE OUT (PIPO).

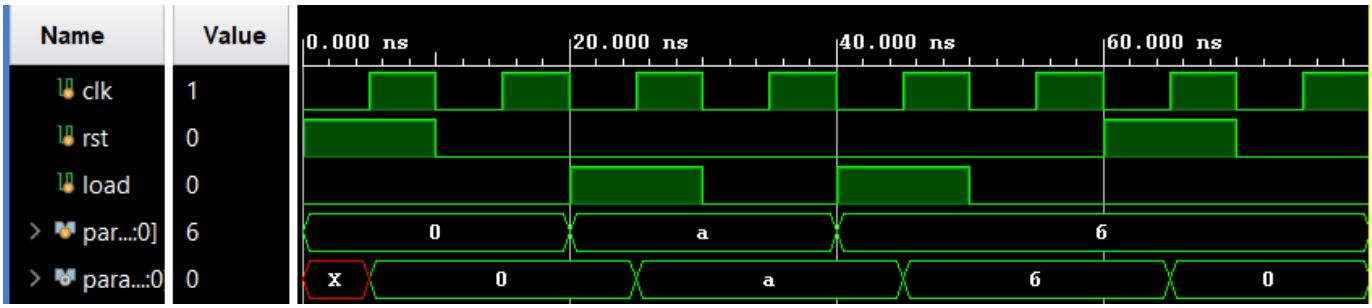
VERILOG CODE:--

```
module pipo (
    input clk,
    input rst,
    input load,
    input [3:0] parallel_in,
    output [3:0] parallel_out
);

    reg [3:0] reg_data;

    always @(posedge clk) begin
        if (rst) begin
            reg_data <= 4'b0000;
        end else if (load) begin
            reg_data <= parallel_in;
        end
    end

    assign parallel_out = reg_data;

endmodule
```

TESTBENCH CODE:---

```
module tb_pipo;
    reg clk;
    reg rst;
    reg load;
    reg [3:0] parallel_in;

    wire [3:0] parallel_out;

    pipo uut (
        .clk(clk),
        .rst(rst),
        .load(load),
        .parallel_in(parallel_in),
        .parallel_out(parallel_out)
    );

    initial begin
        clk = 0;
        forever #5 clk = ~clk;
    end

    initial begin

        rst = 0;
        load = 0;
        parallel_in = 4'b0000;

        rst = 1;
        #10;
        rst = 0;
        #10;
```

WAVEFORM:-----



SCHEMATIC BLOCK :-------