DAY-61
#100DAYSOFRTL

AIM:--IMPLEMENTATION OF JK FLIP-FLOP USING D FLIP-FLOP.

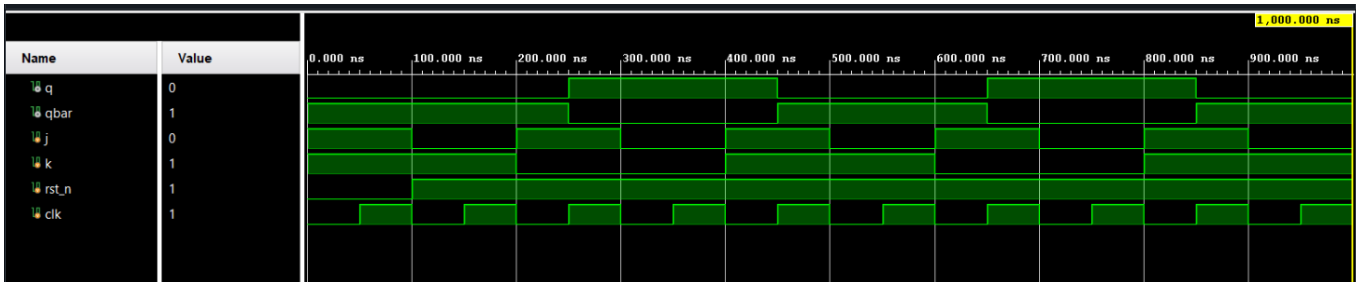
VERILOG CODE:--

```
1  module d_flipflop(input clk,d,output reg q,qbar);
2  always@(posedge clk)
3  begin
4
5  q<=d;
6  qbar<=~d;
7
8  end
9  endmodule
10
11 module d_to_jk(input clk,j,k,output q,qbar);
12 wire d;
13
14 assign d=q&~k + ~qbar&j;
15
16 d_flipflop dff(clk,d,q,qbar);
17 endmodule
18
```

TESTBENCH CODE:--

```
1  module d_to_jk_tb();
2  reg clk,j,k;
3  wire q,qbar;
4
5  jkff dut (clk,j,k,q,qbar);
6
7
8  always #5 clk = ~clk;
9
10 initial begin
11 clk = 0;
12 j = 0;
13 k = 0;
14
15     #10; j = 0; k = 1;
16     #10 ;j = 0; k = 0;
17     #10 ;j = 0; k = 1;
18     #10 ;j = 1; k = 0;
19     #10 ;j = 1; k = 1;
20      $finish;
21
22
23
24 end
25 endmodule
26
```

WAVEFORM:--



SCHEMATIC:-