DAY-97
#100DAYSOFRTL

AIM:--- IMPLEMENTATION OF MOORE MACHINE.

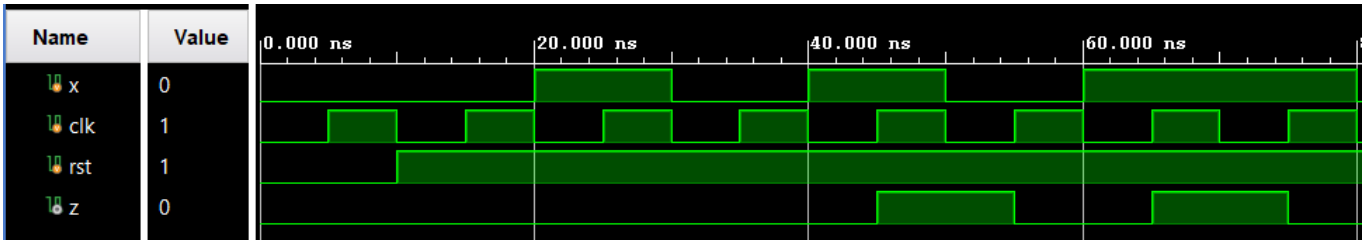
VERILOG CODE:--

```
module moore_seq_detect (input x,
                         input clk,
                         input rst,
                         output reg z);

parameter s0 = 2'b00, s1 = 2'b01, s2 = 2'b10, s3 = 2'b11;

  reg[1:0] current_state, next_state;

    always @(posedge clk or negedge rst)
    begin
      if(!rst)
         current_state <= s0;
         else
         current_state <= next_state;
    end

   always@(*)
    begin
      case (current_state)
      s0 : begin
            if (x == 1)
                next_state = s1;
                else
                next_state = s0;
            end
      s1 : begin
            if (x == 1)
                next_state = s1;
                else
                next_state = s2;
            end
```

TESTBENCH CODE:---

```
module tb_moore_seq_detect;

  reg x;
  reg clk;
  reg rst;
  wire z;

  moore_seq_detect uut (
    .x(x),
    .clk(clk),
    .rst(rst),
    .z(z)
  );

  always #5 clk = ~clk;

  initial begin
    clk = 0;
    rst = 0;
    x = 0;

    #10 rst = 1;

    #10 x = 1;
    #10 x = 0;
    #10 x = 1;
    #10 x = 0;
    #10 x = 1;

    #10 x = 1;
    #10 x = 0;
    #10 x = 1;
```

WAVEFORM:-----



SCHEMATIC BLOCK :-------