DAY-77
#100DAYSOFRTL

AIM:--- IMPLEMENTATION OF UNIVERSAL SHIFT REGISTER .

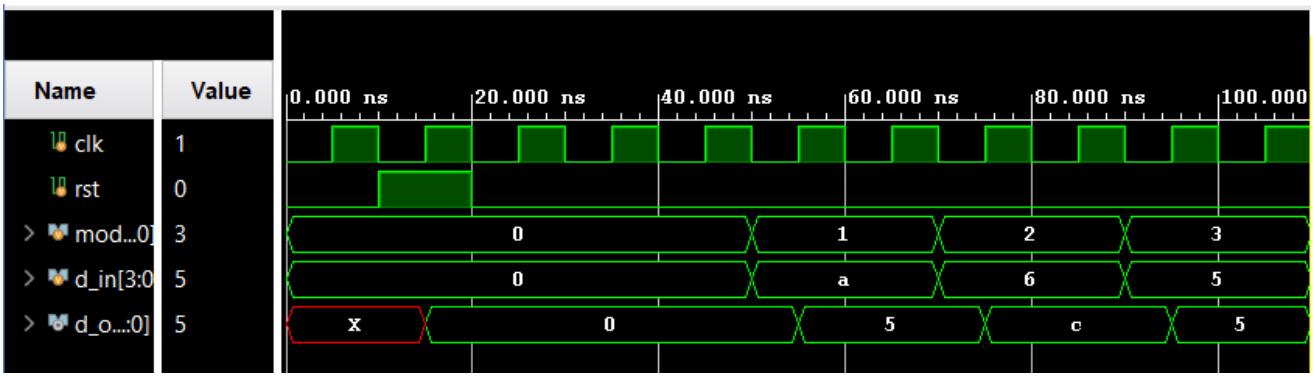
VERILOG CODE:--

```
module universal_shift_reg(input clk,rst,[1:0]mode,[3:0]d_in, output reg[3:0]d_out);
//  wire [1:0]mode;
//  wire [3:0]d_in;

 always @(posedge clk)
  begin
    if(rst)
      d_out <= 0;
    else
      begin
        case(mode)
         2'b00 : d_out <= d_out;       // locked mode, do nothing
         2'b01 : d_out <= {d_in[0], d_in[3:1]};//right_shift;
         2'b10 : d_out <= {d_in[2:0], d_in[3]};//left_shift;
         2'b11 : d_out <= d_in;        // parallel in parallel out
        endcase
      end
  end

endmodule
```

TESTBENCH CODE:---

```
1  module universal_shift_reg_tb();
2    reg clk,rst;
3    reg [1:0]mode;
4    reg [3:0]d_in;
5    wire [3:0]d_out;
6
7    ///Instantiation
8    universal_shift_reg usr(clk,rst,mode,d_in,d_out);
9
10   ///clock Initialization
11   initial...
17
18
19   task initialize();...
22
23   task reset();
24   begin
25     @(negedge clk)
26     rst = 1'b1;
27     @(negedge clk)
28     rst = 1'b0;
29   end
30   endtask
31
32   task inputs(input [3:0]i);...
35
36   initial
37   begin...
57
58   initial #110 $finish;
59
60 endmodule
```

WAVEFORM:-----



SCHEMATIC BLOCK :-------