DAY-41
#100DAYSOFRTL

AIM:--IMPLEMENTATION OF D FLIP-FLOP WITH SYN RST.

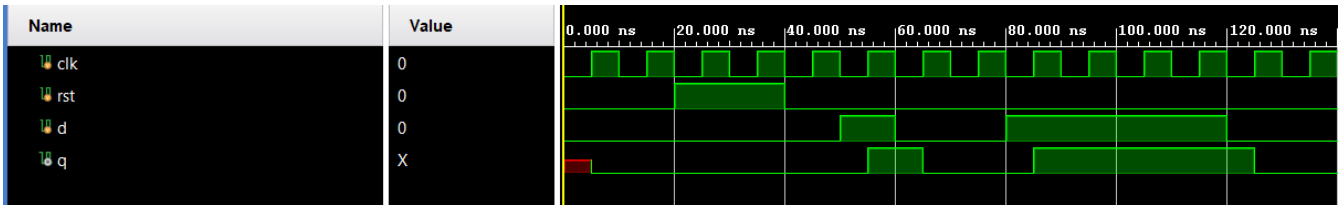
VERILOG CODE:--

```
1   module dffsynrst (clk,reset,d,q);
2   input clk,reset,d;
3   output reg q;
4
5   always @ (posedge clk)begin
6       if(reset)
7           q <= 0;
8       else
9           q <= d;
10  end
11
12  endmodule
```

TESTBENCH CODE:--

```
1   module dffsynrst_tb;
2
3       reg clk, rst, d;
4       wire q;
5
6       dffsynrst dff_inst (clk,rst,d,q);
7
8       always #5 clk = ~clk;
9
10      initial begin
11
12          clk = 0;
13          rst = 0;
14          d = 0;
15
16          #20 rst = 1;
17          #20 rst = 0;
18
19          #10 d = 1; // Apply input D = 1
20          #10 d = 0; // Apply input D = 0
21
22          #20 d = 1; // Apply input D = 1
23          #20 d = 1; // Apply input D = 1
24
25          #20 d = 0; // Apply input D = 0
26          #20 d = 1; // Apply input D = 1
27           $finish;
28      end
29
30
31  endmodule
```

WAVEFORM:--



SCHEMATIC:--