# DAY-70
# #100DAYSOFRTL

**AIM:---** IMPLEMENTATION OF 4-BIT DOWN COUNTER.

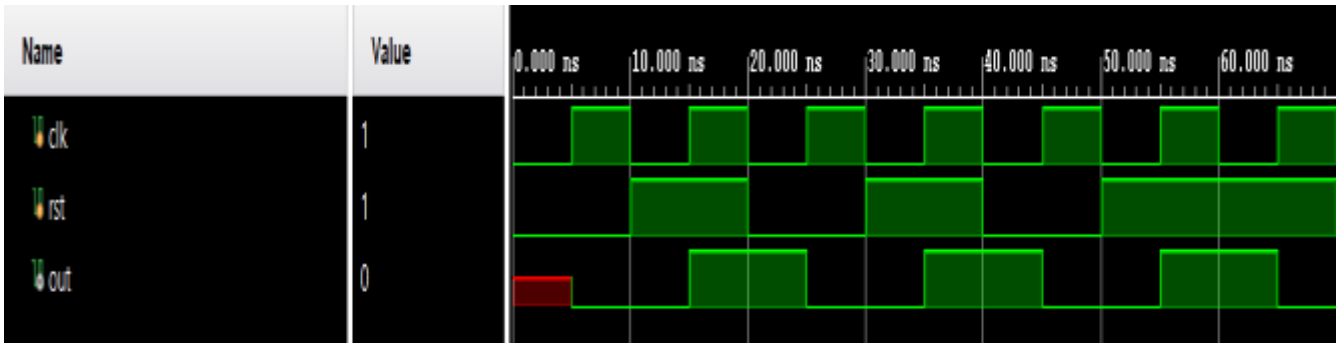
**VERILOG CODE:--**

```
1   module fourbitdown( clk,rst,out);
2
3   input clk,rst;
4   output reg[3:0] out ;
5
6   always@(posedge clk)
7   begin
8
9   if(rst==0)
10  out<=0;
11
12  else
13  out<=out-1;
14
15
16  end
17  endmodule
18
```

## TESTBENCH CODE:---

```
1   module fourbitdown_tb();
2
3   reg clk,rst;
4   wire out;
5
6   fourbitdown dut ( clk,rst,out);
7
8   always #5 clk=~clk;
9
10  initial
11  begin
12  clk=0;rst=0;
13
14  #10 rst=1;
15  #10 rst=0;
16  #10 rst=1;
17  #10 rst=0;
18  #10 rst=1;
19  #10 rst=1;
20  #10 rst=0;
21  #10 rst=0;
22  #10 rst=1;
23  $finish ;
24
25
26  end
27  endmodule
28
```

## WAVEFORM:-----




## SCHEMATIC :-------