DAY-2
#100DAYSOFRTL

AIM:--implement half adder using Verilog.

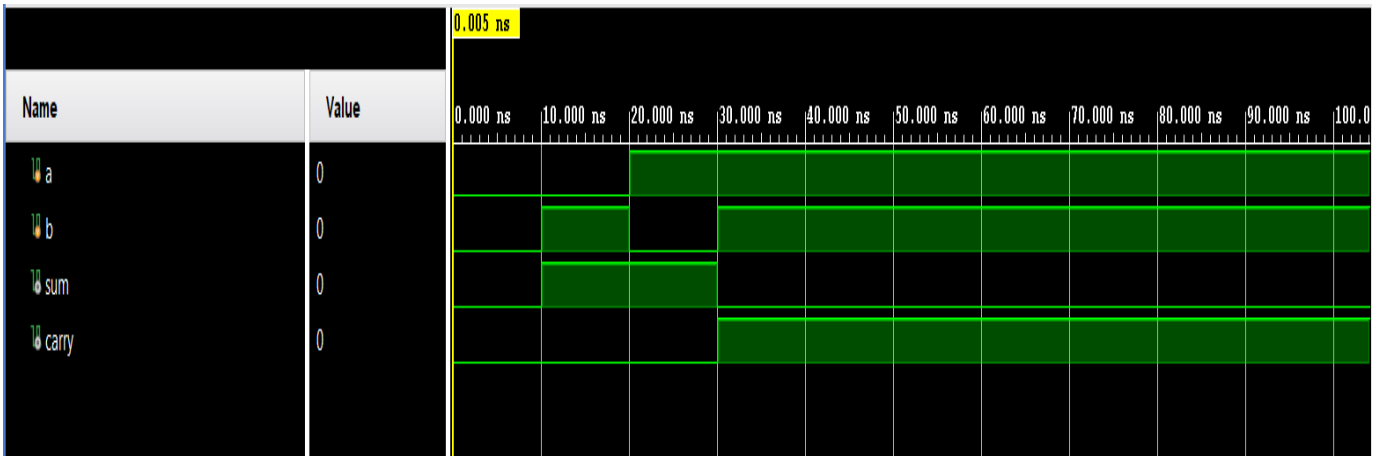
RTL CODE:--

```
1   module ha(input a,b, output sum,carry);
2
3   assign sum=a^b;
4   assign carry=a&b;
5
6   endmodule
7
8
9
10
11
```

TESTBENCH:--

```
1   module ha_tb();
2
3   reg a,b;
4   wire sum,carry;
5
6   ha dut(a,b,sum,carry);
7   initial begin
8
9   a=0;b=0;
10
11  #10
12  a=0;b=1;
13
14  #10
15  a=1;b=0;
16
17  #10
18  a=1;b=1;
19
20  end
21
22
23  endmodule
24
```

WAVEFORM:--



SCHEMATIC:--