DAY-36
#100DAYSOFRTL

AIM:--IMPLEMENTATION OF SR FLIP-FLOP WITHOUT RESET .

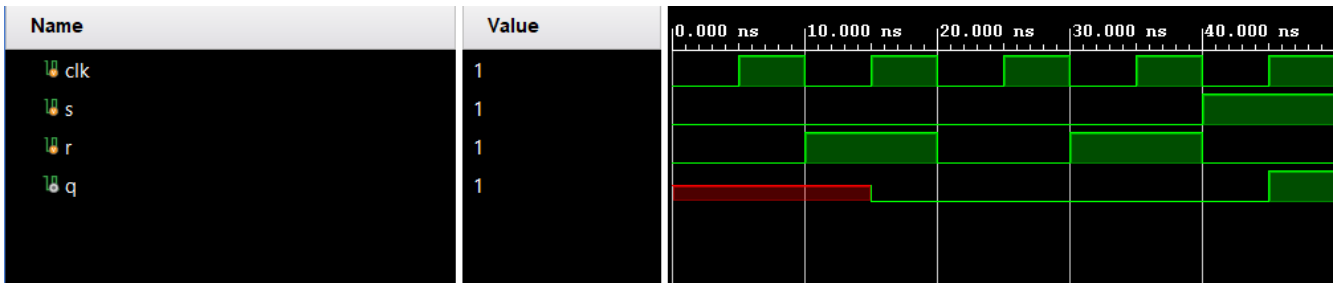
VERILOG CODE:--

```
module srffnand(
    input clk, s, r,
    output reg q
);

always @(posedge clk) begin
    case({s,r})
        2'b00: q <= q; // No change
        2'b01: q <= 0; // Reset
        2'b10: q <= 1; // Set
        2'b11: q <= 1'bx; // Invalid state
    endcase
end

endmodule
```

TESTBENCH CODE:--

```
1   module srffnand_tb();
2
3   reg clk, s, r;
4   wire q;
5
6   srffnand dut (clk,s,r,q);
7
8   always #5 clk = ~clk;
9
10  initial begin
11  clk = 0;
12  s = 0;
13  r = 0;
14
15      #10 s = 0; r = 1;
16      #10 s = 0; r = 0;
17      #10 s = 0; r = 1;
18      #10 s = 1; r = 0;
19      #10 s = 1; r = 1;
20       $finish;
21  end
22
23  endmodule
24
```

WAVEFORM:--



SCHEMATIC:--