DAY-42
#100DAYSOFRTL

AIM:--IMPLEMENTATION OF T FLIP-FLOP.

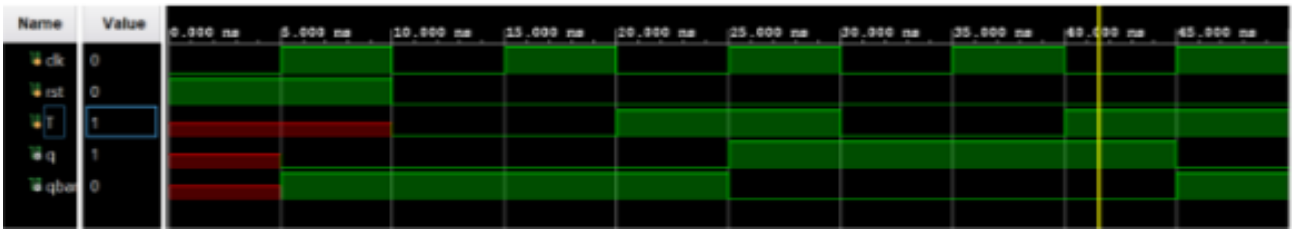
VERILOG CODE:--

```
1   module tff(clk,t,q);
2
3   input clk,t;
4   output reg q;
5
6   always @(posedge clk)
7   begin
8     if (t==0)
9     q=q;
10
11    else
12    q=(~q);
13
14    end
15    endmodule
```

TESTBENCH CODE:--

```
1   module tff_tb();
2
3   reg clk,t;
4   wire q;
5
6   tff dut (clk,t,q);
7
8   always #5 clk=~clk;
9
10  initial
11  begin
12
13  clk=0;t=0;
14
15  #10 clk=1;
16
17  #10 t=0;
18  #10 t=1;
19
20  $finish;
21
22  end
23  endmodule
```

WAVEFORM:--



SCHEMATIC:--