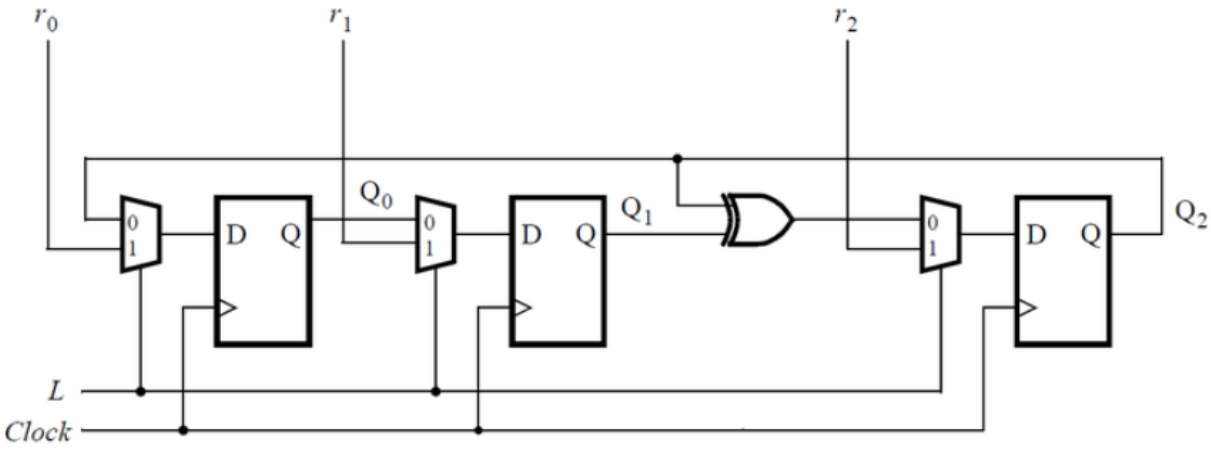
DAY-47
#100DAYSOFRTL

PROBLEM STATEMENT:--

1.

Consider the sequential circuit below:



Write your solution here

[Load a previous submission] Load

```
module top_module (
    input clk,
    input L,
    input r_in,
    input q_in,
    output reg Q);

    always@(posedge clk )
        begin
            if(L)
                Q<= r_in;
            else
                Q<=q_in;


        end
    endmodule

```

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Upload a source file...

mt2015_muxdff — Compile and simulate

Running Quartus synthesis. Show Quartus messages...
Running ModelSim simulation. Show Modelsim messages...

Status: Success!

You have solved 79 problems. See my progress...