DAY-9
#100DAYSOFRTL

AIM:--- IMPLEMENTATION OF SEQUENCE 1101 RECOGNIZER USING FSM.

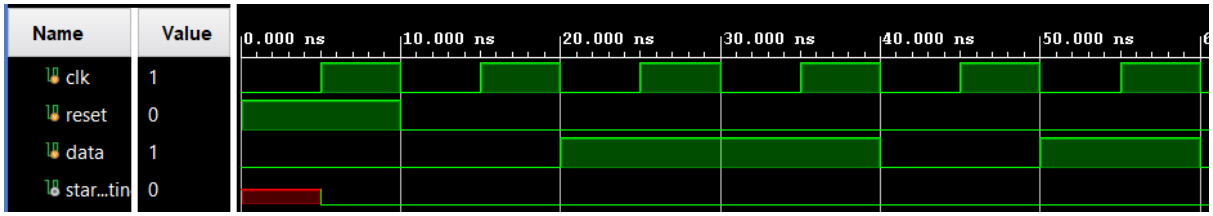
VERILOG CODE:--

```
module top_module (
    input clk,
    input reset,
    input data,
    output reg start_shifting
);

    parameter S0 = 3'b000;
    parameter S1 = 3'b001;
    parameter S2 = 3'b010;
    parameter S3 = 3'b011;
    parameter S4 = 3'b100;

    reg [2:0] state, next_state;

    always @(*) begin
        case (state)
            S0: next_state = data ? S1 : S0;
            S1: next_state = data ? S2 : S0;
            S2: next_state = data ? S2 : S3;
            S3: next_state = data ? S4 : S0;
            S4: next_state = S4;
            default: next_state = S0;
        endcase
    end

    always @(posedge clk) begin
        if (reset)
            state <= S0;
        else
            state <= next_state;
    end
```

TESTBENCH CODE:---

```
module tb_top_module;

    reg clk;
    reg reset;
    reg data;
    wire start_shifting;

    top_module uut (
        .clk(clk),
        .reset(reset),
        .data(data),
        .start_shifting(start_shifting)
    );

    always begin
        #5 clk = ~clk;
    end

    initial begin
        clk = 0;
        reset = 0;
        data = 0;

        reset = 1;
        #10;
        reset = 0;

        data = 0;
        #10;

        data = 1;
        #10;
```

WAVEFORM:-----



SCHEMATIC BLOCK :-------