DAY-57
#100DAYSOFRTL

AIM:--IMPLEMENTATION OF SR FLIP-FLOP USING JK FLIP-FLOP.

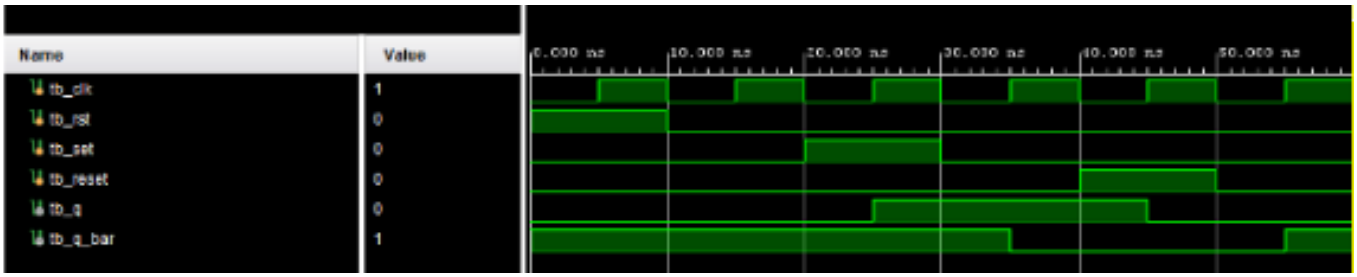
VERILOG CODE:--

```
module jk_flipflop( input clk, j, k,output reg q, qbar);

    always @(posedge clk)
    begin
        q=1'b1;
        qbar = 1'b1;

        case ({j, k})
            2'b00: begin
                q <= q;
                qbar <= qbar;end
            2'b01: begin
                q <= 1'b0;
                qbar <= 1'b1;end
            2'b10: begin
                q <= 1'b1;
                qbar <= 1'b0;end
            2'b11: begin
                q <= 1'bx;
                qbar <= 1'bx;end
        endcase
    end
endmodule
module jk_to_sr(
    input clk,s,r,
    output q, qbar);
wire j, k;
 assign j = s;
    assign k = r;
jk_flipflop jkff (clk, j, k, q, qbar);
endmodule
```

TESTBENCH CODE:--

```
module jk_to_sr_tb();
    reg s, r, clk;
    wire q, qbar;

    jk_to_jr dut (clk,s,r,q,qbar);
    initial
    clk = 0;
    always #5 clk = ~clk;


    initial begin


        s = 0;r = 0;#10;
        s = 0;r = 1;#10;
        s = 1;r = 0;#10;
        s = 1;r = 1;#10;

        #20;

$finish;
end
endmodule
```

WAVEFORM:--



SCHEMATIC:-