DAY-73
#100DAYSOFRTL

AIM:--- IMPLEMENTATION OF 4-BIT SERIAL IN SERIAL OUT (SISO).

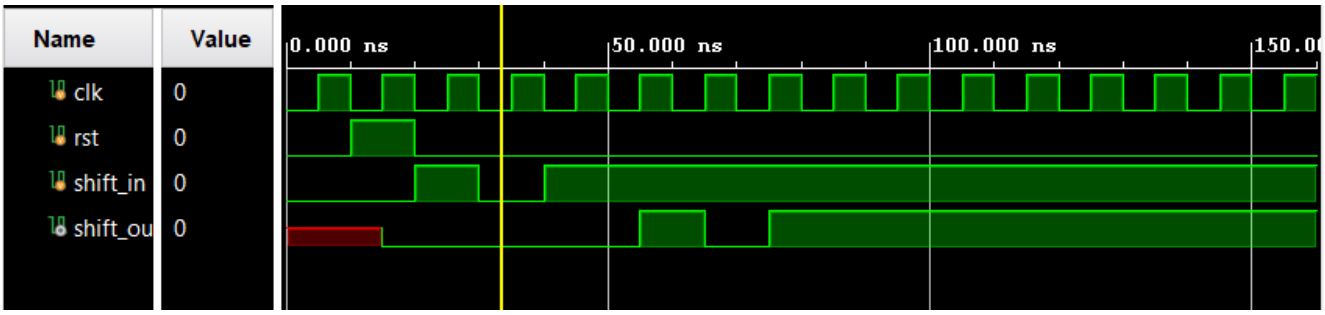
VERILOG CODE:--

```
module siso (
    input wire clk,
    input wire rst,
    input wire shift_in,
    output wire shift_out
);
 reg [3:0] q;

    always @(posedge clk ) begin
        if (rst) begin

            q <= 4'b0000;
        end

        else
         begin
            q <= {shift_in, q[3:1]};
        end
    end

    assign shift_out = q[0];

endmodule
```

TESTBENCH CODE:---

```
module tb_siso();
reg clk;
reg rst;
reg shift_in;
wire shift_out;

    siso uut (
        .clk(clk),
        .rst(rst),
        .shift_in(shift_in),
        .shift_out(shift_out)
    );
initial begin
        clk = 0;
        forever #5 clk = ~clk;
    end
initial begin
        rst = 0;
        shift_in = 0;
#10;
        rst = 1;
        #10;
        rst = 0;
 shift_in = 1; #10;
        shift_in = 0; #10;
        shift_in = 1; #10;
        shift_in = 1; #10;
#100;
$stop;
    end
endmodule
```

WAVEFORM:-----



SCHEMATIC :-------