DAY-35
#100DAYSOFRTL

AIM:--IMPLEMENTATION OF SR LATCH USING NAND GATES.

VERILOG CODE:--

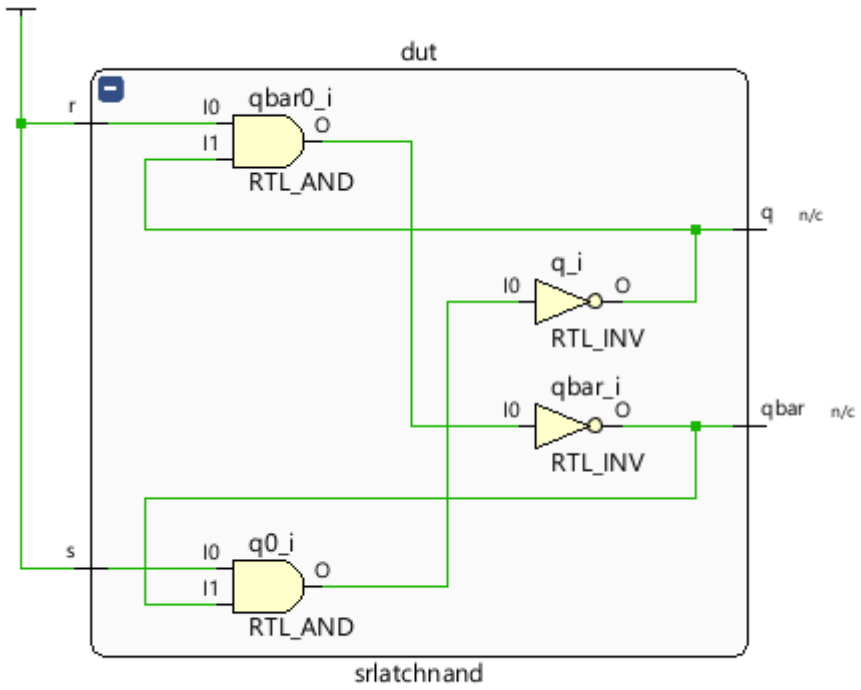
```
1  module srlatchnand( s,r ,q,qbar );
2  input s,r;
3  output q,qbar;
4
5  assign q=~(s & qbar);
6  assign qbar=~(r & q);
7
8  endmodule
9
```

TESTBENCH CODE:--

```
1   module srlatchnand_tb();
2
3   reg s,r;
4   wire q,qbar;
5
6   srlatchnand dut( s,r ,q,qbar );
7
8   initial
9   begin
10
11  #10;s=0 ; r=0;
12  #10;s=0 ; r=1;
13  #10;s=1 ; r=0;
14  #10;s=1 ; r=1;
15
16
17  $finish;
18
19  end
20  endmodule
21
```

WAVEFORM:--

SCHEMATIC:--



AIM:--IMPLEMENTATION OF SR LATCH USING NOR GATES.

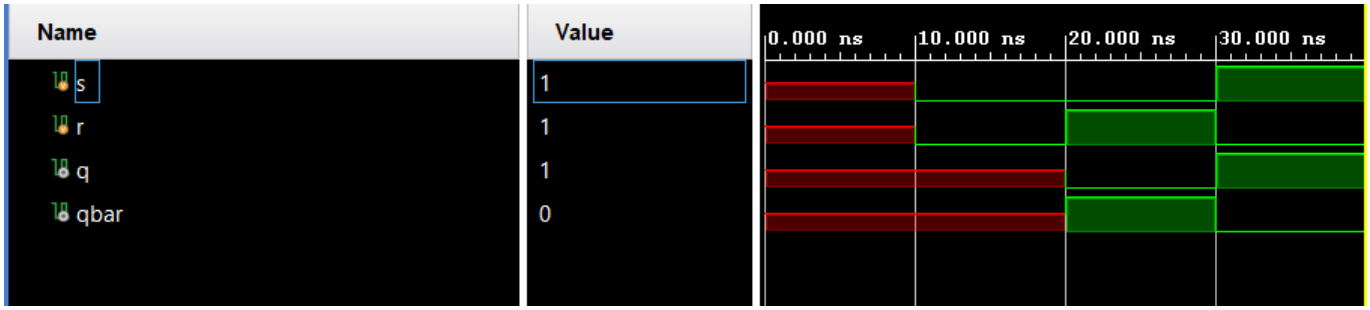
VERILOG CODE:--

```
1   module srlatchnor(s,r,q,qbar);
2
3   input s,r;
4   output q,qbar;
5
6   assign q=~(r | qbar);
7   assign qbar=~(s |q );
8
9   endmodule
10
```

TESTBENCH CODE:--

```
1   module srlatchnor_tb();
2
3   reg s,r;
4   wire q,qbar;
5
6   srlatchnor dut (s,r,q,qbar);
7
8   initial
9   begin
10
11  #10 ;s=0; r=0 ;
12  #10 ;s=0; r=1 ;
13  #10; s=1; r=0 ;
14  #10; s=1; r=1 ;
15
16  $finish;
17
18  end
19  endmodule
20
```

WAVEFORM:--



SCHEMATIC:--