DAY-9
#100DAYSOFRTL

1. Implement the following circuit:

Write your solution here

[Load a previous submission] Load

```
module top_module (
    input in,
    output out);

    assign out=in;

endmodule
```

Submit | Submit (new window)

Upload a source file...

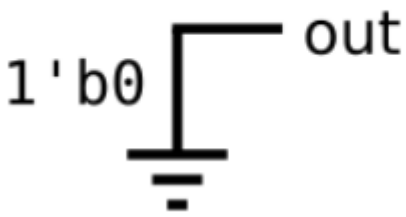
exams/m2014_q4h — Compile and simulate

Running Quartus synthesis. Show Quartus messages...
Running ModelSim simulation. Show Modelsim messages...

Status: Success!

You have solved 38 problems. See my progress...

2. Implement the following circuit:



Write your solution here

[Load a previous submission] Load

```
module top_module (
    output out);

    assign out=1'b0;

endmodule
```

Submit | Submit (new window)

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exams/m2014_q4i — Compile and simulate

Running Quartus synthesis. Show Quartus messages...
Running ModelSim simulation. Show Modelsim messages...

Status: Success!

You have solved 39 problems. See my progress...

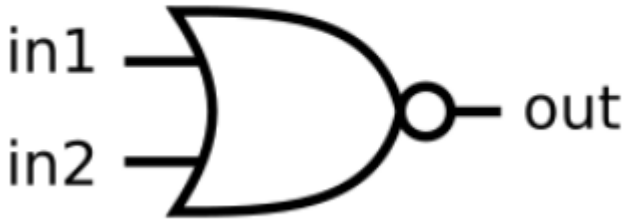
Warning messages that may be important

Quartus messages (Show all)

`Warning (13024): Output pins are stuck at VCC or GND`
This warning says that an output pin never changes (is "stuck"). This can sometimes indicate a bug if the output pin shouldn't be a constant. If this pin is not supposed to be constant, check for bugs that cause the value being assigned to never change (e.g., `assign a = x & ~x;`)

3.

Implement the following circuit:



Write your solution here

[Load a previous submission] Load

```
module top_module (
    input in1,
    input in2,
    output out);

    nor(out,in1,in2);

endmodule

```

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exams/m2014_q4e — Compile and simulate

Running Quartus synthesis. Show Quartus messages...
Running ModelSim simulation. Show Modelsim messages...

Status: Success!

You have solved 40 problems. See my progress...

4. Implement the following circuit:

Write your solution here

[Load a previous submission] Load

```
module top_module (
    input in1,
    input in2,
    output out);

    and(out,in1,~in2);

endmodule

```

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exams/m2014_q4f — Compile and simulate

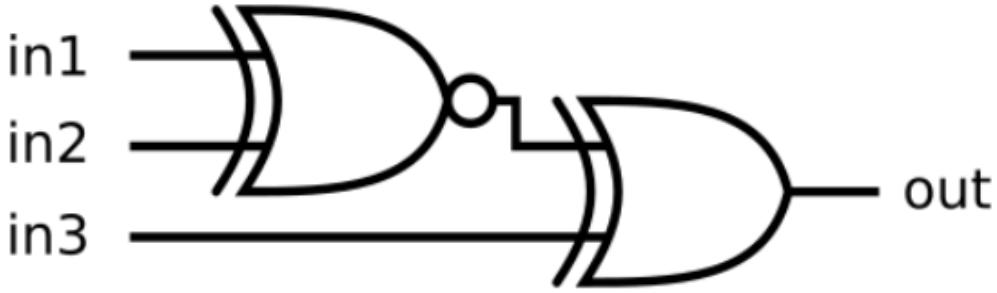
Running Quartus synthesis. Show Quartus messages...
Running ModelSim simulation. Show Modelsim messages...

Status: Success!

You have solved 41 problems. See my progress...

5.

Implement the following circuit:



Write your solution here

[Load a previous submission] Load

```
module top_module (
    input in1,
    input in2,
    input in3,
    output out);

wire t1;

    xnor(t1,in1,in2);
    xor(out,t1,in3);

endmodule
```

Submit | Submit (new window)

Upload a source file...

exams/m2014_q4g — Compile and simulate

Running Quartus synthesis. Show Quartus messages...
Running ModelSim simulation. Show Modelsim messages...

Status: Success!

You have solved 42 problems. See my progress...