DAY-6
#100DAYSOFRTL

AIM:--IMPLEMENTATION OF 4-BIT BINARY TO GREY CODE CONVERTER.

VERILOG RTL CODE:--

```
module bin_to_gr(
    input [3:0] b,
    output [3:0] g
);

    assign g[0] = b[1] ^ b[0];
    assign g[1] = b[2] ^ b[3];
    assign g[2] = b[3] ^ b[2];
    assign g[3] = b[3];

endmodule
```

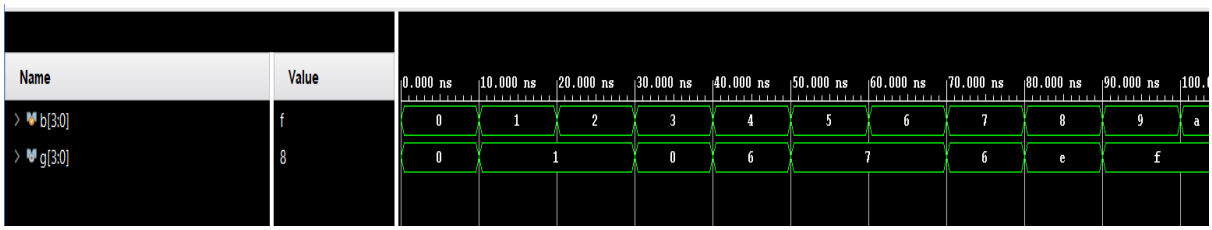
TESTBENCH CODE:--

```
module bin_to_gr_tb;        reg [3:0]b;
        wire [3:0]g;

        bin_to_gr dut (b,g);

        initial begin
        b=4'b0000;
        #10   b=4'b0001;
        #10   b=4'b0010;
        #10   b=4'b0011;
        #10   b=4'b0100;
        #10   b=4'b0101;
        #10   b=4'b0110;
        #10   b=4'b0111;
        #10   b=4'b1000;
        #10   b=4'b1001;
        #10   b=4'b1010;
        #10   b=4'b1011;
        #10   b=4'b1100;
        #10   b=4'b1101;
        #10   b=4'b1110;
        #10   b=4'b1111;
        end
endmodule
```

WAVEFORM:--



SCHEMATIC:--