DAY-38
#100DAYSOFRTL

AIM:--IMPLEMENTATION OF JK FLIP-FLOP WITH SYN RST.

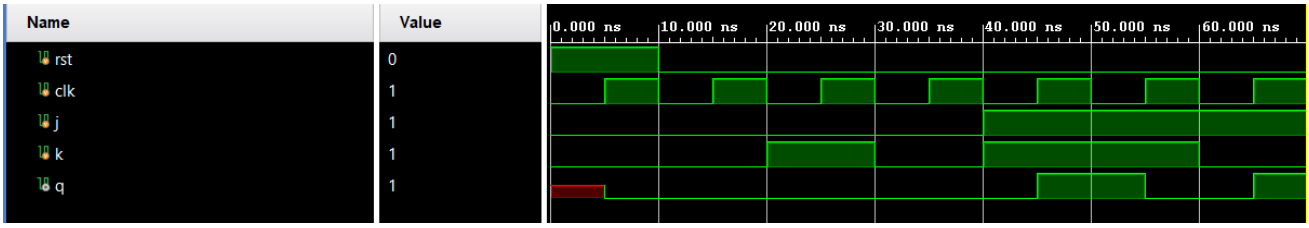
VERILOG CODE:--

```
module jkffwithsynrst( clk,rst,j,k,q);

input rst,clk,j,k;
output reg q;

always@(posedge clk)
begin
      if(rst)
      q<=0;

      else
      case({j,k})
    2'b00:q<=q;
    2'b01:q<=0;
    2'b10:q<=1;
    2'b11:q<=~q;

    default:q<=q;

endcase
end
endmodule
```

TESTBENCH CODE:--

```
1   module jkffwithsynrst_tb();
2
3   reg rst,clk,j,k;
4   wire q;
5
6   jkffwithsynrst dut ( clk,rst,j,k,q);
7
8   always #5 clk=~clk;
9
10  initial
11  begin
12
13  clk=0;rst=1;j=0;k=0;
14
15  #10 rst=0;
16
17  #10 j=0;k=1;
18  #10 j=0;k=0;
19  #10 j=1;k=1;
20  #10 j=1;k=1;
21  #10 j=1;k=0;
22  #10 j=1;k=1;
23  $finish;
24
25  end
26  endmodule
27
```

WAVEFORM:--



SCHEMATIC:--