DAY-71
#100DAYSOFRTL

AIM:--- IMPLEMENTATION OF 4-BIT JOHNSON COUNTER.

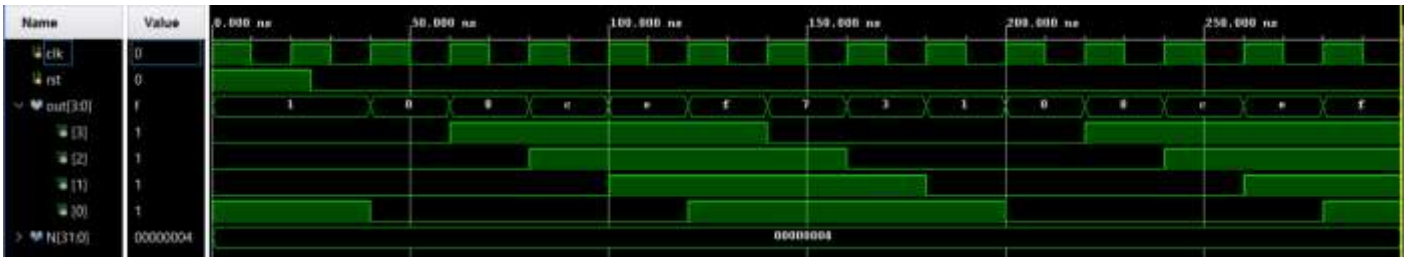
VERILOG CODE:--

```
1  module johnson_counter( out,reset,clk);
2  input clk,reset;
3  output [3:0] out;
4
5  reg [3:0] q;
6
7  always @(posedge clk)
8  begin
9
10 if(reset)
11  q=4'd0;
12  else
13     begin
14          q[3]<=q[2];
15          q[2]<=q[1];
16          q[1]<=q[0];
17          q[0]<=(~q[3]);
18     end
19  end
20
21 assign out=q;
22 endmodule
```

TESTBENCH CODE:---

```
module johnson_counter_tb();
  reg clk,rst;
  wire [3:0] out;

  johnson_counter dut (.out(out), .rst(rst), .clk(clk));

  always
    #5 clk =~clk;

  initial begin
    rst=1'b1; clk=1'b0;
   #20 rst= 1'b0;
  end

  initial
    begin
     $monitor( $time, " clk=%b, out= %b, rst=%b", clk,out,rst);
     #105  $stop;
   end

endmodule
```

WAVEFORM:-----



SCHEMATIC :-------