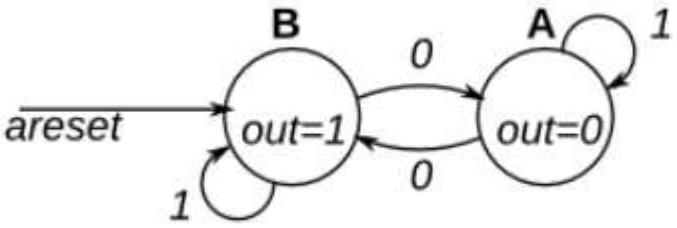
DAY-93
#100DAYSOFRTL

AIM:--- IMPLEMENTATION OF FINITE STATE MACHINE



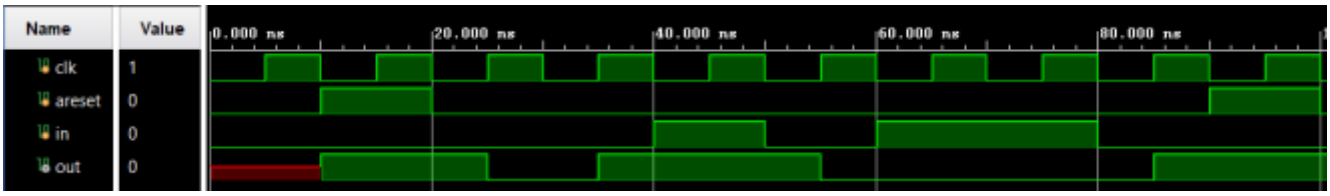
VERILOG CODE:--

```
module top_module(
    input clk,
    input areset,
    input in,
    output out
  );

    parameter A=0, B=1;
    reg state, next_state;

    always @(*) begin
        case(state)
            A : next_state = (in == 1) ? A : B;
            B : next_state = (in == 1) ? B : A;
        endcase
    end

    always @(posedge clk, posedge areset) begin
        if(areset) state <= B;
        else state <= next_state;
    end

    assign out = (state == B);

endmodule
```

TESTBENCH CODE:---

```
module top_module_tb;

  reg clk;
  reg areset;
  reg in;
  wire out;

  top_module uut (
    .clk(clk),
    .areset(areset),
    .in(in),
    .out(out)
  );


  always begin
    #5 clk = ~clk;
  end

  initial begin...

  initial begin
    $monitor("Time: %0d, clk: %b, areset: %b, in: %b, state: %b, out: %b", $time, clk, areset, in, uut.state, out);
  end

endmodule
```

WAVEFORM:-----



SCHEMATIC BLOCK :-------