DAY-96
#100DAYSOFRTL

AIM:--- IMPLEMENTATION OF MEALY MACHINE.

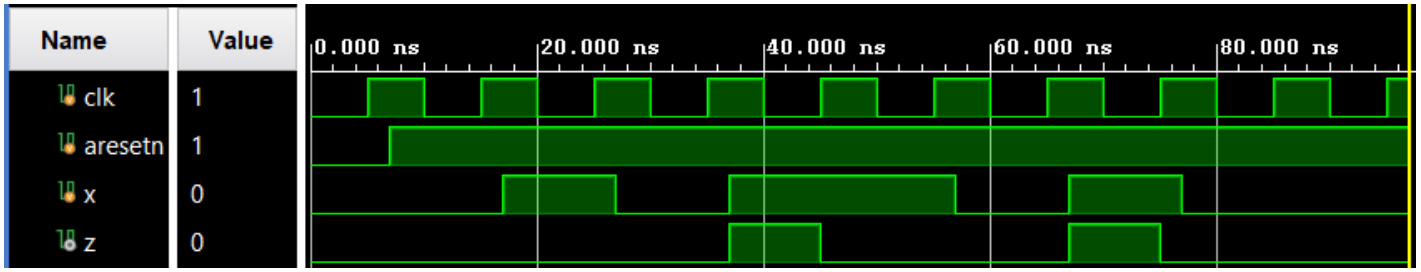
VERILOG CODE:--

```
module top_module (
    input clk,
    input aresetn,
    input x,
    output z );

    parameter S0=2'b00, S1=2'b01, S2=2'b10;
    reg [1:0] state, next_state;

    always @(*) begin
        case (state)
            S0: next_state = x ? S1:S0;
            S1: next_state = x ? S1:S2;
            S2: next_state = x ? S1:S0;
            default: next_state = S0;
        endcase
    end

    always @(posedge clk, negedge aresetn) begin
        state <= (aresetn==0) ? S0:next_state ;
    end

    assign z = (state==S2 && x==1);

endmodule
```

TESTBENCH CODE:---

```
module tb_top_module;

    reg clk;
    reg aresetn;
    reg x;

    wire z;

    top_module uut (
        .clk(clk),
        .aresetn(aresetn),
        .x(x),
        .z(z)
    );

    always #5 clk = ~clk;

    initial begin
        clk = 0;
        aresetn = 0;
        x = 0;

        #7 aresetn = 1;



        #10 x = 1;
        #10 x = 0;
        #10 x = 1;
        #10 x = 1;
        #10 x = 0;
        #10 x = 1;
        #10 x = 0;
```

WAVEFORM:-----



SCHEMATIC BLOCK :-------