

DAY-69

#100DAYSOFRTL

AIM:--- IMPLEMENTATION OF 4-BIT UP COUNTER.

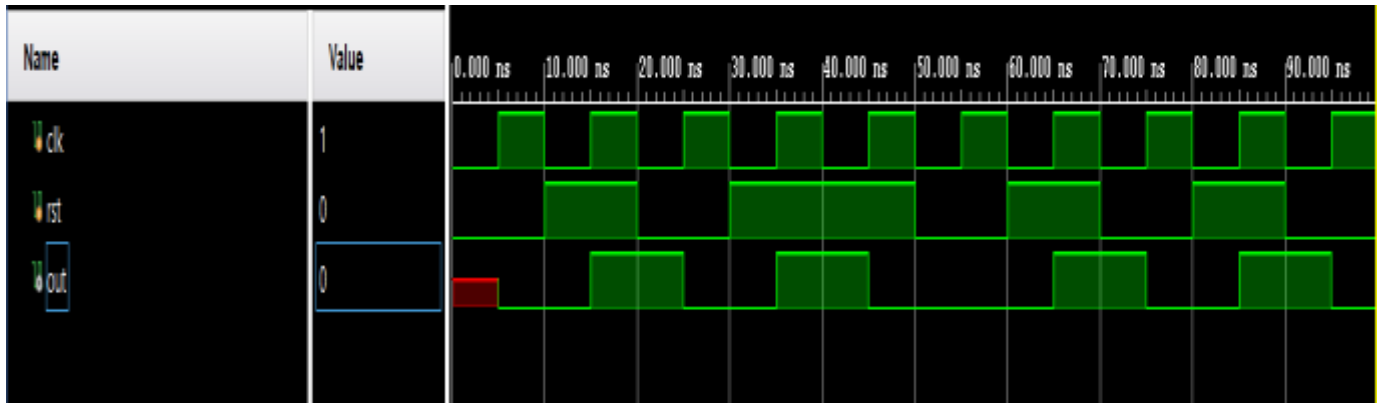
VERILOG CODE:--

```
1 module fourbitup(clk,rst,out);
2 input clk,rst;
3 output reg [3:0] out;
4
5 always@(posedge clk)
6 begin
7
8 if(rst==0)
9 out<=0;
10
11 else
12 out<=out+1;
13
14 end
15 endmodule
16
```

TESTBENCH CODE:---

```
1 module fourbitup_tb();
2   reg clk,rst;
3   wire out;
4
5   fourbitup dut (clk,rst,out);
6
7   always #5 clk=~clk;
8
9   initial
10  begin
11    clk=0;rst=0;
12
13
14
15    #10 rst=1;
16    #10 rst=0;
17    #10 rst=1;
18    #10 rst=1;
19    #10 rst=0;
20    #10 rst=1;
21    #10 rst=0;
22    #10 rst=1;
23    #10 rst=0;
24    #10 rst=1;
25
26    $finish ;
27
28
29
30  end
31 endmodule
32
```

WAVEFORM:-----



SCHEMATIC :-----

