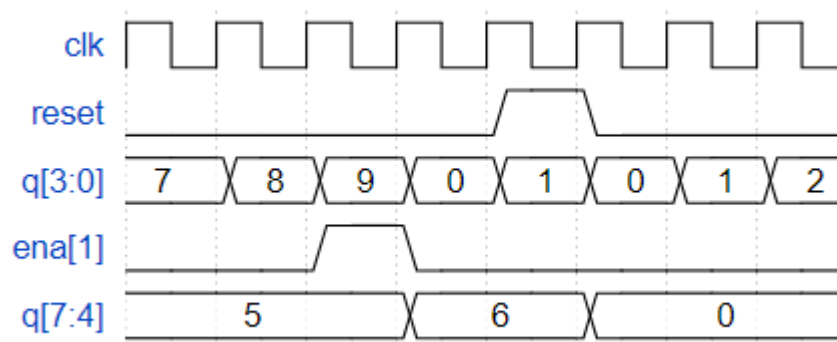


DAY-68

#100DAYSOFRTL

PROBLEM STATEMENT:--

1. Build a 4-digit BCD (binary-coded decimal) counter. Each decimal digit is encoded using 4 bits: $q[3:0]$ is the ones digit, $q[7:4]$ is the tens digit, etc. For digits [3:1], also output an enable signal indicating when each of the upper three digits should be incremented.



```

1 module top_module (
2     input clk,
3     input reset,    // Synchronous active-high reset
4     output [3:1] ena,
5     output [15:0] q):
6     always @(posedge clk) begin
7         if(reset) begin
8             q = 0;
9             ena = 0;
10        end
11        else begin
12            q[3:0] = q[3:0] + 1;
13            ena[1] = (q[3:0] == 9) ? 1 : 0;
14            if(q[3:0] == 10) begin
15                q[3:0] = 0;
16                q[7:4] = q[7:4] + 1;
17            end
18            ena[2] = ((q[7:4] == 9) && (q[3:0] == 9)) ? 1 : 0;
19            if(q[7:4] == 10) begin
20                q[7:4] = 0;
21                q[11:8] = q[11:8] + 1; end
22            ena[3] = ((q[11:8] == 9) && (q[7:4] == 9) && (q[3:0] == 9)) ? 1 : 0;
23            if(q[11:8] == 10) begin
24                q[11:8] = 0;
25                q[15:12] = q[15:12] + 1;
26            end
27            if(q[15:12] == 10) begin
28                q = 0;
29            end
30        end
31    end
32 endmodule

```

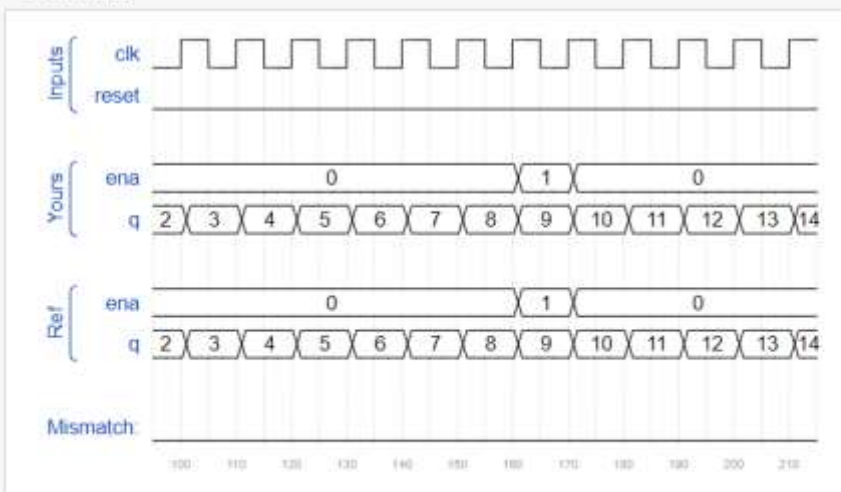
Status: Success!

You have solved 92 problems. [See my progress...](#)

Timing diagrams for selected test cases

These are timing diagrams from some of the test cases we used. They may help you debug your circuit. The diagrams show inputs to the circuit, outputs from your circuit, and the expected reference outputs. The 'Mismatch' trace shows which cycles your outputs don't match the reference outputs (0 - correct, 1 - incorrect).

Counting



100 rollover

