DAY-92
#100DAYSOFRTL

AIM:--- IMPLEMENTATION OF PRIORITY RESOLVER.

VERILOG CODE:--

```
1   module priority_resolver(gnt_a,gnt_b,gnt_c,gnt_d,req_a,req_b,req_c,req_d,clk,rst);
2
3     output reg gnt_a,gnt_b,gnt_c,gnt_d;
4     input req_a,req_b,req_c,req_d;
5     input clk,rst;
6
7     parameter idle=3'b000;
8     parameter GNTa=3'b001;
9     parameter GNTb=3'b010;
10    parameter GNTc=3'b011;
11    parameter GNTd=3'b100;
12
13    reg [2:0]  p_s,n_s;
14
15
16    always @ (posedge clk)...
23
24
25    always @ (p_s,req_a,req_b,req_c,req_d)
26      begin...
76
77
78  always @ (p_s)
79    begin
80       if(p_s==idle)...
115   end
116 endmodule
117
```

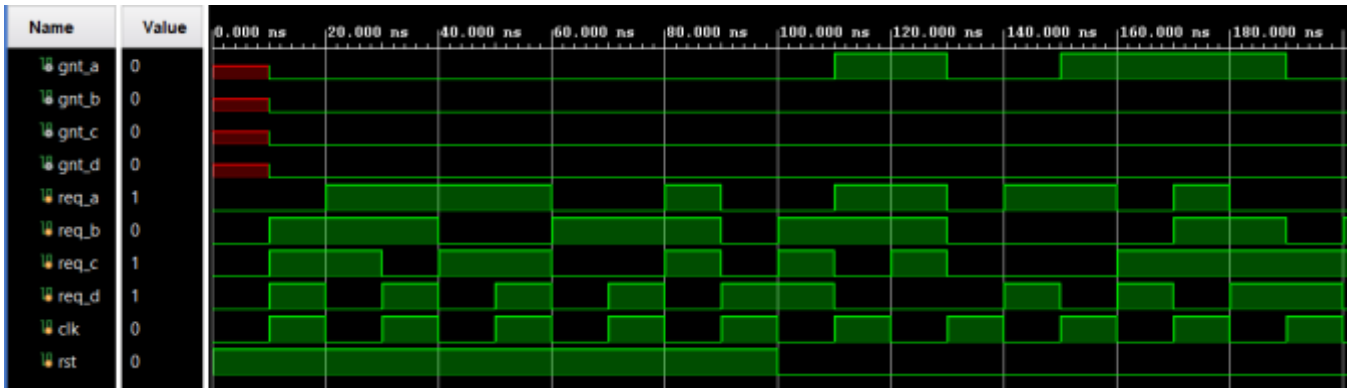
TESTBENCH CODE:---

```
module priority_resolver_tb;
   wire gnt_a,gnt_b,gnt_c,gnt_d;
   reg req_a,req_b,req_c,req_d;
   reg clk,rst;
   priority_resolver uut (gnt_a,gnt_b,gnt_c,gnt_d,req_a,req_b,req_c,req_d,clk,rst);

   initial
     begin
      rst=1'b1;
      clk=1'b0;
      req_a=1'b0;
      req_b=1'b0;
      req_c=1'b0;
      req_d=1'b0;
      #100;
      rst=1'b0;
      end

   always
     begin
      #10 clk=~clk;
      req_a=$random;
      req_b=$random;
      req_c=$random;
      req_d=$random;
      end
endmodule
```

WAVEFORM:-----



SCHEMATIC BLOCK :-------