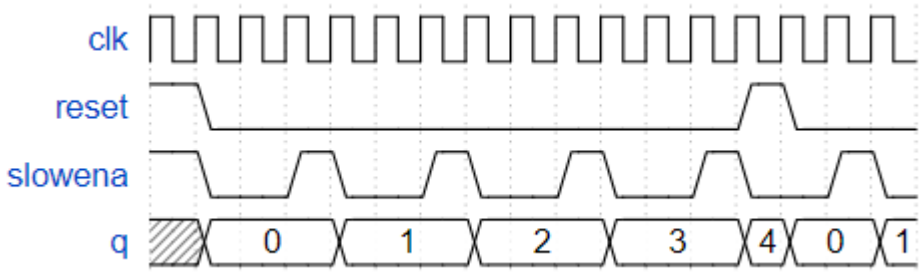
DAY-64
#100DAYSOFRTL

PROBLEM STATEMENT:--

1. Build a decade counter that counts from 0 through 9, inclusive, with a period of 10. The reset input is synchronous, and should reset the counter to 0. We want to be able to pause the counter rather than always incrementing every clock cycle, so the `slowing` input indicates when the counter should increment.



Write your solution here

[Load a previous submission] Load

```
module top_module (
    input clk,
    input slowena,
    input reset,
    output [3:0] q);

    always @ (posedge clk) begin
        if (reset) q <= 4'd0;
        else if (slowena) begin
            if (q == 4'd9) q<= 4'd0;
            else q <= q+4'd1;
        end
    end

endmodule
```

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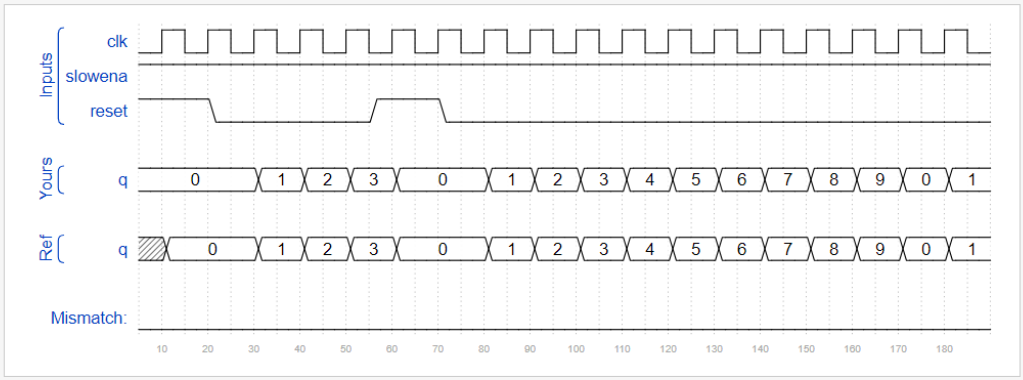
Timing diagrams for selected test cases

These are timing diagrams from some of the test cases we used. They may help you debug your circuit. The diagrams show inputs to the circuit, outputs from your circuit, and the expected reference outputs. The "Mismatch" trace shows which cycles your outputs don't match the reference outputs (0 = correct, 1 = incorrect).

Synchronous reset and counting.



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