

DAY-12

#100DAYSOFRTL

Problem statement :-

1. Create a circuit that has two 2-bit inputs $A[1:0]$ and $B[1:0]$, and produces an output z . The value of z should be 1 if $A = B$, otherwise z should be 0.

Write your solution here

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Load

```
1 module top_module ( input [1:0] A, input [1:0] B, output z );
2
3 wire t1, t2, t3, t4;
4
5 and(t1, ~A[0], ~A[1], ~B[0], ~B[1]);
6 and(t2, ~A[0], A[1], ~B[0], B[1]);
7 and(t3, A[0], ~A[1], B[0], ~B[1]);
8 and(t4, A[0], A[1], B[0], B[1]);
9 or(z, t1, t2, t3, t4);
10
11 endmodule
12
```

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mt2015_eq2 — Compile and simulate

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2. Module A is supposed to implement the function $z = (x^y) \& x$. Implement this module.

Write your solution here

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Load

```
1 module top_module (input x, input y, output z);  
2  
3     assign z=(x^y)&x;  
4  
5 endmodule  
6
```

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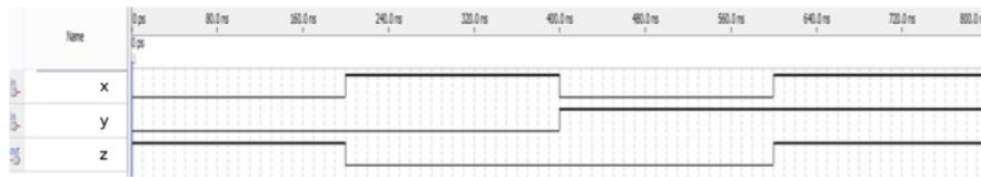
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3.

Circuit B can be described by the following simulation waveform:



Write your solution here

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Load

```
1 module top_module ( input x, input y, output z );
2
3     xnor(z, x, y);
4
5 endmodule
6
```

Submit

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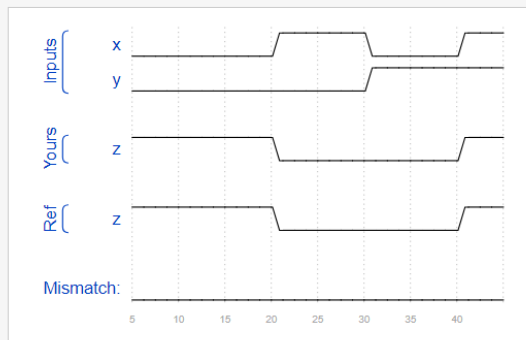
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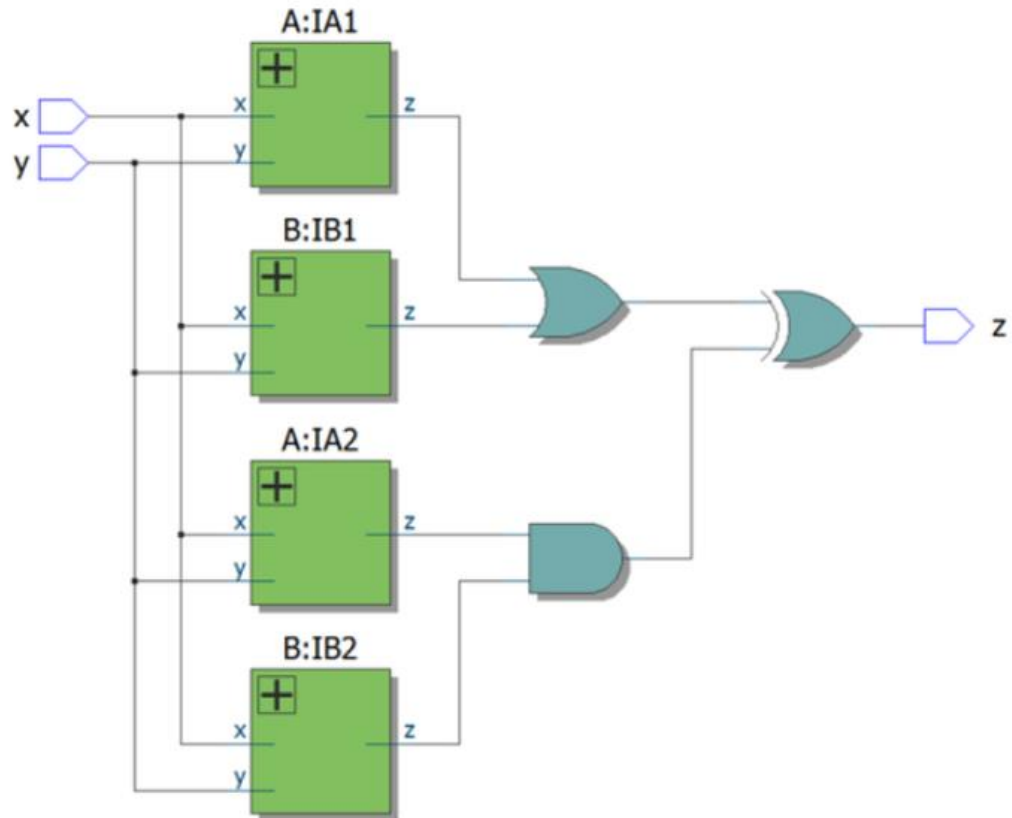
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Timing diagrams for selected test cases

These are timing diagrams from some of the test cases we used. They may help you debug your circuit. The diagrams show inputs to the circuit, outputs from your circuit, and the expected reference outputs. The "Mismatch" trace shows which cycles your outputs don't match the reference outputs (0 = correct, 1 = incorrect).



4.



Write your solution here

[Load a previous submission] Load

```

1 module top_module (input x, input y, output z);
2
3     wire t1,t2,t3,t4,t5,t6;
4     A a1(x,y,t1);
5     A a2(x,y,t2);
6     B b1(x,y,t3);
7     B b2(x,y,t4);
8     or(t5,t1,t2);
9     and(t6,t3,t4);
10    xor(z,t5,t6);
11
12 endmodule
13
14 module A (input x, input y, output z);
15
16     assign z=(x^y)&x;
17
18 endmodule
19
20
21 module B ( input x, input y, output z );
22
23     xnor(z,x,y);
24
25 endmodule
26
27

```

mt2015_q4 — Compile and simulate

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