DAY-21
#100DAYSOFRTL

PROBLEM STATEMENT:--

1. create a half adder. A half adder adds two bits (with no carry-in) and produces a sum and carry-out.

Write your solution here

Last non-success: 3/21/2024, 9:58:59 PM ▼   Load

```verilog
1  module top_module(
2      input a, b,
3      output cout, sum );
4
5    assign  sum=a^b;
6     assign cout=a&b;
7
8  endmodule
9
```

Submit   Submit (new window)

Upload a source file... ⌄

hadd — Compile and simulate

Running Quartus synthesis. Show Quartus messages...
Running ModelSim simulation. Show Modelsim messages...

Status: Success!

You have solved 55 problems. See my progress...