DAY-4
#100DAYSRTL

AIM:--IMPLEMENTATION OF FULL SUBTRACTOR IN VERILOG.

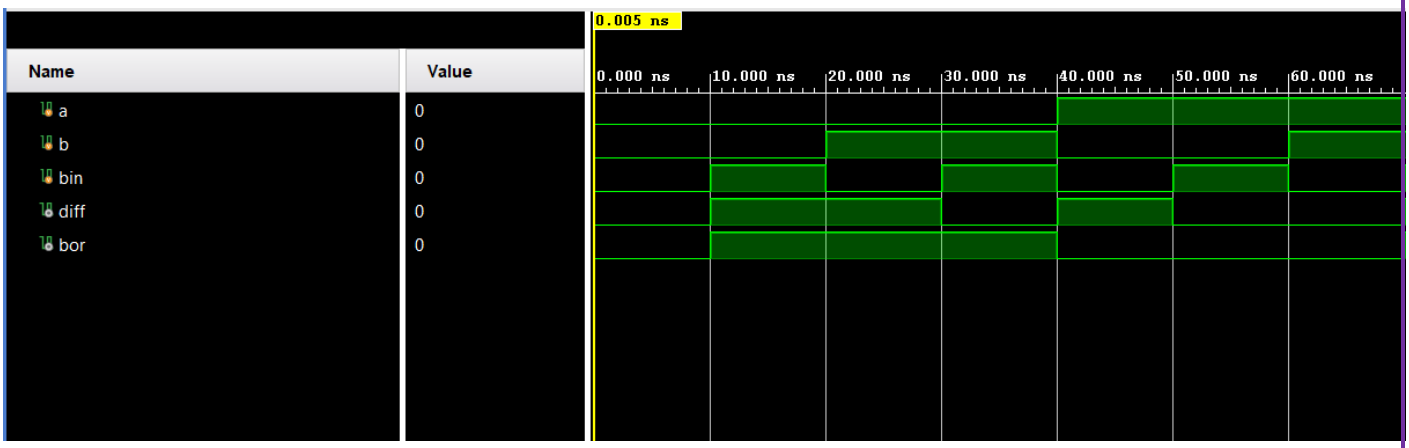
VERILOG RTL CODE:--

```
1   module full_sub(a,b,bin,diff,bor);
2
3   input a,b,bin;
4   output diff,bor;
5
6   assign diff =a^b^bin;
7   assign bor =(~a&b)|(bin&(a~^b));
8
9   endmodule
10
11
```

TESTBENCH CODE:--

```
1   module full_add_tb();
2
3   reg a,b,bin;
4   wire diff,bor;
5
6   full_sub dut (a,b,bin,diff,bor);
7
8   initial
9   begin
10
11  a=0;b=0;bin=0;#10;
12  a=0;b=0;bin=1; #10;
13  a=0;b=1;bin=0; #10;
14  a=0;b=1;bin=1; #10;
15  a=1;b=0;bin=0; #10;
16  a=1;b=0;bin=1; #10;
17  a=1;b=1;bin=0; #10;
18  a=1;b=1;bin=1; #10;
19
20  end
21
22  endmodule
23
```

WAVEFORM:--



SCHEMATIC:--