DAY-6
#100DAYSRTL

AIM:--IMPLEMENTATION OF 1-BIT COMPARATOR IN VERILOG.

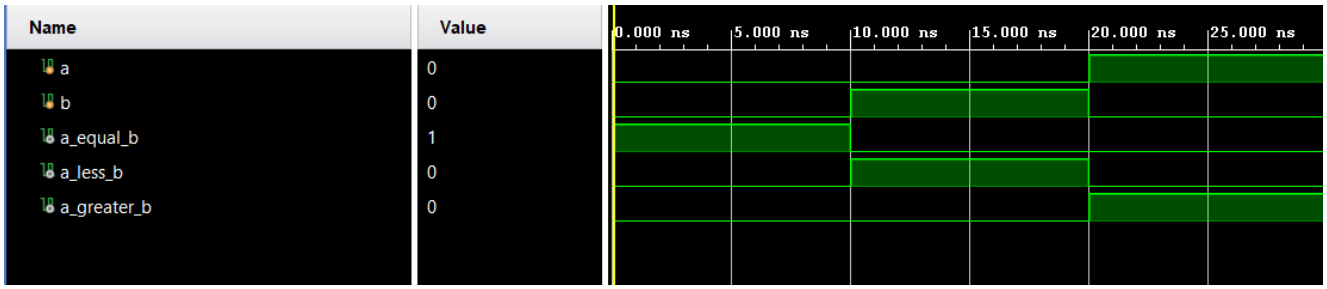
VERILOG RTL CODE:--

```
1   module com (a,b,a_equal_b,a_less_b,a_greater_b);
2
3   input a,b;
4   output a_equal_b,a_less_b,a_greater_b;
5
6   assign a_equal_b =(a == b);
7   assign a_less_b = ( a<b );
8   assign a_greater_b =(a>b);
9
10  endmodule
11
```

TESTBENCH CODE:--

```
1   module com_tb();
2
3   reg a,b;
4   wire a_equal_b,a_less_b,a_greater_b;
5
6   com dut(a,b,a_equal_b,a_less_b,a_greater_b);
7   initial begin
8
9   a=0;b=0;
10
11  #10
12  a=0;b=1;
13
14  #10
15  a=1;b=0;
16
17  #10
18  a=1;b=1;
19
20  end
21
22
23  endmodule
24
```

WAVEFORM:--



SCHEMATIC:--