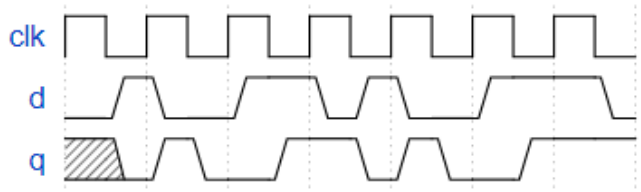
DAY-53
#100DAYSOFRTL

PROBLEM STATEMENT:--

1. You're familiar with flip-flops that are triggered on the positive edge of the clock, or negative edge of the clock. A dual-edge triggered flip-flop is triggered on both edges of the clock. However, FPGAs don't have dual-edge triggered flip-flops, and `always @(posedge clk or negedge clk)` is not accepted as a legal sensitivity list.

Build a circuit that functionally behaves like a dual-edge triggered flip-flop:



Write your solution here

[Load a previous submission] Load

```
module top_module (
    input clk,
    input d,
    output q
);
    reg q1,q2;
    always @ (posedge clk) begin
        q1 <= q2^d;
    end

    always @ (negedge clk) begin
        q2 <= q1^d;
    end

    assign q = q1^q2;
endmodule
```

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Timing diagrams for selected test cases

These are timing diagrams from some of the test cases we used. They may help you debug your circuit. The diagrams show inputs to the circuit, outputs from your circuit, and the expected reference outputs. The "Mismatch" trace shows which cycles your outputs don't match the reference outputs (0 = correct, 1 = incorrect).