DAY-12
#100DAYSOFRTL

AIM:--IMPLEMENTATION OF 1:4 DEMUX.

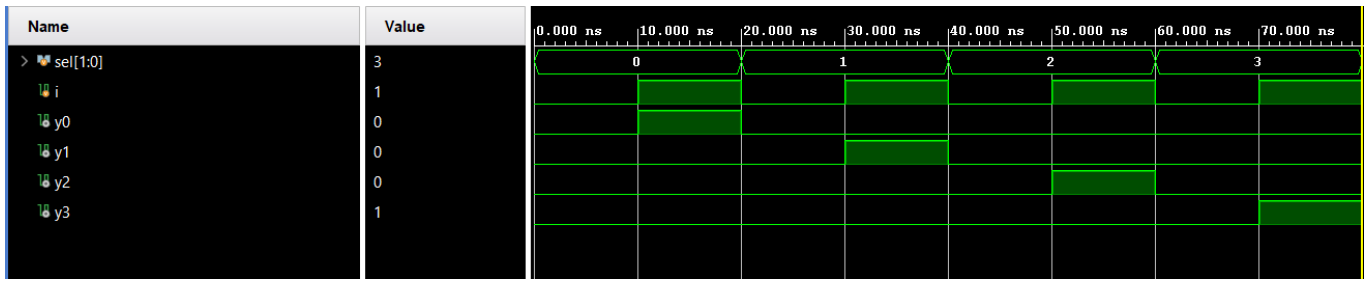
VERILOG CODE:--

```
module demux4(
  input [1:0] sel,
  input  i,
  output reg y0,y1,y2,y3);

  always @(*) begin
    case(sel)
      2'h0: {y0,y1,y2,y3} = {i,3'b0};
      2'h1: {y0,y1,y2,y3} = {1'b0,i,2'b0};
      2'h2: {y0,y1,y2,y3} = {2'b0,i,1'b0};
      2'h3: {y0,y1,y2,y3} = {3'b0,i};

    endcase
  end
endmodule
```

TESTBENCH CODE:--

```
1  module demux_tb();
2    reg [1:0] sel;
3    reg i;
4    wire y0,y1,y2,y3;
5
6    demux4 dut(sel, i, y0, y1, y2, y3);
7
8    initial begin
9
10     sel=2'b00; i=0; #10;
11     sel=2'b00; i=1; #10;
12     sel=2'b01; i=0; #10;
13     sel=2'b01; i=1; #10;
14     sel=2'b10; i=0; #10;
15     sel=2'b10; i=1; #10;
16     sel=2'b11; i=0; #10;
17     sel=2'b11; i=1; #10;
18
19     $finish;
20   end
21 endmodule
```

WAVEFORM:--



SCHEMATIC:--