DAY-14
#100DAYSOFRTL

AIM:--IMPLEMENTATION OF 8:3 ENCODER.

VERILOG CODE:--

```
module prio_enco_8x3(d_out, d_in);

   output [2:0] d_out;
   input [7:0] d_in ;

assign d_out = (d_in[7] ==1'b1 ) ? 3'b111:
               (d_in[6] ==1'b1 ) ? 3'b110:
               (d_in[5] ==1'b1 ) ? 3'b101:
               (d_in[4] ==1'b1) ? 3'b100:
               (d_in[3] ==1'b1) ? 3'b011:
               (d_in[2] ==1'b1) ? 3'b010:
               (d_in[1] ==1'b1) ? 3'b001:
               (d_in[0] ==1'b1) ? 3'b000: 3'bxxx;

endmodule
```

TESTBENCH CODE:--

```
1   module prio_enco_8x3_tst;
2      reg [7:0] d_in;
3      wire[2:0] d_out;
4
5      prio_enco_8x3 u1 (.d_out(d_out), .d_in(d_in) );
6
7      initial
8        begin
9       d_in=8'b11001100;
10      #10;
11      d_in=8'b01100110;
12      #10;
13      d_in=8'b00110011;
14      #10;
15      d_in=8'b00010010;
16      #10;
17      d_in=8'b00001001;
18      #10;
19      d_in=8'b00000100;
20      #10;
21      d_in=8'b00000011;
22      #10;
23      d_in=8'b00000001;
24      #10;
25      d_in=8'b00000000;
26      # 10;
27      $finish;
28       end //
29   endmodule
```

WAVEFORM:--

SCHEMATIC:--