DAY-8
#100DAYSOFRTL

AIM:--IMPLEMENTATION OF 4-BIT GREY TO BINARY CODE GENERATOR.

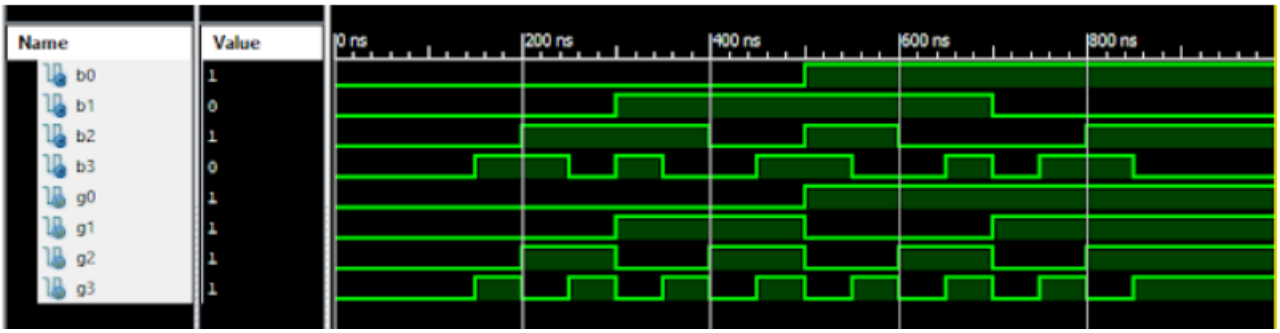
VERILOG RTL CODE:--

```
module gr_to_bin(
    input [3:0] g,
    output reg [3:0] b
);

    always @* begin
        b[0] = g[0] ^ b[1];
        b[1] = b[2] ^ g[1];
        b[2] = b[3] ^ b[2];
        b[3] = g[3];
    end

endmodule
```

TESTBENCH CODE:--

```
1  module gr_to_bin_tb;
2          wire [3:0]b;
3          reg [3:0]g;
4
5          gr_to_bin dut (b,g);
6
7          initial begin
8          g=4'b0000;
9          #10   g=4'b0001;
10         #10   g=4'b0010;
11         #10   g=4'b0011;
12         #10   g=4'b0100;
13         #10   g=4'b0101;
14         #10   g=4'b0110;
15         #10   g=4'b0111;
16         #10   g=4'b1000;
17         #10   g=4'b1001;
18         #10   g=4'b1010;
19         #10   g=4'b1011;
20         #10   g=4'b1100;
21         #10   g=4'b1101;
22         #10   g=4'b1110;
23         #10   g=4'b1111;
24         end
25 endmodule
```

WAVEFORM:--



SCHEMATIC:--