

# DAY-20

## #100DAYSOFRTL

### PROBLEM STATEMENT:--

1. Create a 1-bit wide, 256-to-1 multiplexer. The 256 inputs are all packed into a single 256-bit input vector. sel=0 should select in[0], sel=1 selects bits in[1], sel=2 selects bits in[2], etc.

#### Write your solution here

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```
1 module top_module(  
2     input [255:0] in,  
3     input [7:0] sel,  
4     output out );  
5  
6     assign out=in[sel];  
7  
8 endmodule  
9
```

Submit

Submit (new window)

Upload a source file... 

#### mux256to1 — Compile and simulate

Running Quartus synthesis. [Show Quartus messages...](#)

Running ModelSim simulation. [Show Modelsim messages...](#)

#### Status: Success!

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