DAY-25
#100DAYSOFRTL

PROBLEM STATEMENT:--

1. Assume that you have two 8-bit 2's complement numbers, a[7:0] and b[7:0]. These numbers are added to produce s[7:0]. Also compute whether a (signed) overflow has occurred.

Write your solution here

[Load a previous submission] Load

```
module top_module (
    input [7:0] a,
    input [7:0] b,
    output [7:0] s,
    output overflow
); //
 assign s = a + b;
    assign overflow = ((a[7] & b[7]) & (~s[7])) | ((~a[7] & ~b[7]) & s[7]);

endmodule

```

Status: Success!

You have solved 59 problems. See my progress...

Timing diagrams for selected test cases

These are timing diagrams from some of the test cases we used. They may help you debug your circuit. The diagrams show inputs to the circuit, outputs from your circuit, and the expected reference outputs. The "Mismatch" trace shows which cycles your outputs don't match the reference outputs (0 = correct, 1 = incorrect).