DAY-11
#100DAYSOFRTL

AIM:--- IMPLEMENTATION OF 1:2 DEMUX.

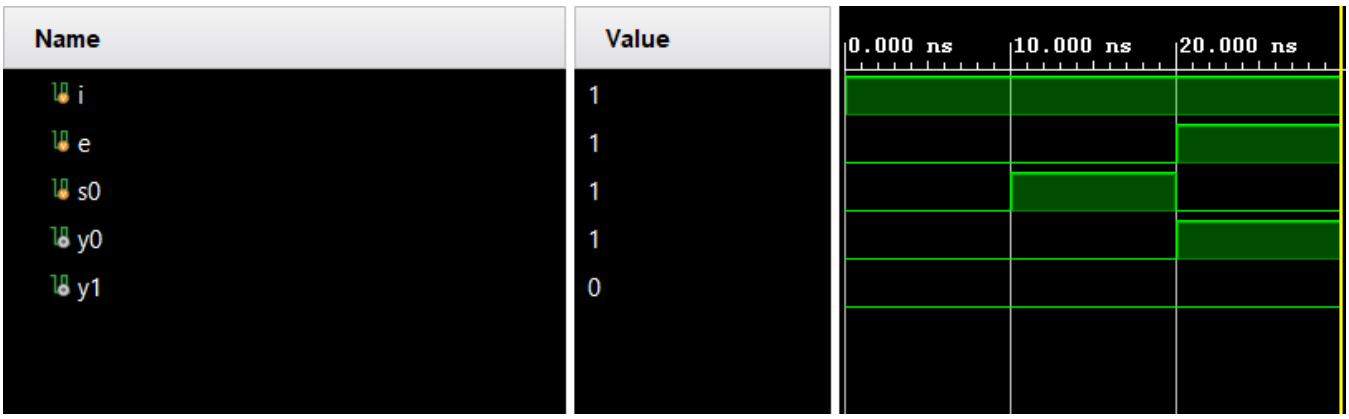
VERILOG CODE:---

```
1   module demuxtwo(i,e,s0,y0,y1);
2   input i,e,s0;
3   output y0,y1;
4
5   assign y0=e&~s0;
6   assign y1=e&s0;
7
8   endmodule
```

TESTBENCH CODE:---

```
1   module demuxtwo_tb();
2
3   reg i,e,s0;
4   wire y0,y1;
5
6   demuxtwo dut(i,e,s0,y0,y1);
7   initial begin
8
9   e=0;s0=0;i=1;
10
11  #10
12  e=0;s0=1;i=1;
13
14  #10
15  e=1;s0=0;i=1;
16
17  #10
18  e=1;s0=1;i=1;
19
20  $finish;
21  end
22
23
24  endmodule
```

WAVEFORM:---



SCHEMATIC:---