DAY-60
#100DAYSOFRTL

AIM:--IMPLEMENTATION OF SR FLIP-FLOP USING D FLIP-FLOP.

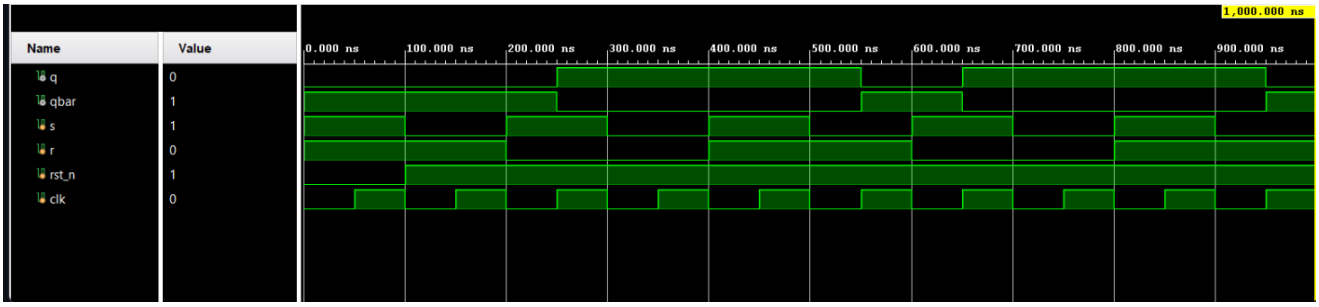
VERILOG CODE:--

```
1   module d_flipflop(input clk,d,output reg q,qbar);
2   always@(posedge clk)
3   begin
4
5   q<=d;
6   qbar<=~d;
7
8   end
9   endmodule
10
11  module d_to_sr(input clk,s,r,output q,qbar);
12  wire d;
13
14  assign d= s+(~r)&qbar;
15
16  d_flipflop dff(clk,d,q,qbar);
17  endmodule
18
```

TESTBENCH CODE:--

```
module d_to_sr_tb();
reg clk,s,r;
wire q,qbar;

srff dut (clk,s,r,q,qbar);


always #5 clk = ~clk;

initial begin
clk = 0;
s = 0;
r = 0;

    #10; s = 0; r = 1;
    #10 ;s = 0; r = 0;
    #10 ;s = 0; r = 1;
    #10 ;s = 1; r = 0;
    #10 ;s = 1; r = 1;
     $finish;


end
endmodule
```

WAVEFORM:--



SCHEMATIC:-