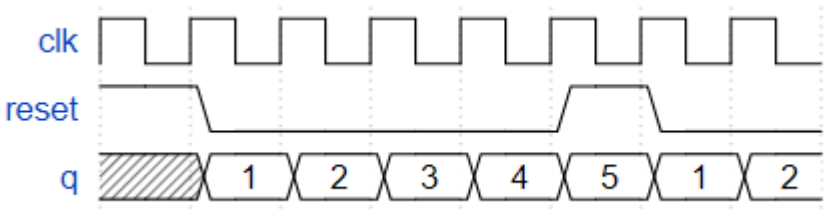
DAY-63
#100DAYSOFRTL

PROBLEM STATEMENT:--

1. Make a decade counter that counts 1 through 10, inclusive. The reset input is synchronous, and should reset the counter to 1.



Write your solution here

[Load a previous submission] Load

```
module top_module (
    input clk,
    input reset,
    output [3:0] q);

    always @ (posedge clk) begin
        if (reset) q <= 4'd1;
        else if (q == 4'd10) q<= 4'd1;
        else q <= q+4'd1;
    end

endmodule
```

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Timing diagrams for selected test cases

These are timing diagrams from some of the test cases we used. They may help you debug your circuit. The diagrams show inputs to the circuit, outputs from your circuit, and the expected reference outputs. The "Mismatch" trace shows which cycles your outputs don't match the reference outputs (0 = correct, 1 = incorrect).

Synchronous reset and counting.