DAY-82
#100DAYSOFRTL

AIM:--- IMPLEMENTATION OF SERIAL ADDER.

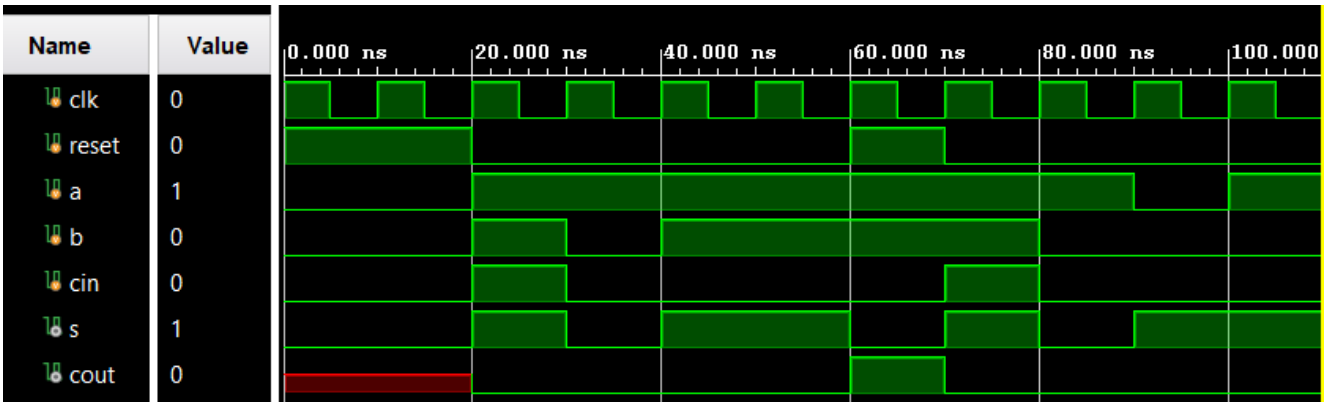
VERILOG CODE:--

```
module Serial_Adder
    (   input clk,reset,
        input a,b,cin,
        output reg s,cout
        );

reg c,flag;

always@(posedge clk or posedge reset)
begin
   if(reset == 1) begin
        s = 0;
        cout = c;
        flag = 0;
   end else begin
        if(flag == 0) begin
            c = cin;
            flag = 1;
        end
        cout = 0;
        s = a ^ b ^ c;
        c = (a & b) | (c & b) | (a & c);
   end
end

endmodule
```

TESTBENCH CODE:---

```
1   module Serial_Adder_tb();
2   ...
21          .s(s),
22          .cout(cout)
23      );
24
25  //generate clock with 10 ns clock period.
26      always
27          #5 clk = ~clk;
28
29      initial begin
30          // Initialize Inputs
31          clk = 1;
32          reset = 0;
33          a = 0;
34          b = 0;
35          cin = 0;
36          reset = 1;
37          #20;
38          reset = 0;
39
40          //add two 4 bit numbers, 1111 + 1101 = 11101
41          a = 1; b = 1; cin = 1;    #10;
42          a = 1; b = 0; cin = 0;  #10;
43          a = 1; b = 1; cin = 0;  #10;
44          a = 1; b = 1; cin = 0;  #10;
45          reset = 1;
46          #10;
47          reset = 0;
48          //add two 5 bit numbers, 11011 + 10001 = 101101
49          a = 1; b = 1; cin = 1;    #10;
50          a = 1; b = 0; cin = 0;  #10;
```

WAVEFORM:-----



SCHEMATIC BLOCK :-------