DAY-38
#100DAYSOFRTL

AIM:--IMPLEMENTATION OF JK FLIP-FLOP WITHOUT RST.

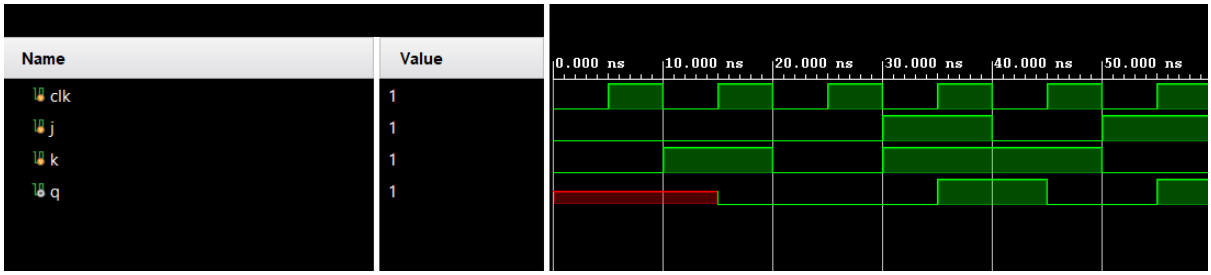
VERILOG CODE:--

```
module jkffwithoutrst( clk,j,k,q);

input clk,j,k;
output reg q;

always @(posedge clk)
begin
   case({j,k})
 2'b00:q<=q;
 2'b01:q<=0;
 2'b10:q<=1;
 2'b11:q<=~q;

 default q<=q;


endcase
end
endmodule

```

TESTBENCH CODE:--

```
1  module jkffwithoutrst_tb();
2
3      reg clk, j, k;
4      wire q;
5
6
7      jkffwithoutrst dut (clk,j,k,q);
8
9
10     always #5 clk = ~clk;
11
12
13     initial begin
14
15         clk = 0;j = 0;k = 0;
16         #10 j = 0; k = 1;
17         #10 j = 0; k = 0;
18         #10 j = 1; k = 1;
19         #10 j = 0; k = 1;
20         #10 j = 1; k = 0;
21         #10 j = 1; k = 1;
22 $finish;
23     end
24
25 endmodule
26
```

WAVEFORM:--



SCHEMATIC:--