DAY-74
#100DAYSOFRTL

AIM:--- IMPLEMENTATION OF 4-BIT SERIAL IN PARALLEL OUT (SIPO).

VERILOG CODE:--

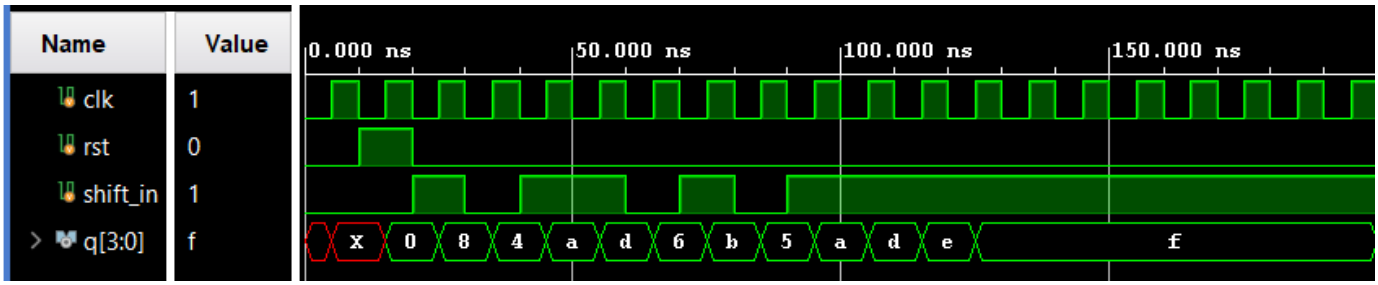
```
1   module sipo (
2       input wire clk,
3       input wire rst,
4       input wire shift_in,
5       output wire [3:0] q
6   );
7
8       reg [3:0] shift_reg;
9       always @(posedge clk) begin
10          if (rst) begin
11        shift_reg <= 4'b0000;
12          end else begin
13              shift_reg <= {shift_in, shift_reg[3:1]};
14          end
15      end
16
17      assign q = shift_reg;
18
19  endmodule
20
```

TESTBENCH CODE:---

```
module sipo_tb();

    reg clk;
    reg rst;
    reg shift_in;
 wire [3:0] q;
sipo uut (
        .clk(clk),
        .rst(rst),
        .shift_in(shift_in),
        .q(q)
    );
initial begin
        clk = 0;
        forever #5 clk = ~clk;
    end
initial begin
 rst = 0;
        shift_in = 0;
 #10;
        rst = 1;
        #10;
        rst = 0;
 shift_in = 1; #10;
        shift_in = 0; #10;
        shift_in = 1; #10;
        shift_in = 1; #10;
 shift_in = 0; #10;
        shift_in = 1; #10;
        shift_in = 0; #10;
        shift_in = 1; #10;
#100;
```

WAVEFORM:-----



SCHEMATIC BLOCK :-------