

DAY-14

#100DAYSOFRTL

AIM:--IMPLEMENTATION OF 8:3 ENCODER.

VERILOG CODE:--

```
1 module prio_enco_8x3(d_out, d_in);  
2  
3     output [2:0] d_out;  
4     input [7:0] d_in ;  
5  
6     assign d_out = (d_in[7] ==1'b1 ) ? 3'b111:  
7                     (d_in[6] ==1'b1 ) ? 3'b110:  
8                     (d_in[5] ==1'b1 ) ? 3'b101:  
9                     (d_in[4] ==1'b1) ? 3'b100:  
10                    (d_in[3] ==1'b1) ? 3'b011:  
11                    (d_in[2] ==1'b1) ? 3'b010:  
12                    (d_in[1] ==1'b1) ? 3'b001:  
13                    (d_in[0] ==1'b1) ? 3'b000: 3'bxxx;  
14  
15 endmodule  
16
```

TESTBENCH CODE:--

```
1  module prio_enco_8x3_tst;
2      reg [7:0] d_in;
3      wire[2:0] d_out;
4
5      prio_enco_8x3 u1 (.d_out(d_out), .d_in(d_in) );
6
7      initial
8      begin
9          d_in=8'b11001100;
10         #10;
11         d_in=8'b01100110;
12         #10;
13         d_in=8'b00110011;
14         #10;
15         d_in=8'b00010010;
16         #10;
17         d_in=8'b00001001;
18         #10;
19         d_in=8'b00000100;
20         #10;
21         d_in=8'b00000011;
22         #10;
23         d_in=8'b00000001;
24         #10;
25         d_in=8'b00000000;
26         # 10;
27         $finish;
28     end //
29 endmodule
```

WAVEFORM:--

Name	Value	0.000 ns	10.000 ns	20.000 ns	30.000 ns	40.000 ns	50.000 ns	60.000 ns	70.000 ns	80.000 ns
> d_in[7:0]	00	cc	66	33	12	09	04	03	01	00
> d_out[2:0]	X	7	6	5	4	3	2	1	0	x

SCHEMATIC:--

