DAY-88
#100DAYSOFRTL

AIM:--- IMPLEMENTATION OF VEDIC MULTIPLIER.

VERILOG CODE:--

```
1   `timescale 1ns / 1ps
2
3   module half_adder(
4       input a,b,
5       output sum,carry
6       );
7       assign sum=a^b;
8       assign carry=a&b;
9   endmodule
10
11  module vedic_mul_2_2(
12      input [1:0] a,b,
13      output [3:0] out
14      );
15
16      wire [3:0] w;
17
18      and m1(out[0],a[0],b[0]);
19      and m2(w[0],a[0],b[1]);
20      and m3(w[1],a[1],b[0]);
21      and m4(w[2],a[1],b[1]);
22
23      half_adder ha1(w[0],w[1],out[1],w[3]);
24      half_adder ha2(w[3],w[2],out[2],out[3]);
25
26  endmodule
```

TESTBENCH CODE:---

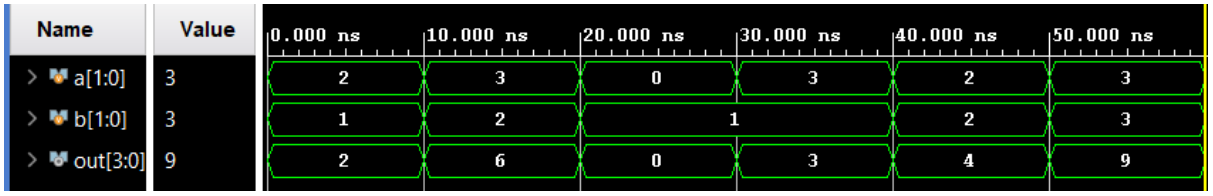
```
module test_bench;
reg [1:0]a,b;
wire [3:0]out;

vedic_mul_2_2 dut(a,b,out);

always begin
    a=2'd2;
    b=2'd1;
    #10;
    a=2'd3;
    b=2'd2;
    #10;
    a=2'd0;
    b=2'd1;
    #10;
    a=2'd3;
    b=2'd1;
    #10;
    a=2'd2;
    b=2'd2;
    #10;
    a=2'd3;
    b=2'd3;
    #10;
    end

initial begin
$monitor("%d * %d = %d", a,b,out);
#60 $finish;
end
endmodule
```

WAVEFORM:-----



SCHEMATIC BLOCK :-------