DAY-56
#100DAYSOFRTL

AIM:--IMPLEMENTATION OF T FLIP-FLOP USING SR FLIP-FLOP.

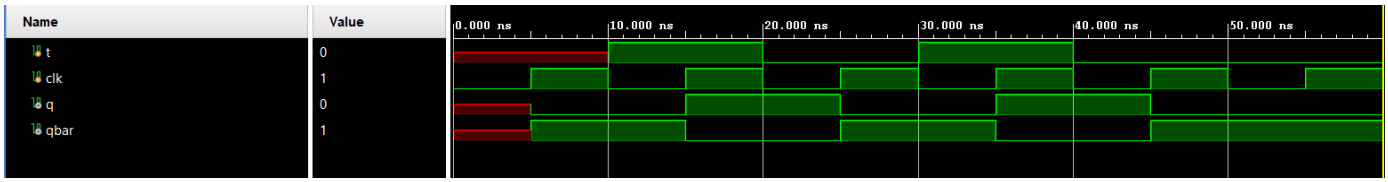
VERILOG CODE:--

```
module sr_To_d(input clk,s,r,output reg q, qbar);
always @(posedge clk) begin
    case ({s, r})
        2'b00: begin
            q <= q;
            qbar <= qbar;end
        2'b01: begin
            q <= 1'b0;
            qbar <= 1'b1;end
        2'b10: begin
            q <= 1'b1;
            qbar <= 1'b0;end
        2'b11: begin
            q <= 1'b0;
            qbar <= 1'b1;end
    endcase
end
endmodule
module srflipflop(
    input clk,
    input d,
    output reg qn,
    output reg qnbar);
wire s = d;
wire r = ~d;

sr_To_d dut (clk, s, r, qn, qnbar);

endmodule
```

TESTBENCH CODE:--

```
module sr_to_t_tb();
 reg t,clk;
  wire q, qbar;

    sr_to_t dut (clk,t,q,qbar);
    initial
    clk = 0;
    always #5 clk = ~clk;


    initial begin

#10 t=1;
#10 t=0;
#10 t=1;
#10 t=0;


        #20;

$finish;
end
endmodule
```

WAVEFORM:--



SCHEMATIC:-