DAY-16
#100DAYSOFRTL

AIM:--IMPLEMENTATION OF 3:8 DECODER

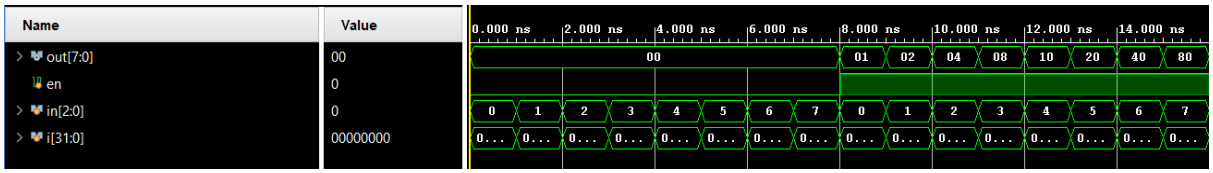
VERILOG CODE:--

```
module decoder3_to_8( in,out, en);
input [2:0]  in;
input en;
output [7:0] out;
  reg [7:0] out;

 always @( in or en)
    begin

      if (en)
        begin
          out=8'd0;
          case (in)
               3'b000: out[0]=1'b1;
               3'b001: out[1]=1'b1;
               3'b010: out[2]=1'b1;
               3'b011: out[3]=1'b1;
               3'b100: out[4]=1'b1;
               3'b101: out[5]=1'b1;
               3'b110: out[6]=1'b1;
               3'b111: out[7]=1'b1;
               default: out=8'd0;
          endcase
      end
else
out=8'd0;
end
endmodule
```

TESTBENCH CODE:--

```
1   module decoder_tb;
2   wire [7:0] out;
3   reg en;
4   reg [2:0] in;
5   integer i;
6
7   decoder3_to_8 dut(in,out,en);
8
9   initial begin
10   $monitor( "en=%b, in=%d, out=%b ", en, in, out);
11     for ( i=0; i<16; i=i+1)
12          begin
13             {en,in}   = i;
14              #1;
15          end
16          $finish;
17  end
18  endmodule
```

WAVEFORM:--



SCHEMATIC:--