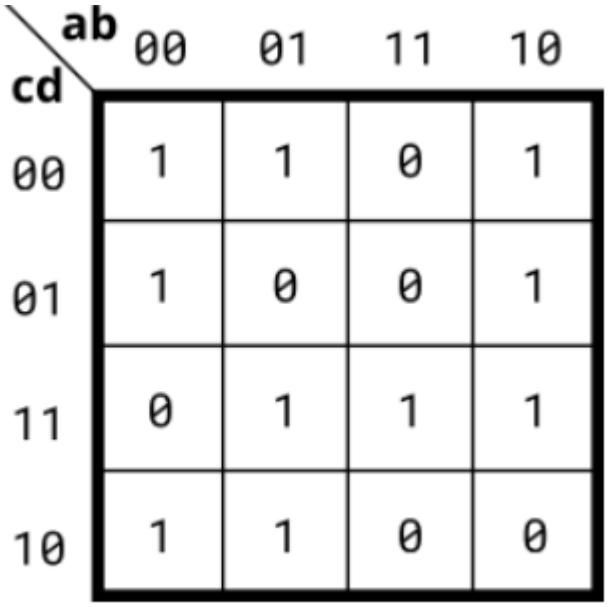
DAY-29
#100DAYSOFRTL

PROBLEM STATEMENT:--

1. Implement the circuit described by the Karnaugh map below.



cd \ ab	00	01	11	10
00	1	1	0	1
01	1	0	0	1
11	0	1	1	1
10	1	1	0	0

Write your solution here

[Load a previous submission] Load

```
module top_module(
    input a,
    input b,
    input c,
    input d,
    output out  );

assign out = (c|!d|!b) & (!a|!b|c) & (a|b|!c|!d) & (!a|!c|d);

endmodule

```

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Timing diagrams for selected test cases

These are timing diagrams from some of the test cases we used. They may help you debug your circuit. The diagrams show inputs to the circuit, outputs from your circuit, and the expected reference outputs. The "Mismatch" trace shows which cycles your outputs don't match the reference outputs (0 = correct, 1 = incorrect).