DAY-86
#100DAYSOFRTL

AIM:--- IMPLEMENTATION OF PSUEDO BIT RANDOM SEQUENCE GENERATOR.

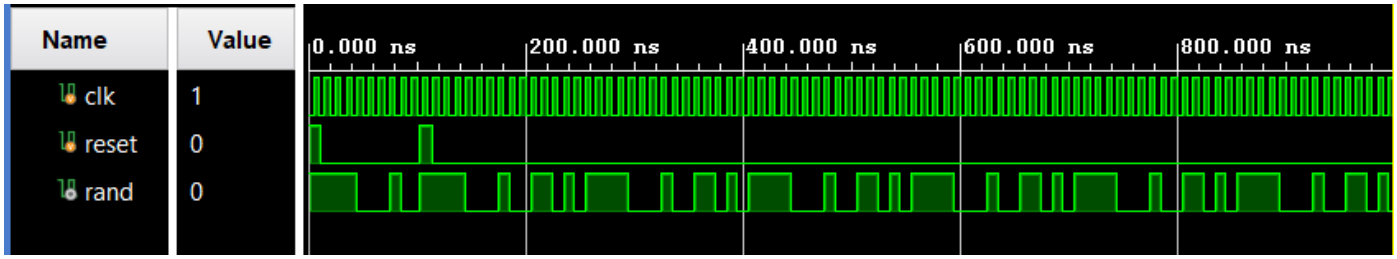
VERILOG CODE:--

```
1  module prbs_gen (rand, clk, reset);
2
3  input clk, reset;
4
5  output rand;
6  wire rand;
7  reg [3:0] temp;
8  always @ (posedge reset)
9   begin
10  temp <= 4'hf;
11 end
12 always @ (posedge clk) begin
13  if (~reset) begin
14  temp <= {temp[0]^temp[1],temp[3],temp[2],temp[1]};
15  end
16 end
17 assign rand = temp[0];
18 endmodule
```

TESTBENCH CODE:---

```
1  module prbs_gen_tb();
2  reg clk, reset;
3  wire rand;
4  prbs_gen pr (rand, clk, reset);
5  initial begin
6   forever begin
7   clk <= 0;
8   #5
9   clk <= 1;
10  #5
11  clk <= 0;
12  end
13 end
14 initial begin
15  reset = 1;
16  #12
17  reset = 0;
18  #90
19  reset = 1;
20  #12
21  reset = 0;
22 end
23 initial
24 begin
25 $monitor(" Random bit : %b | Reset=%b | Clock=%b", rand,reset,clk);
26 #1000 $finish;
27 end
28 endmodule
```

WAVEFORM:-----



SCHEMATIC BLOCK :-------