DAY-40
#100DAYSOFRTL

AIM:--IMPLEMENTATION OF D FLIP-FLOP WITHOUT RST.

VERILOG CODE:--

```
1   module dffwithoutrst(clk,d,q);
2
3   input clk,d;
4   output reg q;
5
6   always@(posedge clk)
7   begin
8
9   q<=d;
10
11  end
12  endmodule
13
```

TESTBENCH CODE:--

```
1  module dffwithoutrst_tb();
2
3      reg clk,d;
4      wire q;
5
6
7      dffwithoutrst dut (clk,d,q );
8
9      always  #5 clk = ~clk;
10
11
12     initial begin
13
14         clk = 0;d=0;
15
16         #10 d = 1;
17         #10 d = 0;
18         #10 d = 1;
19
20       $finish;
21     end
22
23 endmodule
24
```

WAVEFORM:--

SCHEMATIC:--