DAY-37
#100DAYSOFRTL

AIM:--IMPLEMENTATION OF SR FLIP-FLOP WITH SYNCHRONOUS RESET .

VERILOG CODE:--

```verilog
1    module srff(clk,rst,s,r,q);
2
3        input clk,rst,s,r;
4        output reg q;
5
6    always@(posedge clk)
7    begin
8        if (rst)
9        q<=0;
10
11       else
12       begin
13       case({s,r})
14       2'b00:q<=q;
15       2'b01:q<=0;
16       2'b10:q<=1;
17       2'b11:q<=1'bx;
18
19   endcase
20   end
21   end
22   endmodule
23
```
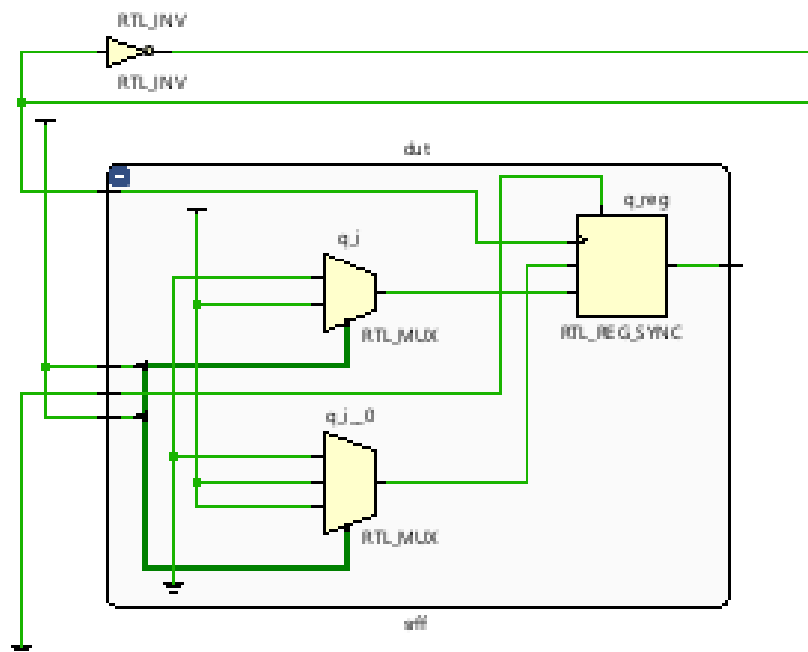
TESTBENCH CODE:--

```
1   module srff_tb();
2   reg clk,rst,s,r;
3   wire q;
4
5   srff dut (clk,rst,s,r,q);
6
7
8   always #5 clk = ~clk;
9
10  initial begin
11  clk = 0;
12  rst=1;
13  s = 0;
14  r = 0;
15
16  #10 rst = 0;
17
18      #10; s = 0; r = 1;
19      #10 ;s = 0; r = 0;
20      #10 ;s = 0; r = 1;
21      #10 ;s = 1; r = 0;
22      #10 ;s = 1; r = 1;
23          $finish;
24
25
26
27  end
28  endmodule
29
```
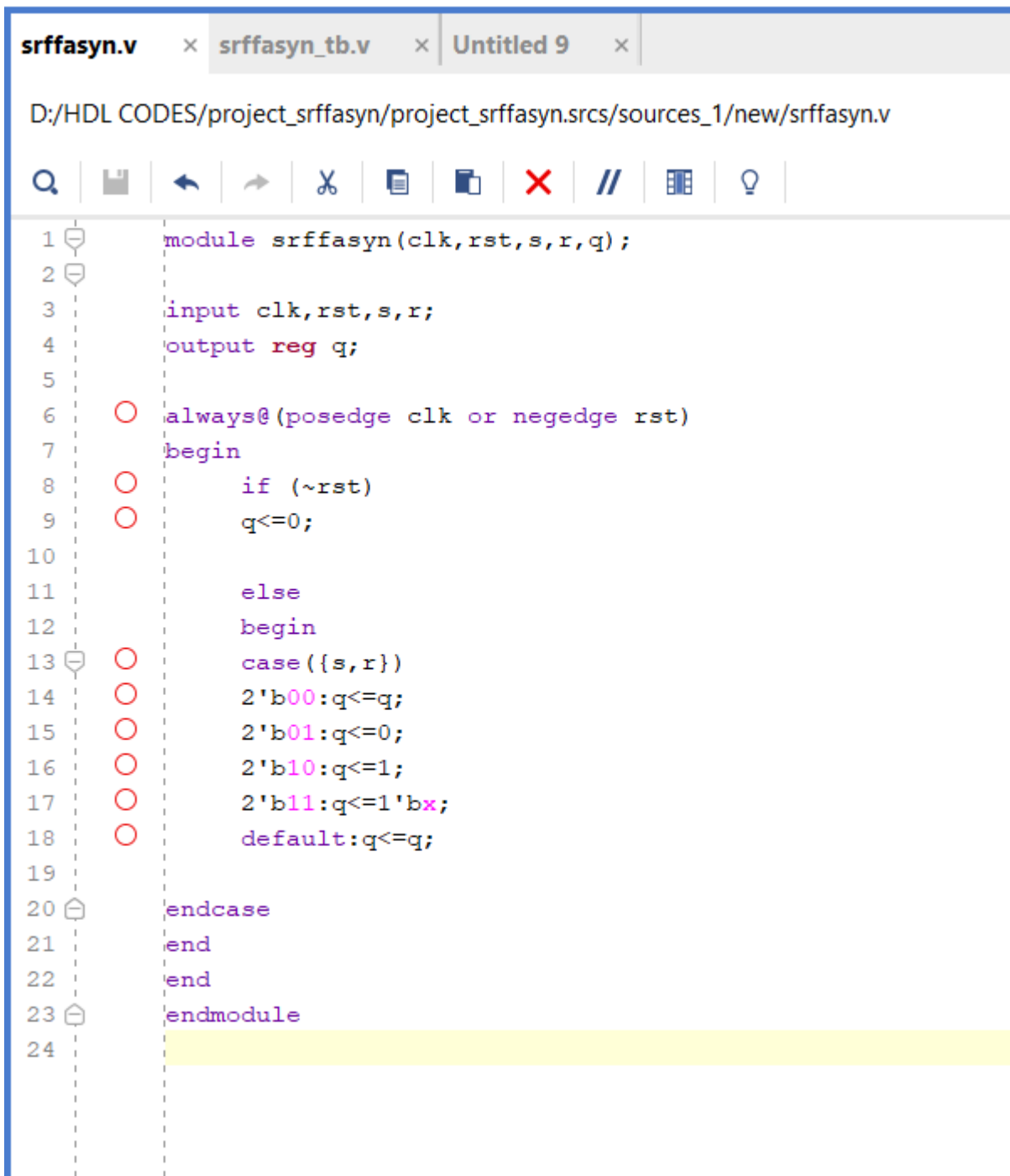
WAVEFORM:--

SCHEMATIC:--

AIM:--IMPLEMENTATION OF SR FLIP-FLOP WITH ASYNCHRONOUS RESET.
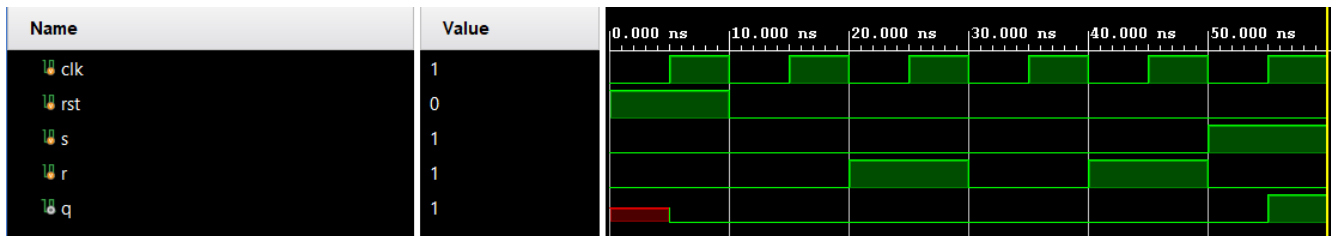
VERILOG CODE:--

```verilog
1   module srff_tb();
2   reg clk,rst,s,r;
3   wire q;
4
5   srff dut (clk,rst,s,r,q);
6
7
8   always #5 clk = ~clk;
9
10  initial begin
11  clk = 0;
12  rst=1;
13  s = 0;
14  r = 0;
15
16  #10 rst = 0;
17
18      #10; s = 0; r = 1;
19      #10 ;s = 0; r = 0;
20      #10 ;s = 0; r = 1;
21      #10 ;s = 1; r = 0;
22      #10 ;s = 1; r = 1;
23      $finish;
24
25
26
27  end
28  endmodule
29
```

TESTBENCH CODE:--

srffasyn.v × srffasyn_tb.v × Untitled 9 ×

D:/HDL CODES/project_srffasyn/project_srffasyn.srcs/sources_1/new/srffasyn.v

```verilog
1    module srffasyn(clk,rst,s,r,q);
2
3    input clk,rst,s,r;
4    output reg q;
5
6    always@(posedge clk or negedge rst)
7    begin
8        if (~rst)
9        q<=0;
10
11       else
12       begin
13       case({s,r})
14       2'b00:q<=q;
15       2'b01:q<=0;
16       2'b10:q<=1;
17       2'b11:q<=1'bx;
18       default:q<=q;
19
20   endcase
21   end
22   end
23   endmodule
24
```

WAVEFORM:--

SCHEMATIC:--