DAY-65
#100DAYSOFRTL

PROBLEM STATEMENT:--

1. Design a 1-12 counter with the following inputs and outputs:

   Reset Synchronous active-high reset that forces the counter to 1

   Enable Set high for the counter to run

   Clk Positive edge-triggered clock input

   Q[3:0] The output of the counter

   c_enable, c_load, c_d[3:0] Control signals going to the provided 4-bit counter, so correct operation can be verified.

   You have the following components available:

   the 4-bit binary counter (count4) below, which has Enable and synchronous parallel-load inputs (load has higher priority than enable). The count4 module is provided to you. Instantiate it in your circuit.

   logic gates

   ```
   module count4(
       input clk,
       input enable,
       input load,
       input [3:0] d,
       output reg [3:0] Q
   );
   ```

   The c_enable, c_load, and c_d outputs are the signals that go to the internal counter's enable, load, and d inputs, respectively. Their purpose is to allow these signals to be checked for correctness.

Write your solution here

[Load a previous submission] Load

```
module top_module (
    input clk,
    input reset,
    input enable,
    output [3:0] Q,
    output c_enable,
    output c_load,
    output [3:0] c_d
  );

      initial Q <= 1;

    always @(posedge clk) begin
        if(reset | ((Q == 12) & enable)) Q <= 1;
        else Q <= (enable) ? Q + 1 : Q;
    end

    assign c_enable = enable;
    assign c_load = (reset | ((Q == 12) & enable));
    assign c_d = c_load ? 1 : 0;

    count4 the_counter (clk, c_enable, c_load, c_d /*, ... */ );

endmodule
```

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Timing diagrams for selected test cases

These are timing diagrams from some of the test cases we used. They may help you debug your circuit. The diagrams show inputs to the circuit, outputs from your circuit, and the expected reference outputs. The "Mismatch" trace shows which cycles your outputs don't match the reference outputs (0 = correct, 1 = incorrect).