DAY-9
#100DAYSOFRTL

AIM:--IMPLEMENTATION OF 2:1 MUX .

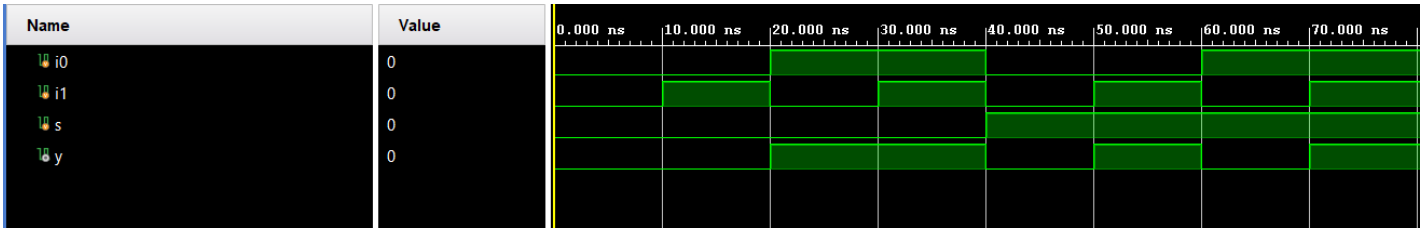
VERILOG RTL CODE:---

```
1   module mux2(s,i0,i1,y);
2   input s,i0,i1;
3   output reg y;
4
5   always@(*)
6   begin
7
8   if(s)
9   y=i1;
10
11  else
12  y=i0;
13
14
15  end
16
17  endmodule
```

TESTBENCH CODE:--

```
1   module mux2_tb;
2   reg i0,i1,s;
3   wire y;
4
5    mux2 dut (s,i0,i1,y);
6
7   initial
8    begin
9
10  s=0;i0=0;i1=0;#10;
11  s=0;i0=0;i1=1;#10;
12  s=0;i0=1;i1=0;#10;
13  s=0;i0=1;i1=1;#10;
14
15  s=1;i0=0;i1=0;#10;
16  s=1;i0=0;i1=1;#10;
17  s=1;i0=1;i1=0;#10;
18  s=1;i0=1;i1=1;#10;
19
20  end
21
22  endmodule
```

WAVEFORM:--



SCHEMATIC:--