DAY-91
#100DAYSOFRTL

AIM:--- IMPLEMENTATION OF FREQUENCY DIVIDER BY ODD NUMBER

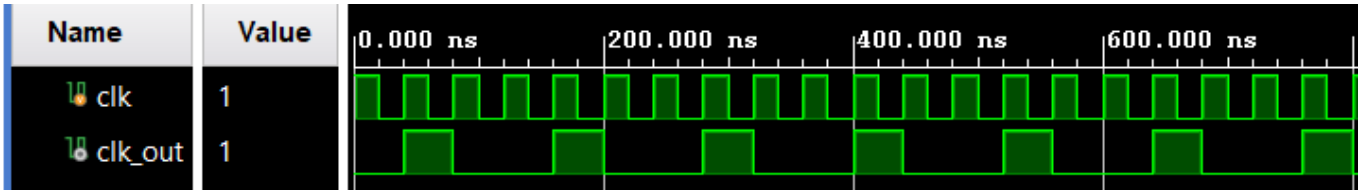
VERILOG CODE:--

```
module clk_div_by_3(
    input clk,
    output clk_out
);

    reg [1:0] state;

    always @(posedge clk) begin
        case(state)
            2'b00: state <= 2'b01;
            2'b01: state <= 2'b10;
            2'b10: state <= 2'b00;
            default: state <= 2'b00;
        endcase
    end

    assign clk_out = (state == 2'b01);

endmodule
```

TESTBENCH CODE:---

```
1  module clk_div_by_3_tb;
2
3      reg clk;
4      wire clk_out;
5
6      clk_div_by_3 dut(
7          .clk(clk),
8          .clk_out(clk_out)
9      );
10
11
12     initial begin
13         clk = 0;
14     end
15
16     always begin
17         clk = ~clk;
18         #20;
19     end
20
21 endmodule
```

WAVEFORM:-----



SCHEMATIC BLOCK :-------