DAY-10
#100DAYSRTL

AIM:--IMPLEMENTATION OF 4:1 MUX .

VERILOG CODE:--

4mux.v * | 4mux_tb.v | Untitled 5

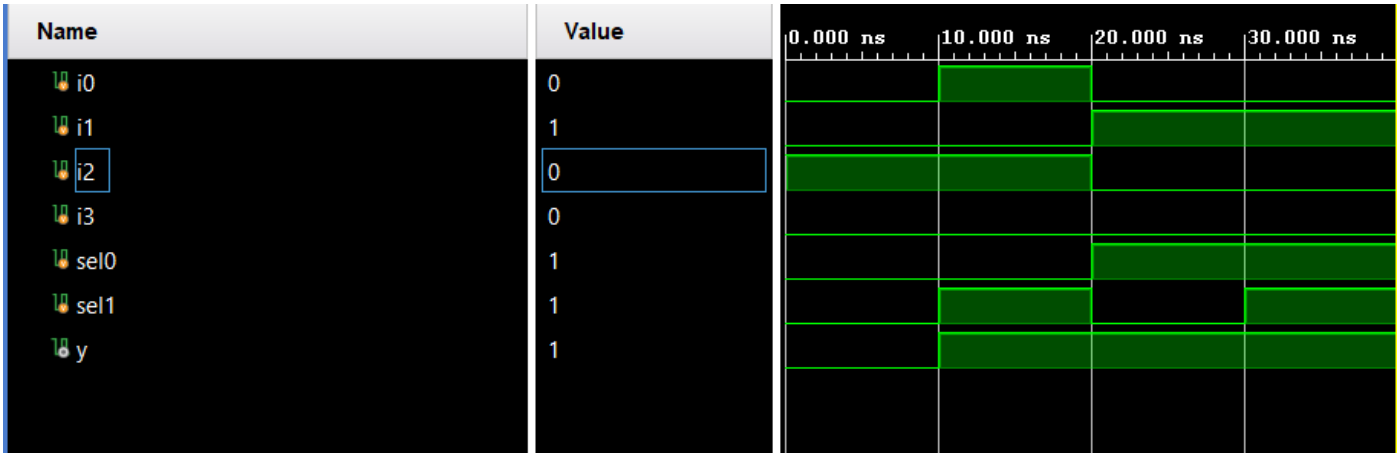
D:/HDL CODES/project_4mux/project_4mux.srcs/sources_1/new/4mux.v

```
1  module mux(    input i0, i1, i2, i3,
2      input sel0, sel1,
3      output reg y
4  );
5
6  always @(*) begin
7      case({sel0, sel1})
8          2'b00: y = i0;
9          2'b01: y = i1;
10         2'b10: y = i2;
11         2'b11: y = i3;
12         default: y = 1'b0;
13     endcase
14 end
15
16 endmodule
17
```

TESTBENCH CODE:--

```
1   module mux_tb;
2
3   reg i0, i1, i2, i3;
4   reg sel0, sel1;
5   wire y;
6
7   mux dut( sel0, sel1,i0, i1, i2, i3, y);
8   initial
9   begin
10      sel0 = 1'b0; sel1 = 1'b0; i0 = 4'b0000; i1 = 4'b0000; i2 = 4'b1001; i3 = 4'b0110; #10;
11      sel0 = 1'b0; sel1 = 1'b1; i0 = 4'b1001; i1 = 4'b0100; i2 = 4'b0001; i3 = 4'b0010; #10;
12      sel0 = 1'b1; sel1 = 1'b0; i0 = 4'b0010; i1 = 4'b1001; i2 = 4'b0010; i3 = 4'b1000; #10;
13      sel0 = 1'b1; sel1 = 1'b1; i1 = 4'b1010; i1 = 4'b1101; i2 = 4'b1010; i3 = 4'b0110; #10;
14
15      $finish;
16  end
17
18  endmodule
19
```

WAVEFORM:--



SCHEMATIC:--