DAY-78
#100DAYSOFRTL

AIM:--- IMPLEMENTATION OF BIDIRECTIONAL SHIFT REGISTER .

VERILOG CODE:--

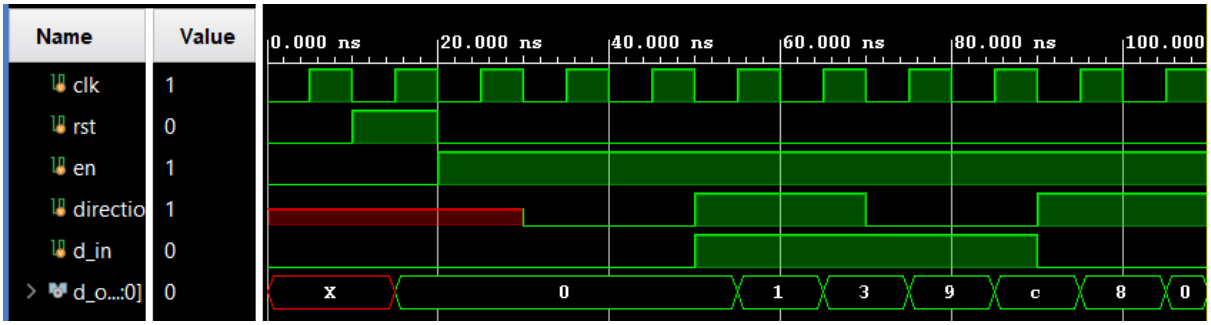
```
module bidirectional_reg(input clk,rst,en,direction,d_in, output reg[3:0]d_out);

 always@(posedge clk)
  begin
   if(rst)
    d_out <= 0;
   else
    if(en)
     begin
      case(direction)
       0 : d_out <= {d_in,d_out[3:1]};
       1 : d_out <= {d_out[2:0],d_in};
       default d_out <= d_out;
      endcase
     end
     else
       d_out <= d_out;
    end
 endmodule
```

TESTBENCH CODE:---

```
1   module bidirectional_shift_reg_tb();
2     reg clk,rst,en,direction,d_in;
3     wire [3:0]d_out;
4
5    ///Instantiation
6     bidirectional_reg BSR(clk,rst,en,direction,d_in,d_out);
7
8    ///clock Initialization
9    initial...
15
16   ///Initialization
17    task initialize();...
20
21    ////reset
22   task reset();
23    begin
24      @(negedge clk)
25      rst = 1'b1;
26      @(negedge clk)
27      rst = 1'b0;
28    end
29    endtask
30
31   ////stimulus generation
32   initial
33    begin...
56   initial #110 $finish;
57   endmodule
58
```

WAVEFORM:-----



SCHEMATIC BLOCK :-------