DAY-13
#100DAYSOFRTL

AIM:--IMPLEMENTATION OF 4:2 ENCODER.

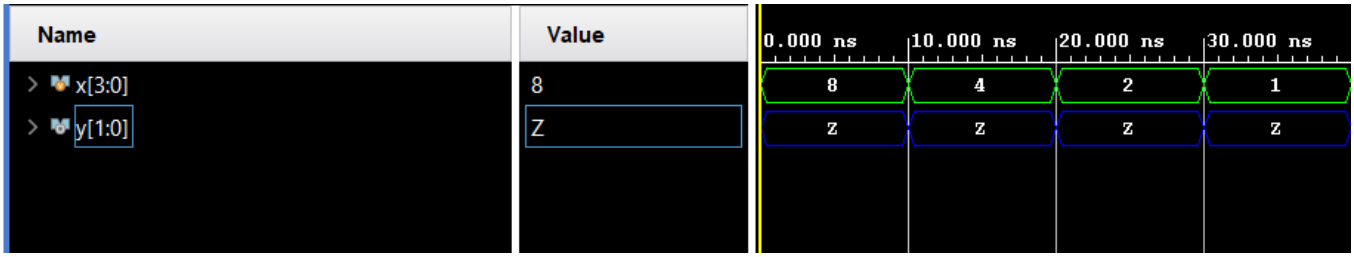
VERILOG CODE:--

```
1  module encoder4(x, y);
2      input [3:0] x;
3      output [1:0] y;
4      reg y;
5
6      always @(*)          // Continuous assignment
7      begin
8          case(x)
9              4'b1000 : y = 2'b00;
10             4'b0100 : y = 2'b01;
11             4'b0010 : y = 2'b10;
12             4'b0001 : y = 2'b11;
13             default: y = 2'b00;
14         endcase
15     end
16 endmodule
17
```

TESTBENCH CODE:--

```
1  module encoder4_tb();
2
3      reg [3:0] x;
4      wire [1:0] y;
5
6      encoder4 dut(x, y);
7
8      initial begin
9
10
11
12         x = 4'b1000; #10;
13
14         x = 4'b0100; #10;
15
16         x = 4'b0010; #10;
17
18         x = 4'b0001; #10;
19
20         $finish;
21     end
22
23 endmodule
24
```

WAVEFORM:--



SCHEMATIC:--