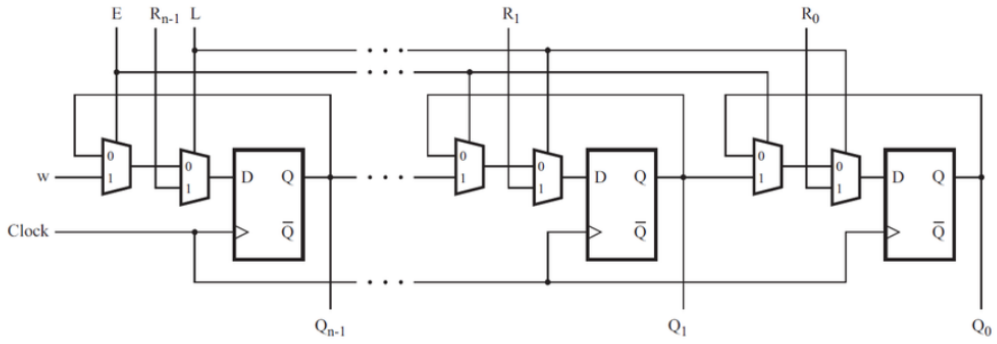
DAY-48
#100DAYSOFRTL

PROBLEM STATEMENT:--

1.

Consider the *n*-bit shift register circuit shown below:



Write a Verilog module named top_module for one stage of this circuit, including both the flip-flop and multiplexers.

Write your solution here

[Load a previous submission] Load

```
module top_module (
    input clk,
    input w, R, E, L,
    output Q
);

    always@(posedge clk)
        begin
            if(L)
                Q<=R;
            else
                begin
                    if(E)
                        Q<=w;
                    else
                        Q<=Q;

                end
        end

endmodule

```

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exams/2014_q4a — Compile and simulate

Running Quartus synthesis. Show Quartus messages...
Running ModelSim simulation. Show Modelsim messages...

Status: Success!

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