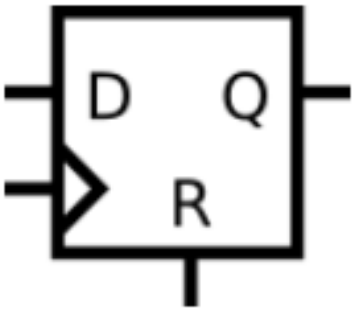
DAY-46
#100DAYSOFRTL

PROBLEM STATEMENT:--

1.

Implement the following circuit:



Write your solution here

[Load a previous submission] Load

```
module top_module (
    input clk,
    input d,
    input r,   // synchronous reset
    output q);

    always@(posedge clk)
        begin
            if(r)
                q<=0;
            else
                q<=d;

        end
endmodule
```

Submit | Submit (new window)

Upload a source file...

exams/m2014_q4c — Compile and simulate

Running Quartus synthesis. Show Quartus messages...
Running ModelSim simulation. Show Modelsim messages...

Status: Success!

You have solved 78 problems. See my progress...