DAY-69
#100DAYSOFRTL

AIM:--- IMPLEMENTATION OF 4-BIT UP COUNTER.

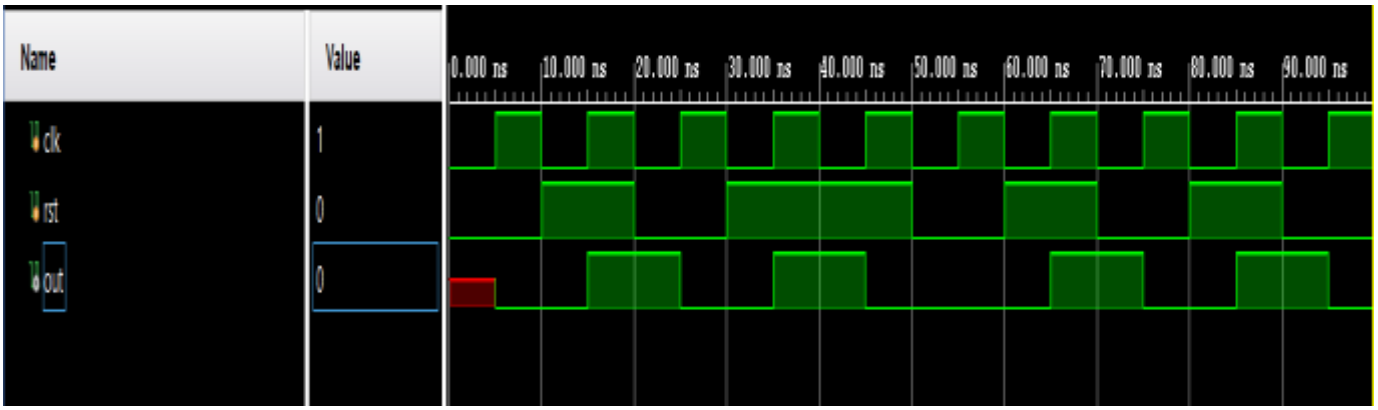
VERILOG CODE:--

```
1  module fourbitup(clk,rst,out);
2  input clk,rst;
3  output reg [3:0] out;
4
5  always@(posedge clk)
6  begin
7
8  if(rst==0)
9  out<=0;
10
11 else
12 out<=out+1;
13
14 end
15 endmodule
16
```

TESTBENCH CODE:---

```
module fourbitup_tb();
reg clk,rst;
wire out;

fourbitup dut (clk,rst,out);

always #5 clk=~clk;

initial
begin
clk=0;rst=0;



#10 rst=1;
#10 rst=0;
#10 rst=1;
#10 rst=1;
#10 rst=0;
#10 rst=1;
#10 rst=0;
#10 rst=1;
#10 rst=0;
#10 rst=1;

$finish ;



end
endmodule
```

WAVEFORM:-----



SCHEMATIC :-------