DAY-85
#100DAYSOFRTL

AIM:--- IMPLEMENTATION OF CLOCK BUFFER.

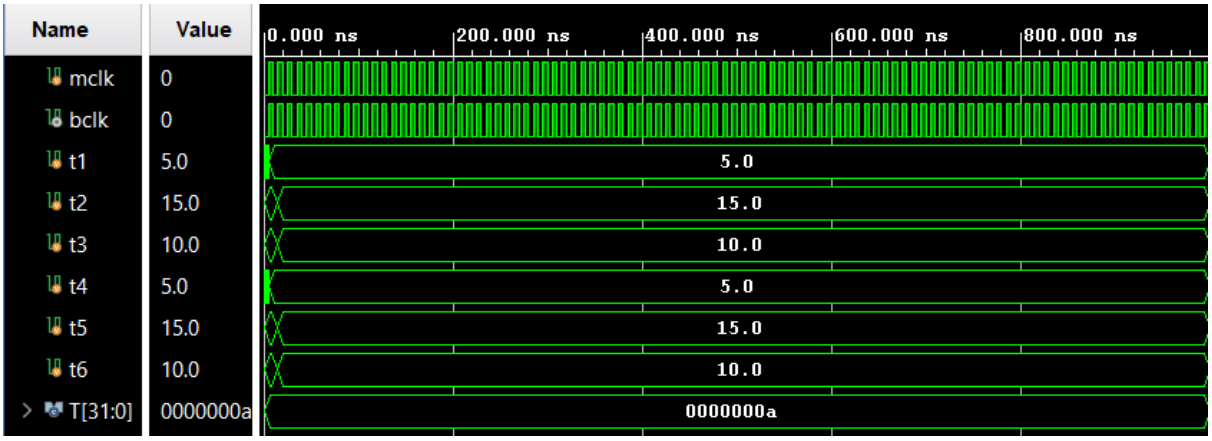
VERILOG CODE:--

```
1   module clock_buffer(mclk,bclk);
2   input mclk;
3   output bclk;
4   buf b1(bclk,mclk);
5   endmodule
```

TESTBENCH CODE:---

```
1  module clock_buffer_tb();
2  reg mclk;
3  wire bclk;
4  realtime t1,t2,t3,t4,t5,t6;
5  parameter T=10;
6  clock_buffer dut(mclk,bclk);
7  initial
8  begin
9  mclk=1'b0;
10 forever #(T/2) mclk=~mclk;
11 end
12 task master;
13 begin
14 @(posedge mclk) t1=$realtime;
15 @(posedge mclk) t2=$realtime;
16 t3=t2-t1;
17 end
18 endtask
19
20 task bufout;
21 begin
22 @(posedge bclk) t4=$realtime;
23 @(posedge bclk) t5=$realtime;
24 t6=t5-t4;
25 end
26 endtask
27
28 task freq_phase;
29 realtime f,p;
30 begin
31 f=t6-t3;
```

WAVEFORM:-----



SCHEMATIC BLOCK :-------