DAY-84
#100DAYSOFRTL

AIM:--- IMPLEMENTATION OF CLOCK DIVIDER.

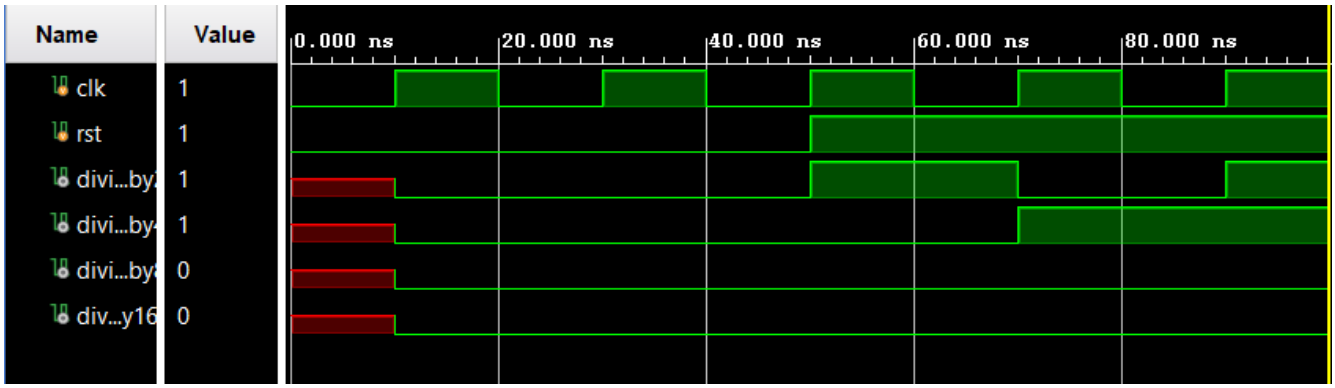
VERILOG CODE:--

```
module clockdivider(clk,divideby2,divideby4,divideby8,divideby16,rst);
input clk,rst;
reg [3:0]count;
output reg divideby2,divideby4,divideby8,divideby16;
always@(posedge clk)
begin
if(rst==0)
count=4'b0000;
else
count=count+1;
  divideby2=count[0];
  divideby4=count[1];
  divideby8=count[2];
  divideby16=count[3];
end
endmodule
```

TESTBENCH CODE:---

```
module clockdivider_tb;
reg clk;
reg rst;
wire divideby2;
wire divideby4;
wire divideby8;
wire divideby16;

    clockdivider uut (
        .clk(clk),
        .divideby2(divideby2),
        .divideby4(divideby4),
        .divideby8(divideby8),
        .divideby16(divideby16),
        .rst(rst)
    );

    initial begin

        clk = 0;
        rst = 0;
        #50 rst=1;
end
    always
    #10 clk=~clk;

    initial
    #100 $finish;

endmodule
```

WAVEFORM:-----



SCHEMATIC BLOCK :-------