DAY-15
#100DAYSOFRTL

AIM:--IMPLEMENTATION OF 2:4 DECODER

VERILOG CODE:--

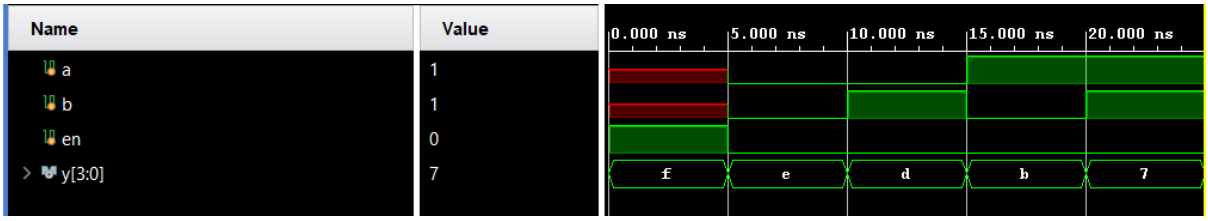
```
module decoder24_behaviour(en,a,b,y);
input en,a,b;
output reg [3:0]y;

always @(en,a,b)
     begin
       if(en==0)
         begin
           if(a==1'b0 & b==1'b0) y=4'b1110;
           else if(a==1'b0 & b==1'b1) y=4'b1101;
           else if(a==1'b1 & b==1'b0) y=4'b1011;
           else if(a==1 & b==1) y=4'b0111;
           else y=4'bxxxx;
         end
       else
        y=4'b1111;
     end
endmodule
```

TESTBENCH CODE:--

```
1  module tb;
2  reg a,b,en;
3  wire [3:0]y;
4
5
6    decoder24_behaviour dut(en,a,b,y);
7
8    initial
9      begin
10
11       en=1;a=1'bx;b=1'bx;#5
12       en=0;a=0;b=0;#5
13       en=0;a=0;b=1;#5
14       en=0;a=1;b=0;#5
15       en=0;a=1;b=1;#5
16
17
18       $finish;
19     end
20 endmodule
```

WAVEFORM:--



SCHEMATIC:--