DAY-59
#100DAYSOFRTL

AIM:--IMPLEMENTATION OF T FLIP-FLOP USING JK FLIP-FLOP.

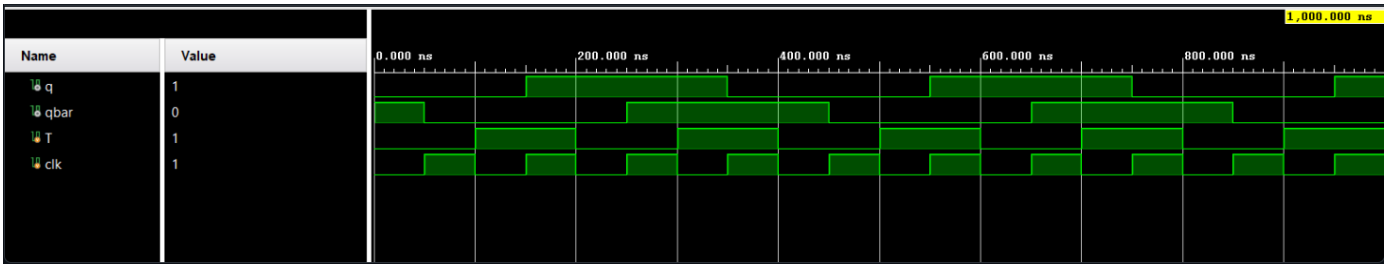
VERILOG CODE:--

```
module jk_flipflop( input clk, j, k,output reg q, qbar);
always @(posedge clk)
    begin
        q=1'b1;
        qbar = 1'b1;

        case ({j, k})
            2'b00: begin
                q <= q;
                qbar <= qbar;end
            2'b01: begin
                q <= 1'b0;
                qbar <= 1'b1;end
            2'b10: begin
                q <= 1'b1;
                qbar <= 1'b0;end
            2'b11: begin
                q <= 1'b1;
                qbar <= 1'b0;end
        endcase
    end
endmodule

module jk_to_t(input clk,
    input t,
    output reg q,
    output reg qbar);
    wire j, k;
 assign t = j & k;
jk_flipflop jkff (clk, j, k, q, qbar);
endmodule
```

TESTBENCH CODE:--

```
module jk_to_t_tb();
 reg t,clk;
  wire q, qbar;

    sr_to_t dut (clk,t,q,qbar);
    initial
    clk = 0;
    always #5 clk = ~clk;


    initial begin

#10 t=1;
#10 t=0;
#10 t=1;
#10 t=0;


        #20;

$finish;
end
endmodule
```

WAVEFORM:--



SCHEMATIC:-