# DAY-5 #100DAYSOFRTL

# **AIM:--**IMPLEMENTATION OF RIPPLE CARRY ADDER IN VERILOG.

#### **VERILOG RTL CODE:--**

```
module full_adder(a,b,cin,sum,carry);
 3
         input a,b,cin;
 4
         output sum, carry;
 5
     O assign sum=a^b^cin;
 6
     O assign carry=(a&b)|(b&cin)|(cin&a);
 8
 9 🖒
         endmodule
10
11 ⊖
        module ripple_carry_adder(input [3:0]a,b,input cin, output [3:0]sum,output c4);
12
13
         wire c1, c2, c3;
14
15
         full adder fa0(a[0],b[0],cin,sum[0],c1);
16
         full_adder fa1(a[1],b[1],c1,sum[1],c2);
         full_adder fa2(a[2],b[2],c2,sum[2],c3);
17
18
         full_adder fa3(a[3],b[3],c3,sum[3],c4);
19
20 🖨
         endmodule
21
```

#### **TESTBENCH CODE:--**

```
1 🖯
        module ripple_carry_adder_tb;
 2
        reg [3:0]a,b;
 3
        reg cin;
        wire [3:0]sum;
 4
 5
        wire c4;
 6
 7
        ripple_carry_adder dut(a,b,cin,sum,c4);
 8
 9 🖨
        initial begin
     O cin = 0;
10
     O | a = 4'b0110;
11 !
12
     0 b = 4'b1100;
     O #10
13
14 !
    O a = 4'b1110;
     0 b = 4'b1000;
15
16 0 #10
17 !
    O \mid a = 4'b0111;
    O b = 4'b1110;
18
19 0 #10
    O \mid a = 4'b0010;
20 :
    O b = 4'b1001;
21
    O #10
22 1
    ○→$finish();
23 :
24 🖨
25 i
26 🖯
     endmodule
```

### **WAVEFORM:--**

Name	Value	0.000 ns  5.000 ns	10.000 ns 15.000 ns	20.000 ns   25.000 ns	30.000 ns   35.000 ns
> <b>₩</b> a[3:0]	6	6	е	7	2
> ₩ b[3:0]	С	С	8	e	9
<sup>™</sup> cin	0				
> <b>₩</b> sum[3:0]	2	2	6	5	h
™ c4	1				

## **SCHEMATIC:--**

