DAY-57
#100DAYSOFRTL

AIM:--IMPLEMENTATION OF D FLIP-FLOP USING JK FLIP-FLOP.

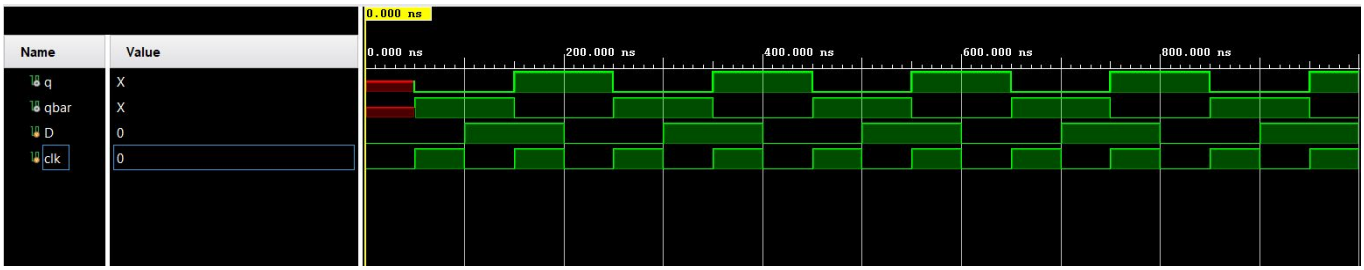
VERILOG CODE:--

```
module jk_flipflop( input clk, j, k,output reg q, qbar);

    always @(posedge clk)
     begin
     q <= 1;
      qbar <= 1;

    case ({j, k})
            2'b00: begin
                q <= q;
                qbar <= qbar;end
            2'b01: begin
                q <= 1'b0;
                qbar <= 1'b1;end
            2'b10: begin
                q <= 1'b1;
                qbar <= 1'b0;end
            2'b11: begin
                q <= 1'b0;
                qbar <= 1'b1;end
        endcase
    end
endmodule

module jk_to_d(input clk,d,output q, qbar);
wire j, k;
assign j = d;
assign k = ~d;
jk_flipflop jkff (clk, d, q, qbar);
endmodule
```

TESTBENCH CODE:--

```
1  module sr_to_d_tb();
2  reg clk,d;
3  wire q,qbar;
4
5  sr_to_d dut (clk,d,q,qbar);
6
7  initial
8  clk=0;
9
10 always #5 clk=~clk;
11
12 initial begin
13
14 #10 d=0;
15 #10 d=1;
16 #10 d=1;
17 #10 d=0;
18
19 $finish;
20 end
21 endmodule
22
```

WAVEFORM:--



SCHEMATIC:-