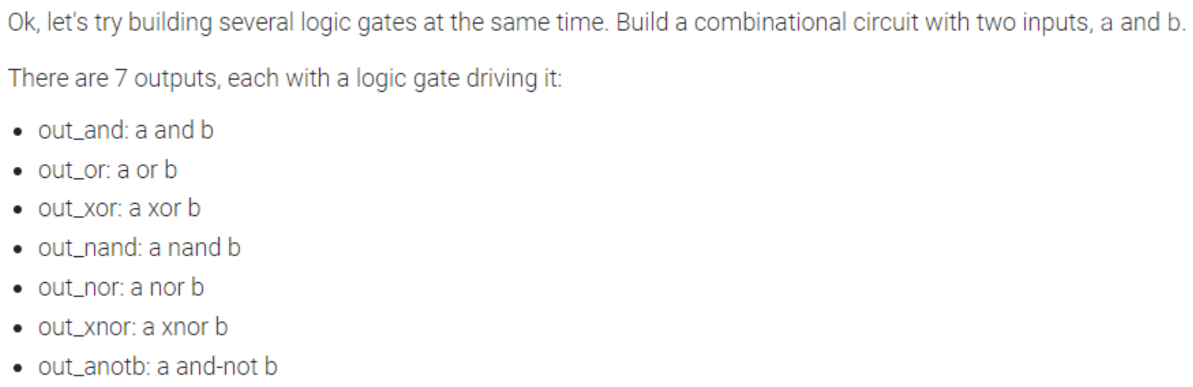
DAY-11
#100DAYSOFRTL

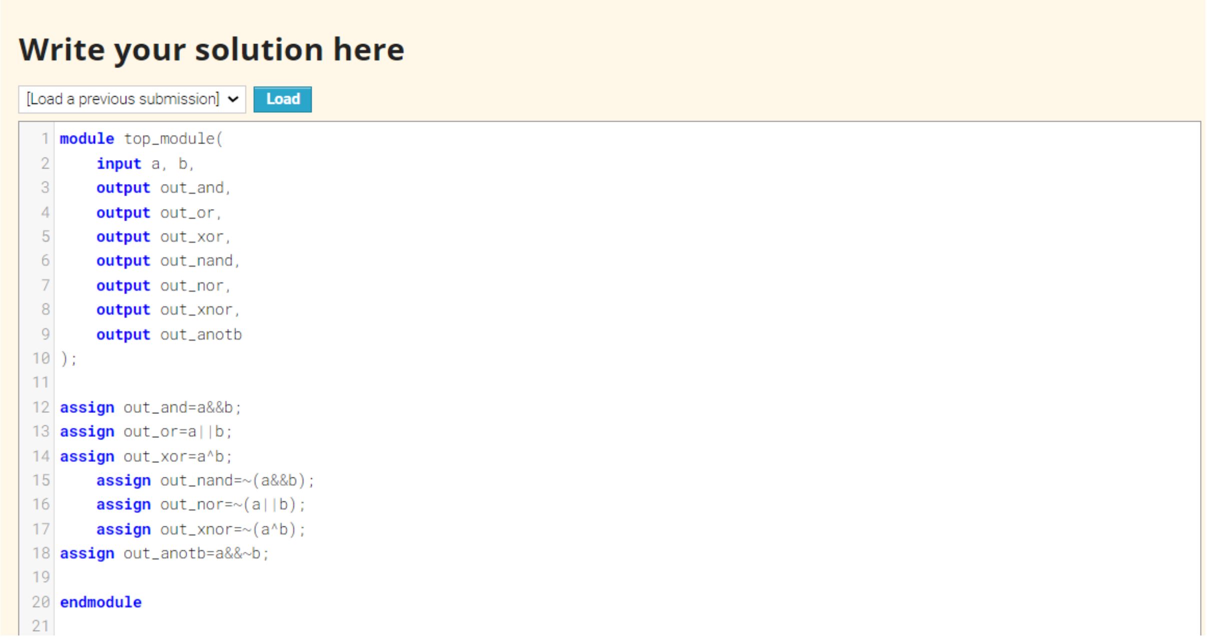
1.



Ok, let's try building several logic gates at the same time. Build a combinational circuit with two inputs, a and b.

There are 7 outputs, each with a logic gate driving it:

- out_and: a and b
- out_or: a or b
- out_xor: a xor b
- out_nand: a nand b
- out_nor: a nor b
- out_xnor: a xnor b
- out_anotb: a and-not b



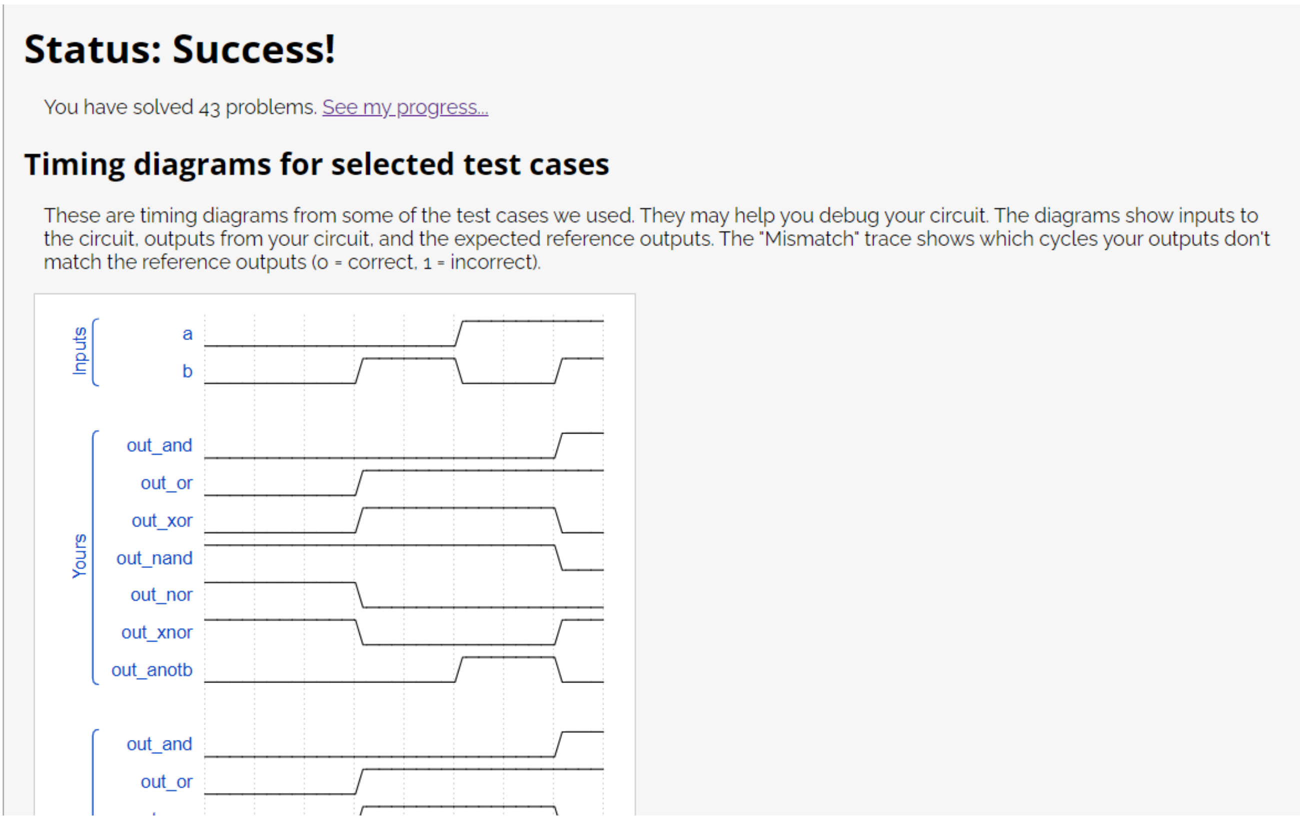
Write your solution here

```
module top_module(
    input a, b,
    output out_and,
    output out_or,
    output out_xor,
    output out_nand,
    output out_nor,
    output out_xnor,
    output out_anotb
);

assign out_and=a&&b;
assign out_or=a||b;
assign out_xor=a^b;
    assign out_nand=~(a&&b);
    assign out_nor=~(a||b);
    assign out_xnor=~(a^b);
assign out_anotb=a&&~b;

endmodule

```



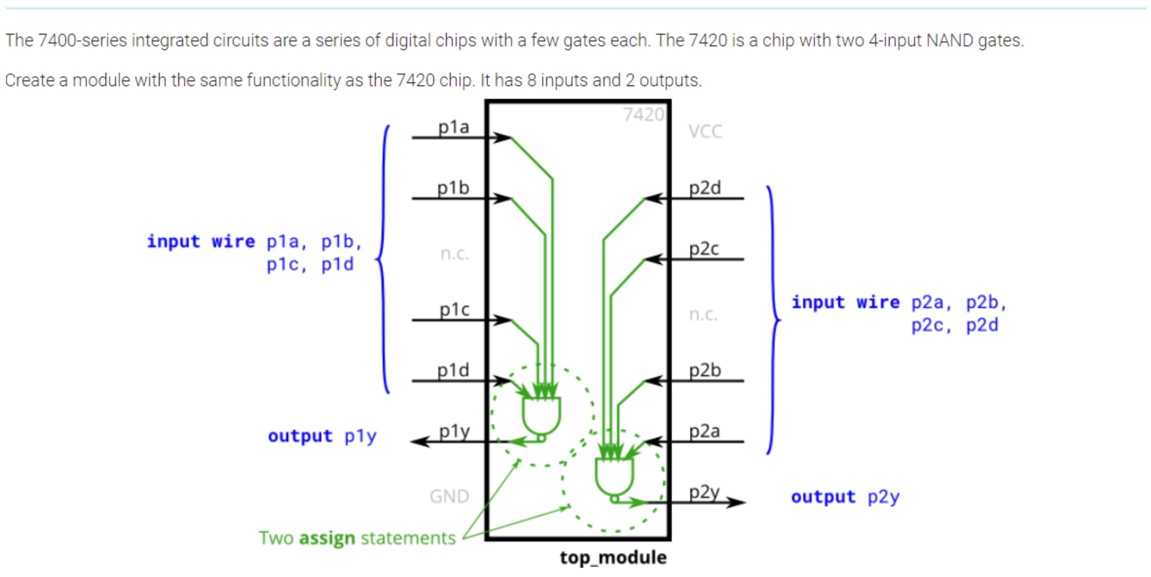
Status: Success!

You have solved 43 problems. See my progress...

Timing diagrams for selected test cases

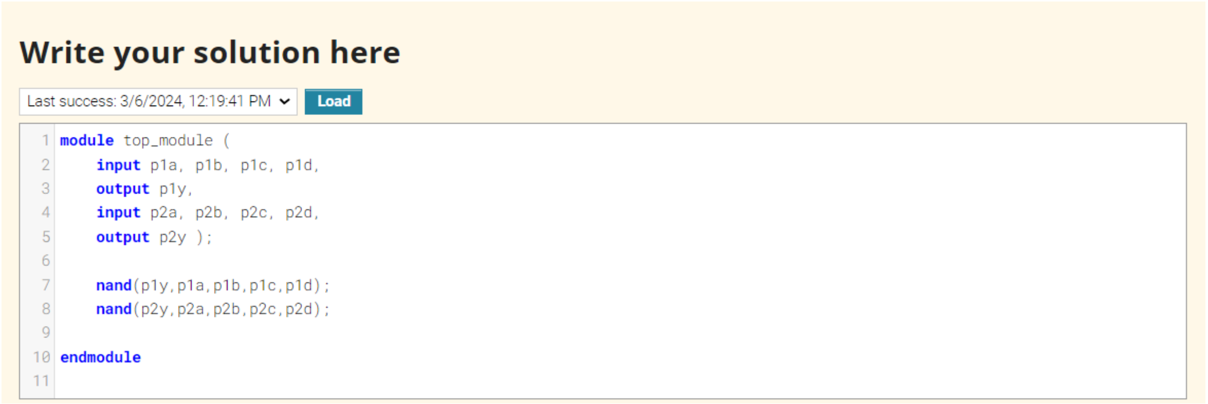
These are timing diagrams from some of the test cases we used. They may help you debug your circuit. The diagrams show inputs to the circuit, outputs from your circuit, and the expected reference outputs. The "Mismatch" trace shows which cycles your outputs don't match the reference outputs (0 = correct, 1 = incorrect).

2.



The 7400-series integrated circuits are a series of digital chips with a few gates each. The 7420 is a chip with two 4-input NAND gates.

Create a module with the same functionality as the 7420 chip. It has 8 inputs and 2 outputs.

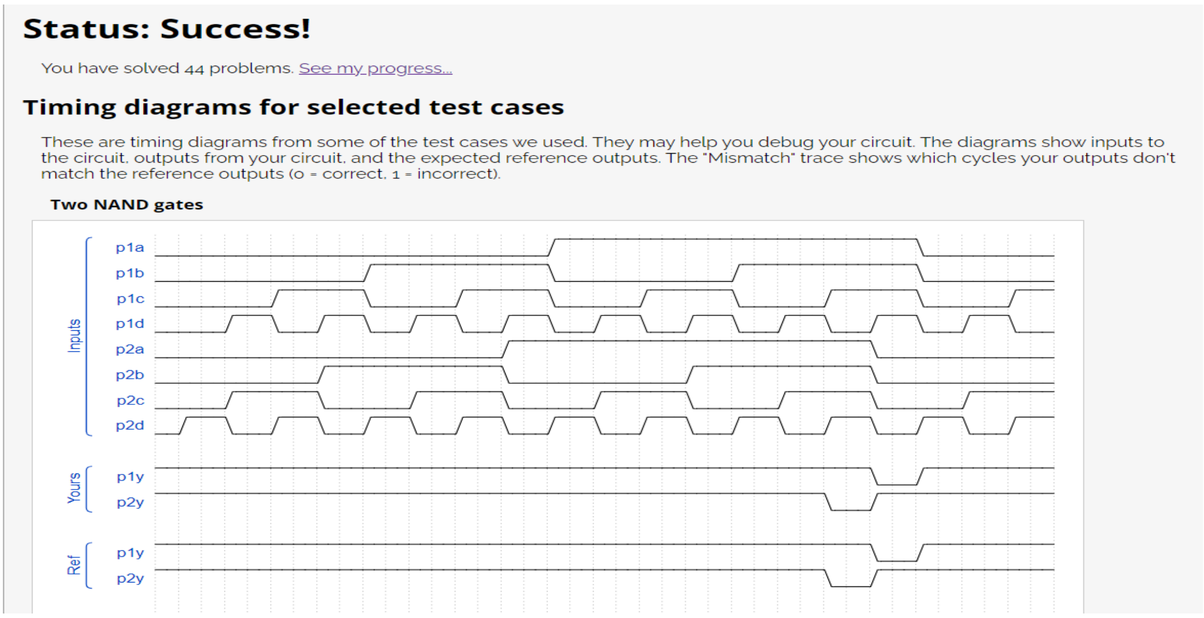


Write your solution here

```verilog
module top_module (
    input p1a, p1b, p1c, p1d,
    output p1y,
    input p2a, p2b, p2c, p2d,
    output p2y );

    nand(p1y,p1a,p1b,p1c,p1d);
    nand(p2y,p2a,p2b,p2c,p2d);

endmodule
```



Status: Success!

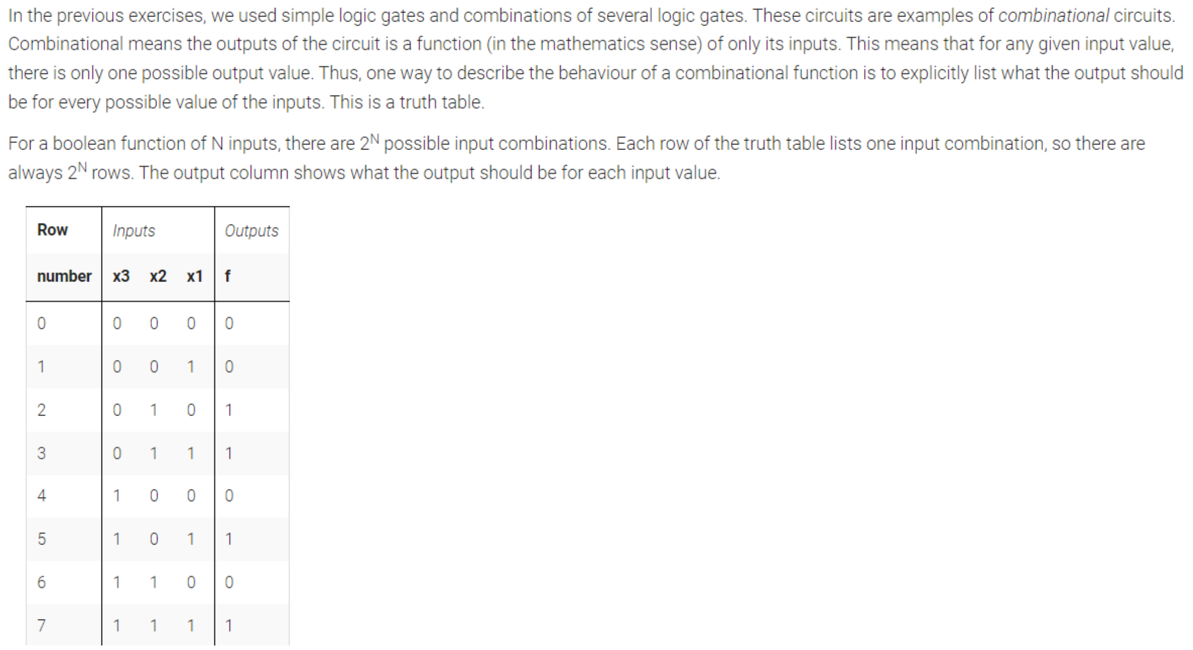
You have solved 44 problems. See my progress...

Timing diagrams for selected test cases

These are timing diagrams from some of the test cases we used. They may help you debug your circuit. The diagrams show inputs to the circuit, outputs from your circuit, and the expected reference outputs. The "Mismatch" trace shows which cycles your outputs don't match the reference outputs (0 = correct, 1 = incorrect).

Two NAND gates

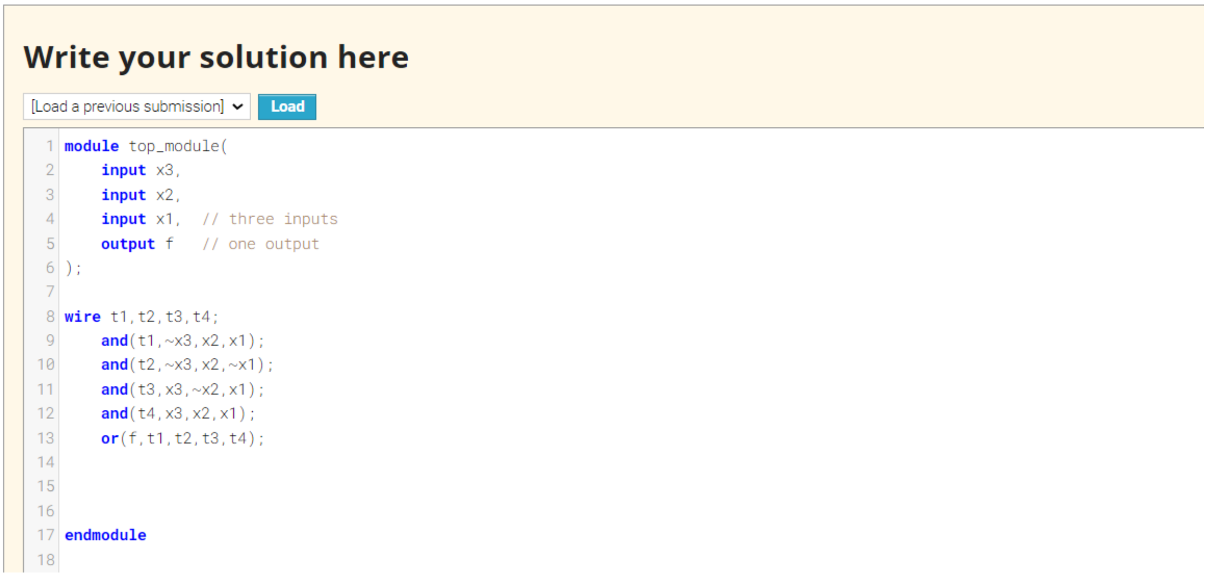
3.



In the previous exercises, we used simple logic gates and combinations of several logic gates. These circuits are examples of *combinational* circuits. Combinational means the outputs of the circuit is a function (in the mathematics sense) of only its inputs. This means that for any given input value, there is only one possible output value. Thus, one way to describe the behaviour of a combinational function is to explicitly list what the output should be for every possible value of the inputs. This is a truth table.

For a boolean function of N inputs, there are 2^N possible input combinations. Each row of the truth table lists one input combination, so there are always 2^N rows. The output column shows what the output should be for each input value.

Row	*Inputs*			*Outputs*
number	**x3**	**x2**	**x1**	**f**
0	0	0	0	0
1	0	0	1	0
2	0	1	0	1
3	0	1	1	1
4	1	0	0	0
5	1	0	1	1
6	1	1	0	0
7	1	1	1	1



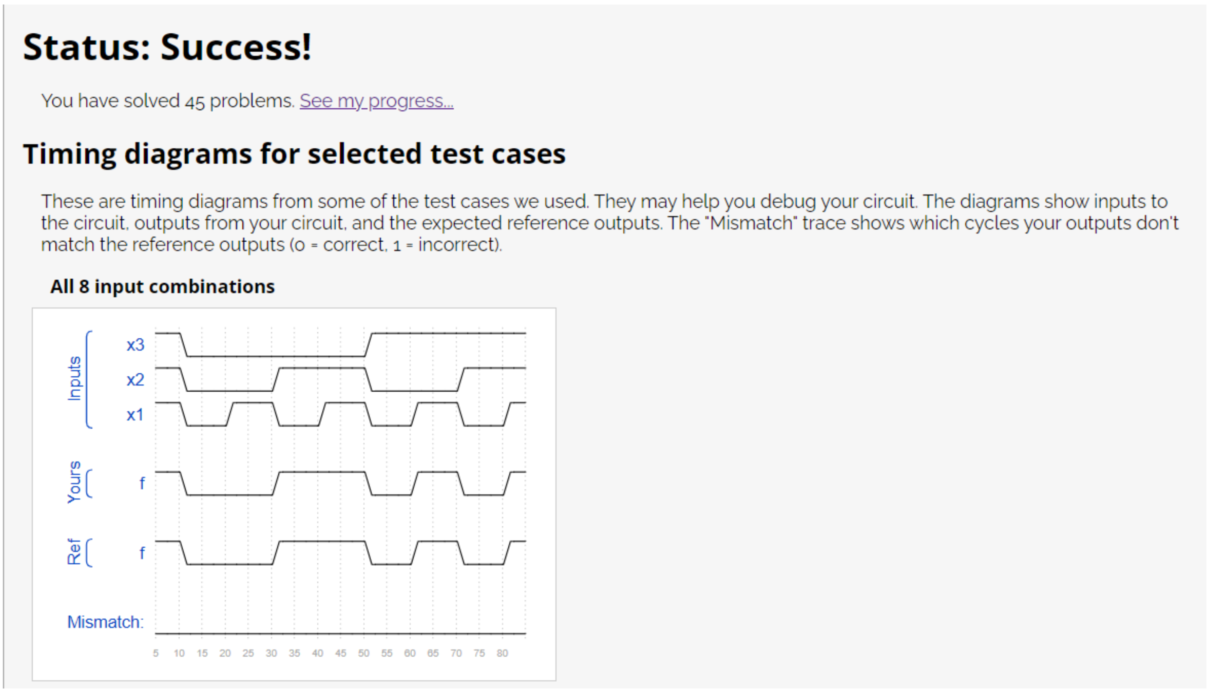
Write your solution here

```
module top_module(
    input x3,
    input x2,
    input x1,  // three inputs
    output f   // one output
);

wire t1,t2,t3,t4;
    and(t1,~x3,x2,x1);
    and(t2,~x3,x2,~x1);
    and(t3,x3,~x2,x1);
    and(t4,x3,x2,x1);
    or(f,t1,t2,t3,t4);



endmodule
```



Status: Success!

You have solved 45 problems. See my progress...

Timing diagrams for selected test cases

These are timing diagrams from some of the test cases we used. They may help you debug your circuit. The diagrams show inputs to the circuit, outputs from your circuit, and the expected reference outputs. The "Mismatch" trace shows which cycles your outputs don't match the reference outputs (0 = correct, 1 = incorrect).

All 8 input combinations