DAY-56 #100DAYSOFRTL

AIM:--IMPLEMENTATION OF T FLIP-FLOP USING SR FLIP-FLOP.

VERILOG CODE:--

```
module sr_To_d(input clk,s,r,output reg q, qbar);
 2 🖯
        always @(posedge clk) begin
 3 🖨
            case ({s, r})
 4 🖨
               2'b00: begin
                    q <= q;
 6 🖒
                    qbar <= qbar;end
 7 🖨
               2'b01: begin
8 ¦
                   q <= 1'b0;
9 🖒 🔘
                    qbar <= 1'b1;end
10 0
               2'b10: begin
11 !
                    q <= 1'b1;
12 🖒 🔘
                    qbar <= 1'b0;end
13 🖟 O
               2'b11: begin
14 :
                   q <= 1'b0;
15 🖨
                    qbar <= 1'b1;end
16 🖨 🔘 🖟
            endcase
17 @ O end
18 🖒
        endmodule
19 🖨
        module srflipflop(
    0
20 :
           input clk,
     0
21
           input d,
22 |
           output reg qn,
23
            output reg qnbar);
    O wire s = d;
24
     O wire r = ~d;
25
26
27
        sr To d dut (clk, s, r, qn, qnbar);
28
29 🖨
        endmodule
```

TESTBENCH CODE:--

```
1 \(\begin{aligned}
\text{module sr_to_t_tb();}
\end{aligned}
     reg t,clk;
 3 wire q, qbar;
5 | sr_to_t dut (clk,t,q,qbar);
6   initial
6 🖯
       clk = 0;
7 🖨
        always #5 clk = ~clk;
9
10
11 \bigcirc initial begin
12
13 | #10 t=1;
14 | #10 t=0;
15 | #10 t=1;
16 #10 t=0;
17
18
19 i
            #20;
20
21 | $finish;
22 🖨 end
23 @ endmodule
24
25
```

WAVEFORM:--



SCHEMATIC:-

