DAY-5
#100DAYSOFRTL

AIM:--IMPLEMENTATION OF RIPPLE CARRY ADDER IN VERILOG.

VERILOG RTL CODE:--

```
1   module full_adder(a,b,cin,sum,carry);
2
3   input a,b,cin;
4   output sum,carry;
5
6   assign sum=a^b^cin;
7   assign carry=(a&b)|(b&cin)|(cin&a);
8
9   endmodule
10
11  module ripple_carry_adder(input [3:0]a,b,input cin, output [3:0]sum,output c4);
12
13  wire c1,c2,c3;
14
15  full_adder fa0(a[0],b[0],cin,sum[0],c1);
16  full_adder fa1(a[1],b[1],c1,sum[1],c2);
17  full_adder fa2(a[2],b[2],c2,sum[2],c3);
18  full_adder fa3(a[3],b[3],c3,sum[3],c4);
19
20  endmodule
21
```

TESTBENCH CODE:--

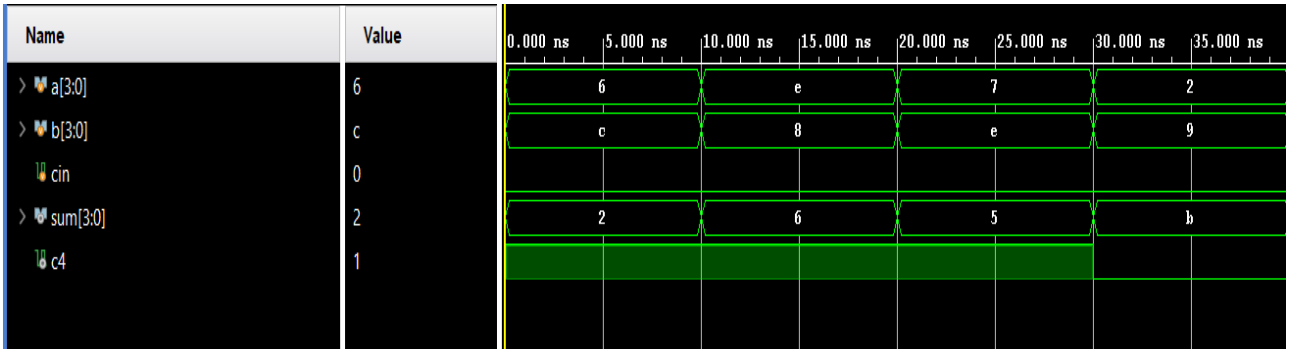
```
module ripple_carry_adder_tb;
reg [3:0]a,b;
reg cin;
wire [3:0]sum;
wire c4;

ripple_carry_adder dut(a,b,cin,sum,c4);

initial begin
cin = 0;
a = 4'b0110;
b = 4'b1100;
#10
a = 4'b1110;
b = 4'b1000;
#10
a = 4'b0111;
b = 4'b1110;
#10
a = 4'b0010;
b = 4'b1001;
#10
$finish();
end

endmodule
```

WAVEFORM:--



SCHEMATIC:--