DAY-90
#100DAYSOFRTL

AIM:--- IMPLEMENTATION OF FREQUENCY DIVIDER BY EVEN NUMBER

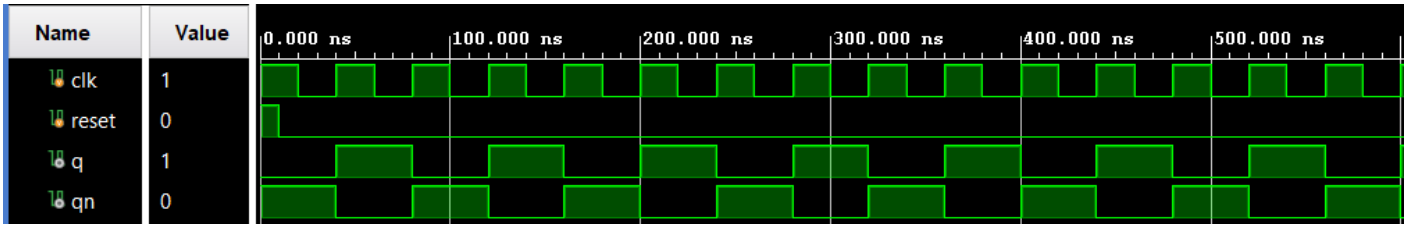
VERILOG CODE:--

```
module d_ff(
    input in,
    input clk,
    input rst,
    output reg q,
    output qbar
    );
    assign qbar=~q;
    always@(posedge clk, posedge rst)
    begin
        if(rst)
            q<= 0;
        else
            q <=in;
        end
endmodule

module freq_by2(
    input clk,reset,
     output q,qn
     );

    wire t;
    d_ff d1(t,clk,reset,q,qn);
    assign t = qn;

endmodule
```

TESTBENCH CODE:---

```
module tb_freq_by2;

    reg clk;
    reg reset;

    wire q;
    wire qn;

    freq_by2 uut (
        .clk(clk),
        .q(q),
        .qn(qn),
        .reset(reset)
    );

    initial begin

        clk = 0;
        reset = 1;

        #10;
        reset = 0;


    end

    always
    begin
    clk = ~clk;
    #20;
    end
```

WAVEFORM:-----



SCHEMATIC BLOCK :-------