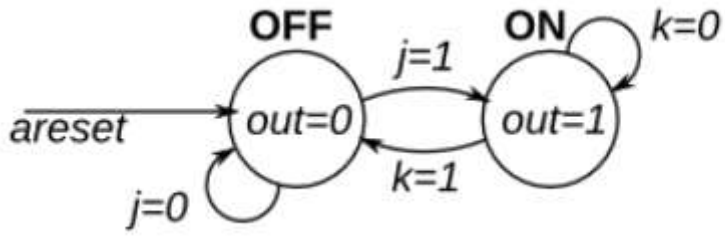
DAY-94
#100DAYSOFRTL

AIM:--- IMPLEMENTATION OF FINITE STATE MACHINE



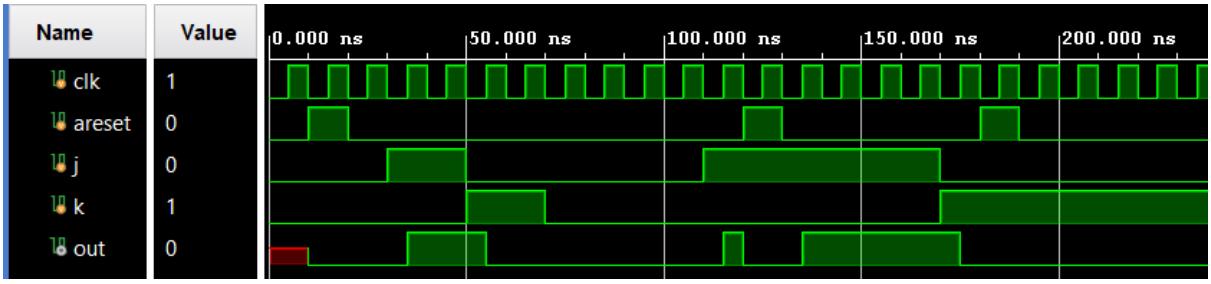
VERILOG CODE:--

```
module top_module(
    input clk,
    input areset,
    input j,
    input k,
    output out);

    parameter OFF=0, ON=1;
    reg state, next_state;

    always @(*) begin
        if(state==OFF&&j==0)
            next_state<=OFF;
        else if(state==OFF&&j==1)
            next_state<=ON;
        else if(state==ON&&k==1)
            next_state<=OFF;
        else if(state==ON&&k==0)
            next_state<=ON;
        else
            next_state<=next_state;


    end

    always @(posedge clk, posedge areset) begin
        if(areset)
            state<=OFF;
        else
            state<=next_state;
    endlogic
    assign out = (state == OFF)?1:
```

TESTBENCH CODE:---

```
1   `timescale 1ns/1ps
2
3   module top_module_tb;
4
5       // Inputs
6       reg clk;
7       reg areset;
8       reg j;
9       reg k;
10
11      wire out;
12
13      top_module uut (
14          .clk(clk),
15          .areset(areset),
16          .j(j),
17          .k(k),
18          .out(out)
19      );
20
21      always begin
22      end
23
24      initial begin
25          clk = 0;
26          areset = 0;
27          j = 0;
28          k = 0;
29          #10 areset = 1;
30          #10 areset = 0;
```

WAVEFORM:-----



SCHEMATIC BLOCK :-------