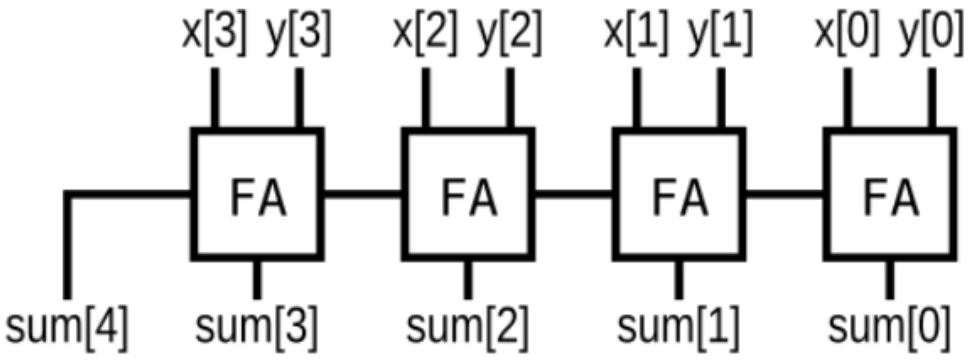
DAY-24
#100DAYSOFRTL

PROBLEM STATEMENT:--

1. Implement the following

Implement the following circuit:



("FA" is a full adder)

Write your solution here

[Load a previous submission] Load

```
module top_module (
    input [3:0] x,
    input [3:0] y,
    output [4:0] sum);

    wire w1,w2,w3;

    full_adder fa1(x[0],y[0],1'b0,w1,sum[0]);
    full_adder fa2(x[1],y[1],w1,w2,sum[1]);
    full_adder fa3(x[2],y[2],w2,w3,sum[2]);
    full_adder fa4(x[3],y[3],w3,sum[4],sum[3]);

endmodule

module full_adder(input a,b,cin,output cout,sum);

    assign sum=a^b^cin;
    assign cout=a&b | b&cin | a&cin;

endmodule
```

exams/m2014_q4j — Compile and simulate

Running Quartus synthesis. Show Quartus messages...
Running ModelSim simulation. Show Modelsim messages...

Status: Success!

You have solved 58 problems. See my progress...