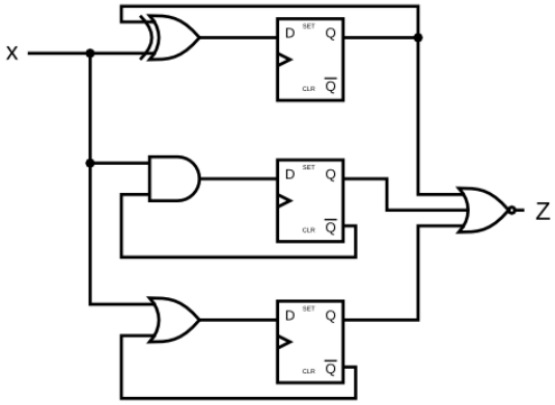
DAY-49
#100DAYSOFRTL

PROBLEM STATEMENT:--

1.

Given the finite state machine circuit as shown, assume that the D flip-flops are initially reset to zero before the machine begins.

Build this circuit.



Write your solution here

[Load a previous submission] Load

```
module top_module (
    input clk,
    input x,
    output z
);
    reg [2:0] Q;
    always@(posedge clk)
        begin
            Q[0]<= Q[0] ^ x;
            Q[1]<= ~Q[1] & x;
            Q[2]<= ~Q[2]|x;

        end
    assign z=~( | Q);
endmodule

```

Submit Submit (new window)

Upload a source file...

exams/ece241_2014_q4 — Compile and simulate

Running Quartus synthesis. Show Quartus messages...
Running ModelSim simulation. Show Modelsim messages...

Status: Success!

You have solved 81 problems. See my progress...

Timing diagrams for selected test cases

These are timing diagrams from some of the test cases we used. They may help you debug your circuit. The diagrams show inputs to the circuit, outputs from your circuit, and the expected reference outputs. The "Mismatch" trace shows which cycles your outputs don't match the reference outputs (0 = correct, 1 = incorrect).