DAY-87
#100DAYSOFRTL

AIM:--- IMPLEMENTATION OF SIMPLE REGISTER .

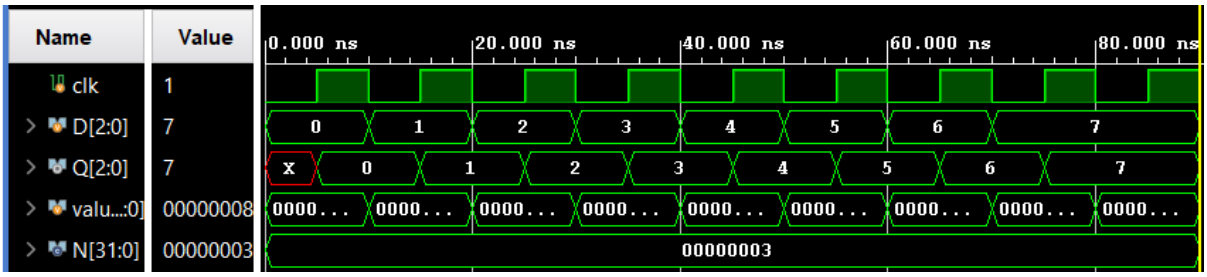
VERILOG CODE:--

```
module simple_register #(parameter N=5)(clk,D,Q);
input clk;
input [N-1:0]D;
output [N-1:0] Q;

reg [N-1:0]q_next,q_reg;

always@(posedge clk)
begin
    q_reg  = q_next;
end

always@(D)
begin
    q_next = D;
end

assign Q = q_reg;
endmodule
```

TESTBENCH CODE:---

```
1  module simple_register_TB();
2  localparam N = 3;
3  reg clk;
4  reg [N-1:0]D;
5  wire [N-1:0] Q;
6
7  integer value;
8
9  simple_register #(N)dut(clk,D,Q);
10
11 initial begin
12  clk = 0;
13 forever #5 clk = ~ clk; end
14
15 initial begin
16     $monitor("D=%b ---> Q=%b",D,Q);
17 end
18
19 initial begin
20     for(value = 0; value < 8; value = value + 1)
21     begin
22         D = value;
23         #10;
24     end
25     #10 $finish;
26 end
27 endmodule
28
```

WAVEFORM:-----



SCHEMATIC BLOCK :-------