DAY-80
#100DAYSOFRTL

AIM:--- IMPLEMENTATION OF MINORITY DECTOR.

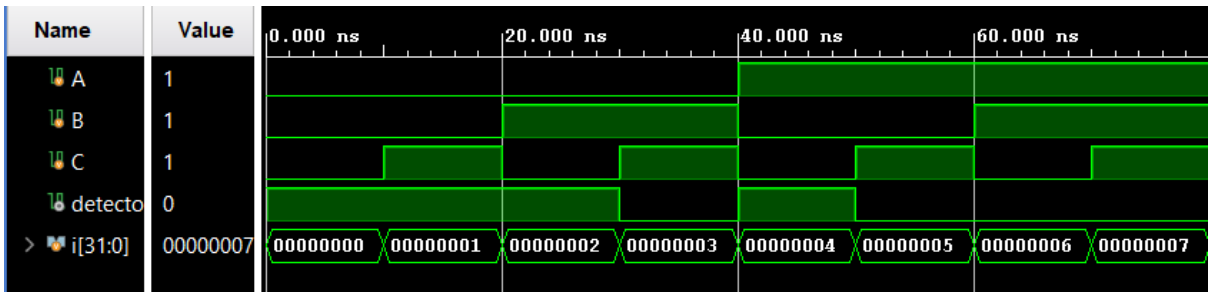
VERILOG CODE:--

```
module minority_detector(A,B,C,detector);
input A,B,C;
output detector;
wire W1,W2,W3;

 assign W1 = A&B;
 assign W2 = B&C;
 assign W3 = C&A;

 assign detector = ~(W1|W2|W3);


endmodule
```

TESTBENCH CODE:---

```
1  module min_dect_tb();
2  reg A,B,C;
3  wire detector;
4  integer i;
5
6  ///Instantiation
7  minority_detector MJ(A,B,C,detector);
8
9  ///Initialization
10 initial
11 {A,B,C} = 0;
12
13 ///stimulus Generation
14 initial
15  begin
16    for(i=0; i<8; i=i+1)
17     begin
18      {A,B,C} = i;
19      #10;
20     end
21  end
22 initial #80 $finish;
23 endmodule
24
```

WAVEFORM:-----



SCHEMATIC BLOCK :-------