

# DAY-88

## #100DAYSOFRTL

**AIM:---** IMPLEMENTATION OF VEDIC MULTIPLIER.

**VERILOG CODE:--**

```
1  | `timescale 1ns / 1ps
2  |
3  | module half_adder(
4  |     input a,b,
5  |     output sum,carry
6  | );
7  |     assign sum=a^b;
8  |     assign carry=a&b;
9  | endmodule
10 |
11 | module vedic_mul_2_2(
12 |     input [1:0] a,b,
13 |     output [3:0] out
14 | );
15 |
16 |     wire [3:0] w;
17 |
18 |     and m1(out[0],a[0],b[0]);
19 |     and m2(w[0],a[0],b[1]);
20 |     and m3(w[1],a[1],b[0]);
21 |     and m4(w[2],a[1],b[1]);
22 |
23 |     half_adder ha1(w[0],w[1],out[1],w[3]);
24 |     half_adder ha2(w[3],w[2],out[2],out[3]);
25 |
26 | endmodule
```

## TESTBENCH CODE:---

```
1 module test_bench;
2   reg [1:0]a,b;
3   wire [3:0]out;
4
5   vedic_mul_2_2 dut(a,b,out);
6
7   always begin
8       a=2'd2;
9       b=2'd1;
10      #10;
11      a=2'd3;
12      b=2'd2;
13      #10;
14      a=2'd0;
15      b=2'd1;
16      #10;
17      a=2'd3;
18      b=2'd1;
19      #10;
20      a=2'd2;
21      b=2'd2;
22      #10;
23      a=2'd3;
24      b=2'd3;
25      #10;
26  end
27
28  initial begin
29      $monitor("%d * %d = %d", a,b,out);
30      #60 $finish;
31  end
32 endmodule
```

## WAVEFORM:-----

Name	Value	0.000 ns	10.000 ns	20.000 ns	30.000 ns	40.000 ns	50.000 ns
> a[1:0]	3	2	3	0	3	2	3
> b[1:0]	3	1	2		1	2	3
> out[3:0]	9	2	6	0	3	4	9

## SCHEMATIC BLOCK :-----

