DAY-54
#100DAYSOFRTL

AIM:--IMPLEMENTATION OF SR FLIP-FLOP USING JK FLIP-FLOP.

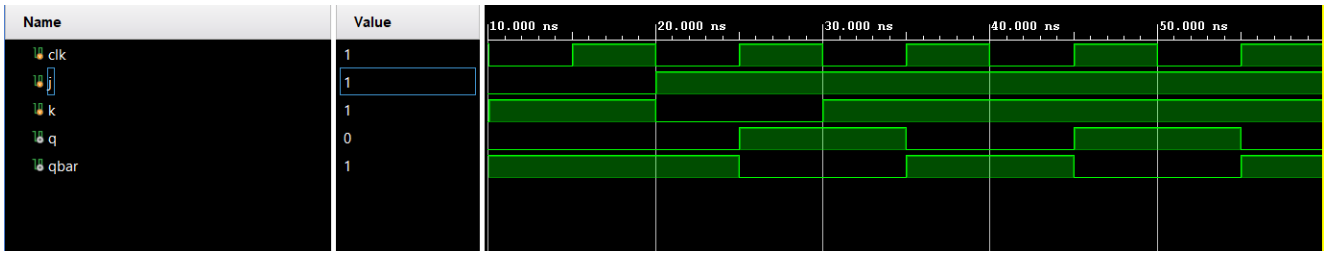
VERILOG CODE:--

```
module sr_flipflop( input clk, s, r,output reg q, qbar);

    always @(posedge clk)
    begin
        q=1'b0;
        qbar = 1'b1;

        case ({s, r})
            2'b00: begin
                q <= q;
                qbar <= qbar;end
            2'b01: begin
                q <= 1'b0;
                qbar <= 1'b1;end
            2'b10: begin
                q <= 1'b1;
                qbar <= 1'b0;end
            2'b11: begin
                q <= 1'b1;
                qbar <= 1'b0;end
        endcase
    end
endmodule
module sr_to_jk(
    input clk,j,k,
    output q, qbar);

    wire s, r;

    assign s = qbar & j;
    assign r = q & k;

    sr_flipflop srff (clk, s, r, q, qbar);

endmodule
```

TESTBENCH CODE:--

```
1   module sr_to_jk_test();
2       reg j, k, clk;
3       wire q, qbar;
4
5       sr_to_jk dut (clk,j,k,q,qbar);
6       initial
7       clk = 0;
8       always #5 clk = ~clk;
9
10
11      initial begin
12
13
14          j = 0;k = 0;#10;
15          j = 0;k = 1;#10;
16          j = 1;k = 0;#10;
17          j = 1;k = 1;#10;
18
19          #20;
20
21  $finish;
22  end
23  endmodule
24
```

WAVEFORM:--



SCHEMATIC:-