DAY-75
#100DAYSOFRTL

AIM:--- IMPLEMENTATION OF 4-BIT PARALLE IN SERIAL OUT (PISO).

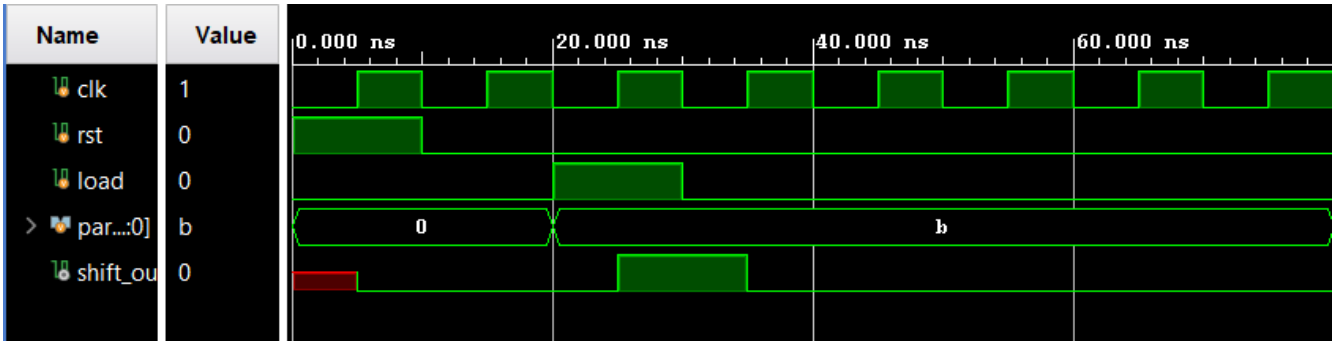
VERILOG CODE:--

```
1   module piso (
2       input clk,
3       input  rst,
4       input load,
5       input  [3:0] parallel_in,
6       output  shift_out
7   );
8
9       reg [3:0] shift_reg;
10      always @(posedge clk) begin
11          if (rst) begin
12              shift_reg <= 4'b0000;
13          end else if (load) begin
14              shift_reg <= parallel_in;
15          end else begin
16              shift_reg <= {shift_reg[2:0], 1'b0};
17          end
18      end
19
20      assign shift_out = shift_reg[0];
21
22  endmodule
23
```

TESTBENCH CODE:---

```
module piso_tb;

    reg clk;
    reg rst;
    reg load;
    reg [3:0] parallel_in;
    wire shift_out;

    piso uut (
        .clk(clk),
        .rst(rst),
        .load(load),
        .parallel_in(parallel_in),
        .shift_out(shift_out)
    );


    always #5 clk = ~clk;


    initial begin
        clk = 0;
        rst = 1;
        load = 0;
        parallel_in = 4'b0000;

        #10 rst = 0;

        #10 load = 1;
        parallel_in = 4'b1011;

        #10 load = 0;
```

WAVEFORM:-----



SCHEMATIC BLOCK :-------