Failure Analysis of QFP Package Interconnection structure under Random Vibration and Temperature

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***Abstract*—Nowadays, electronic equipment plays a key and important role in equipment and system, especially with the development of informatization. The failure of interconnect between the chip and PCB, is a major failure mode in electronic equipment, and vibration and temperature are the main environmental factors leading to solder joint failure, which are also the focus of this paper. This study analyzes the failure of QFP chip by random vibration test under three different temperature conditions. The test piece of QFP chip has a self-monitoring circuit, which can monitor its own state whether it is invalid or not. Firstly, the failure of interconnection structure and the effect of their location on reliability has been investigated. Then, the effect of temperature on vibration reliability for interconnection structures has been analyzed. Finally, combined with the exponential distribution of the interconnection structure, the random vibration reliability of the whole chip at different temperatures is evaluated. The results indicate that the interconnection structure of the same chip has similar failure modes, while the crack growth rate is various due to their location, resulting in the difference in their life. Failure modes of interconnect under 25℃ and 75℃ are similar, which different from failure modes under -25℃, and low temperature reduces vibration reliability of interconnection structure.**

Keywords: Interconnection structure; Temperature; Random vibration; Failure modes; Location; Life distribution

I. INTRODUCTION

Solder joints are a key part of electronic devices, which connect electronic components and PCB to achieve electrical interconnection and mechanical fixation between them [1,2]. Failure of a solder joint may result in failure of the entire electronic equipment, especially the failure of solder joints connecting key chips and the circuit board. Currently, the Plastic Quad Flat Package (QFP), one of surface mount package, is widely used in electronic devices. However, failure of solder joints in electronic device using surface mount package has not been investigated thoroughly.

In fact, two main difficulties are faced with in failure research of solder joints. The first involves finding the effect of environmental loading to solder joints, which including the effect to failure rate and failure mode. According to U.S. Air Force, 75% of failure in electronic devices is induced by temperature and vibration. Therefore, some researches have studied the solder joint reliability under temperature or vibration. There are two main approaches to do this. One is by applying temperature and vibration tests in sequence, for example, Gu et al [3] conduct temperature and vibration test successively on SAC305, to study the reliability of SAC305. The other is by applying both temperature and vibration, such as Zhang et al [4]. They applied both temperature and random vibration to SAC305, to study the failure mode and crack propagation of SAC305. In addition, some research solder joint reliability through simulation. Liu et al [5] have investigated the reliability and fatigue life prediction of BGA solder joints under random vibration. Zhou et al [6] have studied the influence of temperature of cycling mode (continuous and intermittent) on the fatigue life of solder joints.

The second problem arises from the fact that solder joints may suffer from different stress due to their different location. For the sake of simplicity, however, many researchers have only focus on the critical solder joint, assuming that the critical solder joint would failure first comparing the others. In reality, some solder joint may failure before the critical one. The effect of location on solder joints, and the reliability of a chip considering all solder joints, are seldom studied, which is a focus of this paper.

It is known that is will be extremely difficult to assess the reliability of a chip, considering all of solder joints. The first difficulty is how to monitor the status and the failure of solder joints. In order to fixed this problem, some researches have made some attempts. Some use mechanical properties to characterize the solder joint state, such as Tang et al [7], monitoring the strain near the key solder joints, and While Lall et al [8], extracting full field strain of the PCB by high speed cameras. Others use electrical signals to monitor solder joint conditions, such as Liu et al [7], measuring the voltage at both ends of the Daisy chain solder joint, and Wang et al [9,10], measuring solder joint resistance by their online test circuit. However, the strain-method is not possible in practice, and its accuracy and efficiency maybe low. Moreover, the daisy-chain method is impossible to implement when chips are working. In the previous research [11], we have established the equivalent model of the interconnection structure (IS) and

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designed the on-line monitoring circuit. The results show that the charging time can represent the degradation and failure of interconnection structure. Fig. 1 shows the schematic diagram of QFP package. In this article, we would continue to use this method to characterize the failure of the interconnection structure

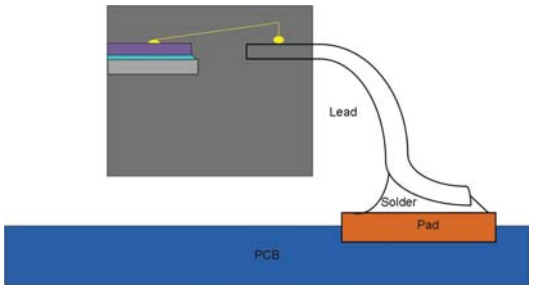


Figure. 1 QFP package structure

The second difficulty, faced to assess the reliability of a chip, is failure modeling. There are many methods [12] to model the failure of interconnection structure, such as model-based approaches and data-driven approaches. In this paper, a general Eyring model [13] is used to model the reliability of ISs subjected to random vibration under different temperature, considering the failure mechanism.

To investigate the effect of environmental loading and location of interconnection structure to failure of interconnection structure, a study is conducted, by applying narrow-band random vibration loading under three temperatures.

II. EXPERIMENT PROCEDURES

A. Experiment platform and test specimen

The combined vibration-temperature tester consists of DONGLING ES-6-230 shaker and THV402-5, which is used to apply vibration and temperature loading, showed as Fig. 2. This tester can provide maximum acceleration of 1000 m/s^2 and temperature from -65 to 150 ℃.

Figure 2 The combined vibration-temperature tester

A specimen is shown in Fig. 3. The chip is QFP100 with 0.5mm pitch, size of 14×14×1.4mm and SnPb solder. And the board size is 180×90×1.6mm. This specimen can monitor the status and failure of 16 pairs of pins in real time [11], by the online monitoring circuit.

Figure 3 A test specimen

B. Environment loading

Eighteen test specimens are subjected to the narrow-band random vibration under different temperature (-25, 25, 75℃) with a frequency range of 280 Hz to 320 Hz (the 1st natural frequency of specimens under -25, 25, 75℃ are 312, 301.6, 293.5 Hz, respectively), and a constant power spectral density 0.8 g^2/Hz. Each specimen is bolted to the holding equipment at the four corners (see Fig. 4). Each specimen is tested to failure.

Figure 4 The fixed mod of each specimen

C. The monitoring of specimens

Charging time can be used as the monitoring signal of IS state based on an external signal capacitor in real-time [11]. The IS monitoring circuit is shown in Fig. 5. Two ISs form a monitoring unit, one is tested IS, and the other is feedback IS. Then, the health status of tested IS would be tested in a charge-discharge circle, by controlling the voltage at the front of the tested IS. There are 16 IS pairs monitored in each specimen, and four at each side, which location is show in Fig. 6.

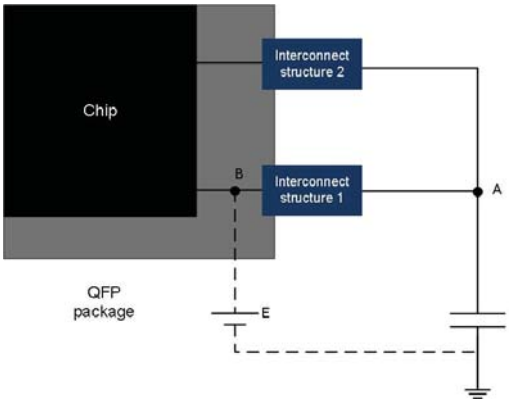


Figure 5 Interconnection structure monitoring circuit

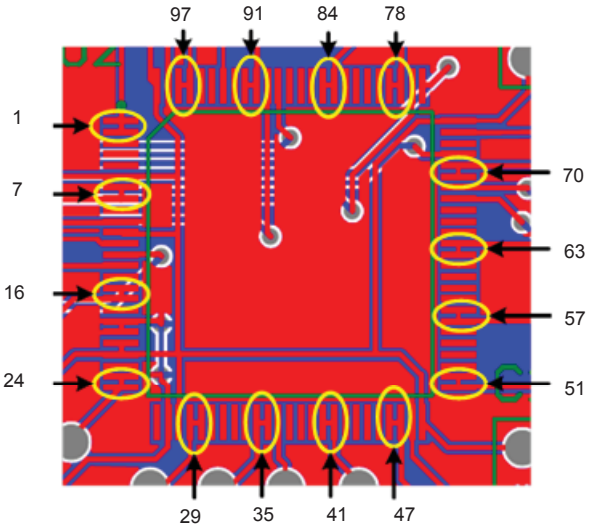


Figure 6 Location of monitored interconnects

From previous research [11], there is two performances in the charging time. Charging time may gradually become bigger or smaller, depended on the failure mode of the IS. So, the failure of interconnection structures is defined that the charging time exceed the high threshold value ζ_h or below the low threshold value ζ_l, and at the next 10% time the incident that exceed or below the threshold value happened at less 5 times. In this study, let $\zeta_h = 150ms$ and $\zeta_l = 10ms$.

III. The Coupled Failure Model

In 1986, McPherson [13] discussed the influence of stress on activation energy, and developed a generalized Eyring model. The form under the condition of high stress can be written,

$$(TTF)_{HS} = A\exp[-\gamma_0\xi]\exp[\frac{Q_0 - \gamma_1\xi}{K_B T}] \quad (1)$$

Where $Q_0 = \Delta H_0^* + \gamma_1\xi_B$, ξ is the external stress and ξ_B is the breakdown strength of the material. Equation (1) can be rewritten in follow form,

$$(TTF)_{HS} = A_1\exp[\gamma\xi]\exp[\frac{\beta}{T}] \quad (2)$$

Here $A_1 = A\exp(\frac{\gamma_1}{K_B T}\xi_B)$, $\gamma = -(\gamma_0 + \frac{\gamma_1}{K_B T})$ and $\beta = \frac{\Delta H_0^*}{K_B}$. It is known that parameters A_1 and γ are temperature dependent. The breakdown strength ξ_B parameter depends on the physics of failure, which depend on the grain size, impurity content, and surface passivation for a metallization. Normal distribution can be used to describe parameter ξ_B for the random effects. So, parameter A_1 obeys lognormal distribution. Therefore, in this paper, the lognormal distribution is used to model the time-to-failure under the same vibration and temperature, and an exponential distribution is used for different temperature.

The TTF of an interconnection structure under special condition is Lognormal distributed $\ln TTF \sim N(\mu,\sigma)$. Thus, the probability density function $f(t)$ of TTF is,

$$f(t) = \frac{1}{\sigma t\sqrt{2\pi}}\exp[-\frac{1}{2}(\frac{\ln t - \mu}{\sigma})^2] \quad (3)$$

And the mean value of TTF is,

$$E(T) = \exp(u + \frac{\sigma^2}{2}) \quad (4)$$

The reliability function $R(t)$ and failure rate function $h(t)$ of the interconnection structure are,

$$R(t) = P[T > t] = P[z > \frac{\ln t - \mu}{\sigma}] \quad (5)$$

$$h(t) = \frac{f(t)}{R(t)} = \frac{\phi(\frac{\ln t - \mu}{\sigma})}{t\sigma R(t)} \quad (6)$$

Interconnection structure on a circuit will suffer from different stress due to their different location. Referring to equation 2, different stress may cause TTF to follow an exponential distribution, which probability density function $f(t)$, reliability function $R(t)$ and failure rate function $h(t)$ are respectively,

$$f(t) = b\exp(\alpha t)\exp(-\int_0^t h(\tau)d\tau) \quad (7)$$

$$R(t) = \exp(-\int_0^t h(\tau)d\tau) \quad (8)$$

$$h(t) = b\exp(\alpha t) \quad (9)$$

Where b is constant $\exp(\alpha t)$ represents the increase of failure rate per unit time.

IV. Results and Discussion

A. Failure Analysis of Interconnection structures

After experiment, failure data are collected. There are 16 pairs interconnection structure monitored in a specimen. The stress on the interconnection structure will be different due to the different location, which could be called location-effect in a circuit board. Time-to-failure (TTF) of some interconnection structure under 75℃ are listed in Tab.1. Fig. 7 shows the fitting of each IS by lognormal distribution. It shows that the failure of those ISs are similar, which could be verified from the result under the scanning electron microscope (SEM) and simulation by ANSYS. Fig. 8 and Fig. 9 are the results of SEM and ANSYS, respectively.

TABLE. 1 FAILURE TIME OF INTERCONNECTION STRUCTURES

No. of IS	IS1(min)	IS7(min)	IS16(min)	IS24(min)
Specimen1	5.05	5.88	5.93	5.30
Specimen2	427.40	427.37	423.13	423.13
Specimen3	120.38	320.48	254.45	254.35
Specimen4	22.45	22.55	22.40	23.28
Specimen5	2.167	7.62	10.40	4.03
Specimen6	14.92	15.22	14.83	16.35

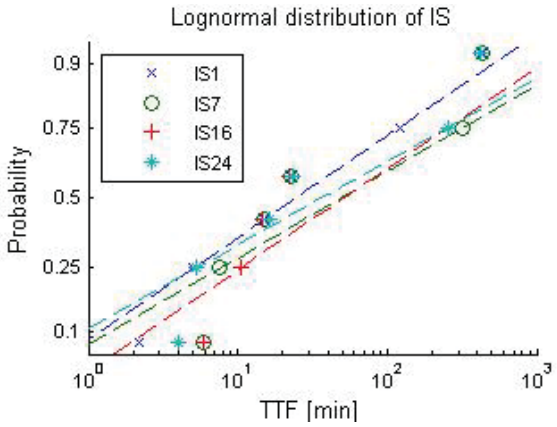
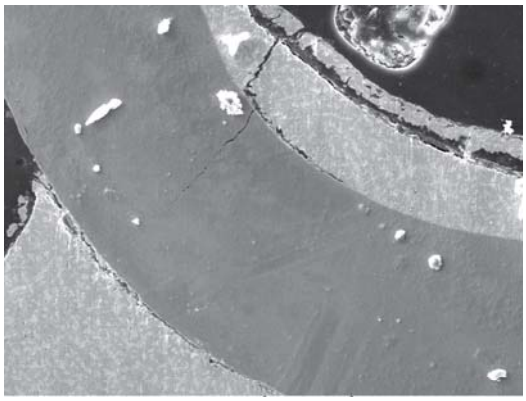
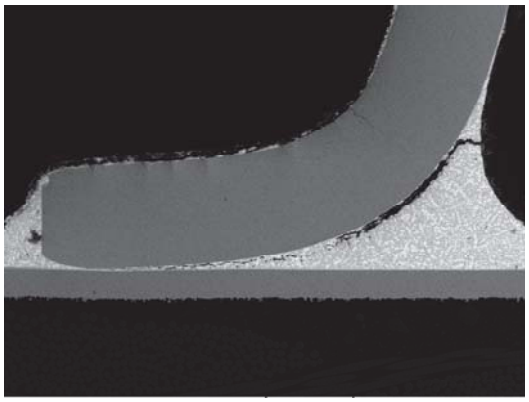


Figure 7 Time-to-Failure of IS under 75℃



(a) SEM of IS1



(b) SEM of IS24

Figure 8 SEM of IS1 and IS24

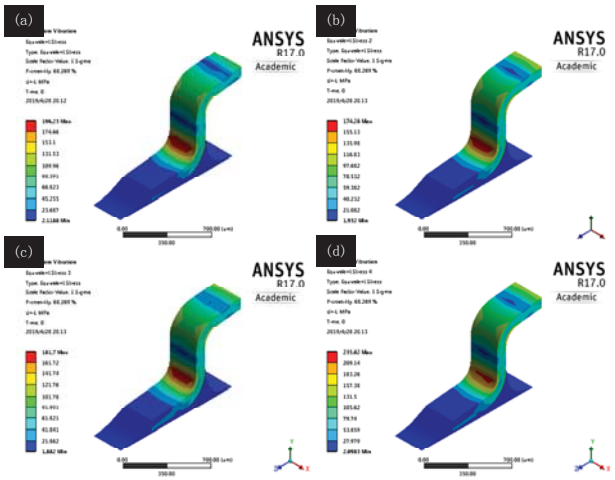


Figure 9 Stress contour from ANSYS: (a) IS1, (b) IS7, (c) IS16, (d) IS24

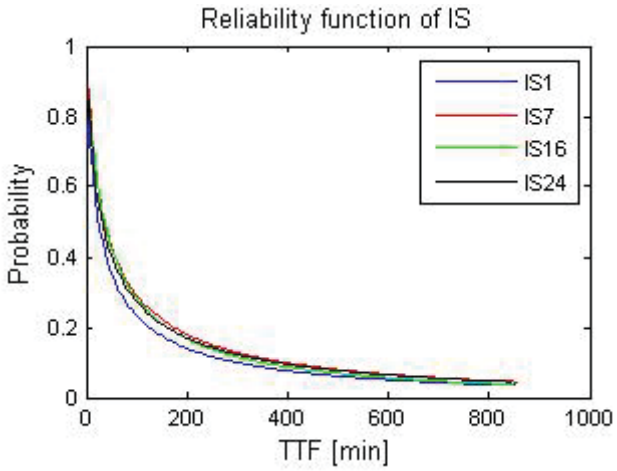


Figure 10 Reliability function of IS under 75℃

TABLE 2 TTF EXPECTANCY OF IS UNDER 75℃

ISs	IS1	IS7	IS16	IS24	IS29	IS35	IS41	IS47
TTF (min)	165	207	173	207	195	266	242	290
ISs	IS51	IS57	IS63	IS70	IS78	IS84	IS91	IS97
TTF (min)	350	277	91	223	206	225	215	369

TTF of Interconnection structures on a circuit board will be different due to their location, because of the fact that interconnection structures at different location suffer from different stress. Fig. 11 shows stress response of IS1, IS7, IS16 and IS24, calculated by ANSYS, in which the figure below is the supplement to the figure above. Tab.2 shows the TTF expectancy of different interconnection structure under 75℃. It can be concluded that interconnection structures inside each side may have higher life.

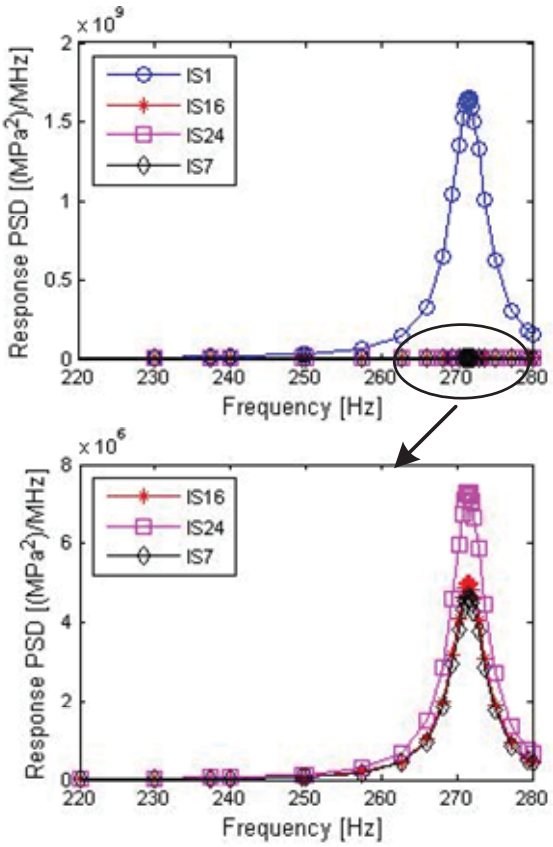


Figure 11 Stress response of IS1, IS7 IS16 and IS24.

B. Failure Analysis of Interconnection structures under different temperature

Failure, including the TTF and failure modes, of each IS under different temperature maybe different. Affected by the parameter A_1, the TTF of each IS could be modeled by a lognormal distribution. Fig. 12 shows the TTF of IS1 under different temperature. It shows that the reference line under 25℃ and 75℃ are parallel, while the reference line under -25℃ is more steeper comparing the others, which indicates that the failure modes under 25℃ and 75℃ are same, while the failure modes under -25℃ are different from 25℃ and 75℃. Temperature affects the rate of crack propagation under narrow band random vibration, and IS has lower random-vibration reliability under lower temperature.

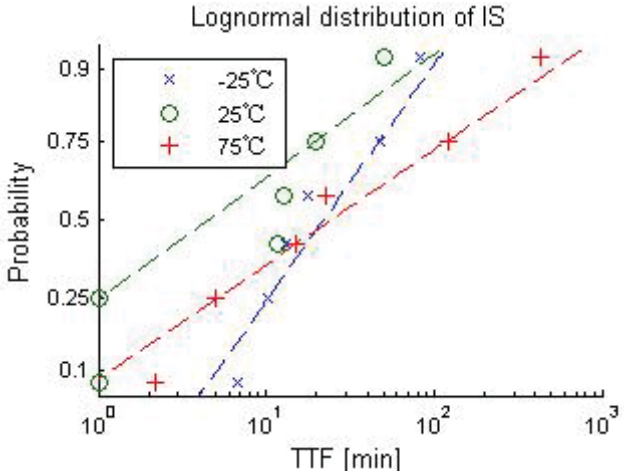


Figure 12 Time-to-Failure of IS1 under different temperature

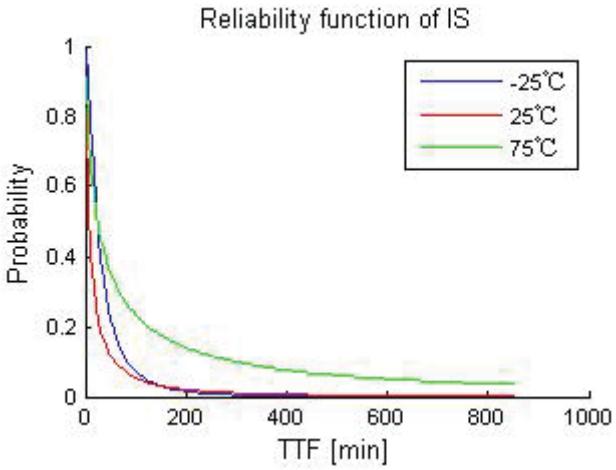


Figure 13 Reliability function of IS1 under different temperature

From the previous analysis, we known that the TTF of interconnection structure will be different due to their location. So, we suppose that difference in TTF of interconnection structures on a circuit board is only the result of their location. Therefore, it can be obtained that an exponential distribution could be used to model the TTF of interconnection structures on a board from equation 2. Fig. 14 shows exponential distributions of interconnection structure on a board under different temperature. It shows the similar result with Fig. 11, which further validates the previous inference that temperature affects the rate of crack propagation, and that the failure modes under 25℃ and 75℃ are same, while the failure modes under -25℃ are different from 25℃ and 75℃.

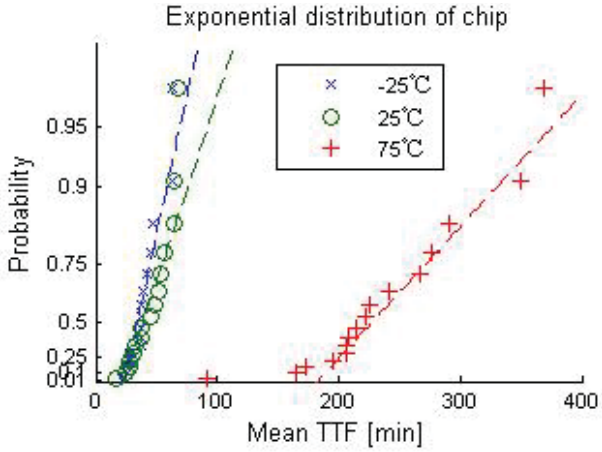


Figure 14 Mean Time-to-Failure of ISs on a chip under different temperature

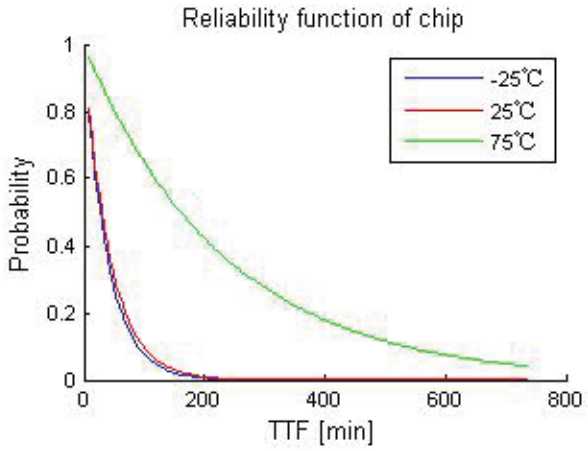


Figure 15 Reliability function of chip under different temperature

V. CONCLUSION

In this paper, the failure of QFP interconnection structures were studied under narrow-band random vibration, with power spectral density $0.8\ g^2/Hz$, and frequency from $280\ Hz$ to $320\ Hz$, at different temperature (-25℃, 25℃, 75℃). In the experiment, the charging time was used to monitor the health status and failure of interconnection structure. From the result of time-to-failure from experiment, ANSYS simulation and SEM, the effect of temperature and the location of interconnection structure were analyzed, combined with the failure physics model.

Results show that failure modes of each interconnection structure in a chip are similarly, while the crack growth rate of interconnection structure varies with their position, and the solder joint life of the four corners is lower than that of the interior of each column. For an interconnection structure, temperature affects the rate of crack propagation under narrow band random vibration, and interconnection structure has lower random-vibration reliability under lower temperature. Failure modes under 25℃ and 75℃ are same, which are different under -25℃. For a chip, reliability under -25℃ and 25℃ are close, which far below the reliability under 75℃.

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