Embedded Technology-based Diagnostic and Prognostics Method Of Electronic System

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***Abstract*—Electronic systems, consisted of analog circuits and digital circuits, is of great importance for being widely used in industrial products and military equipment. Occasionally glitches of electronic systems can be easy caused by defective design, heavy loads and sudden impacts. Unexpected system failures could result in considerable and unacceptable losses. To avoid such situation, detect abnormal system signals, diagnostic incipient faults and predict remaining useful life is drawing more and more attention. By improving signal collection system and analytic system, abundant signal details are extracted to diagnostic system faults. With electronic system topology and causality well considered, a fault indicator (FI) indicating systematic failures is developed from extracted electronic system signal features. Kinds of exploratory approaches were attempted to figure out diagnostic and prognostic problems of DC power convert devices, digital process devices and analog circuits respectively. Compared to the traditional way, solving these puzzles with a complex mathematical model base on input/output signals, electronic system states and transfer function analysis, tiny but effective methods based on embedded technology are presented in this paper. Moreover, a power conversion efficiency based model is developed, and analysis procedure are exhibited.**

Keywords-embedded technology; diagnostic; fault indicator; mathematical model

I. INTRODUCTION

Electronic system is playing an increasingly important role in almost every fields such as space exploration, national defense and industrial manufacture. Electronic systems are often the first parts of these systems to fail[1]. The occurrence of circuit failures during field operation can affect system functionality, and the cost of failure can be enormous[2],[3]. Such unexpected failures in field working process usually leads to inestimable system crashes and unacceptable maintenance cost. Prognostics and health management (PHM) is a repertoire techniques and methodologies that enables the assessment of system reliability during field operation so as to determine the advent of failure and mitigate system risks[4].

PHM derive from the U.S. Department of Defense (DoD). The motivation is to reduce the operation and support (O&S) costs of large military or industrial systems while maintaining or increasing the availability of these systems[5]. In most cases implement PHM in electronic system means monitor abnormal signals and behaviors of the system, perform signal analysis to diagnose early anomalies and predict possible system failure through system architecture based mathematical models. While the above method is very effective for implementing prognostic and health management in analog circuits and small-scale electronic system, it becomes impractical to implement PHM strategies to diagnosing potential anomaly and predicting possible failure for analog-digital-mixed system and large-scale electronic system.

For the purpose of facilitate diagnostic and prognostics, it is necessary to acquire kinds of signals of the electronic system accurately in real time. And degradation mechanisms of major circuits and components must be studied to support modeling work and optimization. However, degradation in electronics is difficult to detect and analyze due to the complex architecture of electronic systems, the interdependency of system components, and the miniaturization of electronic devices[6]. Futhermore, the limited computing resource and layout space of electronic system hinder the PHM technology reaching its optimum performance.

This paper provides a Embedded technology-based method in solving fault diagnostic and failure prognostics of electronic system. Viewing intact electronic system as

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decomposed circuits, performing fault diagnostic and failure prognostics respectively, and partial PHM results can be merged to obtain whole-system-level health status.

This paper is organized as follows. Section 2 presents the proposed embedded health assessment approach of each subsystem. Section 3 describes the detail implementation and data analysis approach for power convert circuit. Section 4 concludes the paper.

II. Embedded Technology Based Health Assessment Approach

In order to assess the health status of electronic system, this paper have developed probe-type signal acquisition and fault injection platform. The platform can realise accurate signal acquisition and fault analysis. The electronic system is divided into several subsystems, such as power convert circuit, analog-digital convert circuit, and information processing circuit. After analysing signal features and diagnosing potential fault of each subsystem, system level PHM approach is achieved.

A. Probe-type Signal Acquisition and Fault Injection Platform

Due to the compact structure and high intergration density of the electronic system, it is quite annoying to collect signals on the pins of critical components. And the size of the pins could be too small to conduct direct testing. Futhermore, the quantity of the pins to be tested simultaneously is 2 or 3 orders of magnitude. To test some signal, the frequency of sampling signal must be at least as twice as the original signal frequency. These conditions is not easily satisfied, which not only requires higher sample performance, but also puts forward great information processing ability.

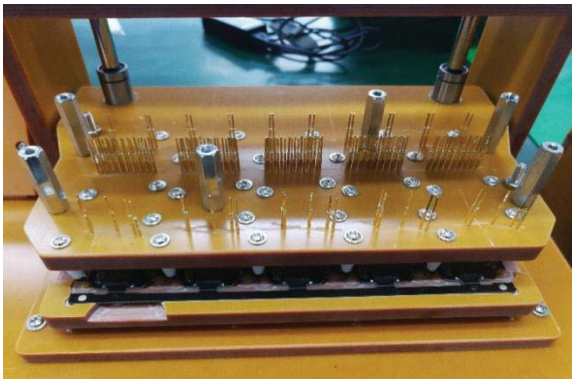

Figure 1. Probe-type Signal Acquisition and Fault Injection Platform

The probe-type signal acquisition and fault injection device is shown in figure 1. Metal probes are embedded in the lifting platform, which is fixed by five Φ5 screws and thirty Φ3 screws, and the lifting platform must be kept critical parallel with the electronic system motherboard. Precision linear rail system supports the lifting platform through the entire testing process. Once the lifting platform drop in place, the probes are connect to the test points exactly.

This paper has developed an edge computing device base on Xilinx ZYNQ all programmable embedded technology, of which the sample rate is up to 200MHz, and the sample channel is up to 16. Besides, the device also provides fault injection ability by generating different signals such as sine waveform, step waveform, and exponential waveform. Its frequency and phase ban be adjusted precisely through the control panel.

B. Power Convert Circuit

In this paper power convert circuit refers to DC/DC power supply circuit of electronic system. The stability of voltage and current outputted by power convert circuit is the fundamental mechanism to ensure that the system works correctly. For long time consistent ongoing, the power convert circuit degrade performance inevitably. Traditionally, simulation-before-test (SBT) strategies are carried out to diagnose faults in circuits[7-11]. However, only simulation analysis is insufficient for its lack of the analysis of the continuously stresses.

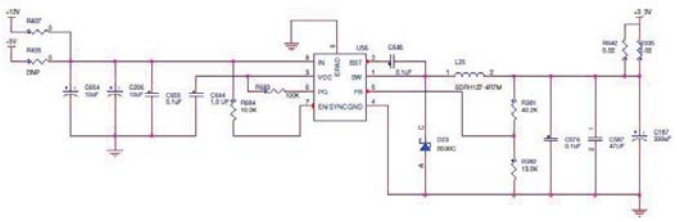

Figure 2. 5V-3.3V power convert circuit

In this experiment, 5V-3.3V power convert circuit has been tested for 20 continuous days in 105℃ temperature test chamber. Both input and output voltage and current data has been continuously collected under 10MHz sample rate. The ripple of output voltage and energy transforming efficiency has been caculated as the fault indicator to figure out the degradation process of the power convert circuit.

C. Analog-Digital Convert Circuit

Analog-to-Digital convert circuit is like the eyes of electronic system. Its correct conversion enable electronic system obtain accurate information. Once deviation occur in analog-to-digital conversion, it gets bigger and bigger along with the computing process and may causes serious problems.

Analog device drifts gradually and inevitably. It is possible to calibrate the analog-digital convert circuit with standard voltage and regression algorithm. Fixed standard voltage reflect the offset of the electronic system and

regression algorithm standardize the convert value of the sensors.

In the experiment, a on-chip 2.5V standard voltage is introduced into the analog-digital convert circuit through a multiplexer, and a third order regression function is used to decrease the nonlinear errors.

D. Information Processing Circuit

Information processing circuit is pure digital system. Information process ICs, such as ARM, FPGA, and DSP, is beyond diagnostic and prognostics for its severe manufacturing technologies and strictly confidential design. There is no obvious detectable signals indicating the degradation of digital components, and traditional PHM strategy won't work in this situation.

To address PHM on digital components, benchmark, which is originally developed to compare of different computer architectures, could be introduced to evaluate the performance indicators of the processors.

This paper introduce coremark to assess the ability of the ARM microcontroller in the electronic system. Coremark implement the kinds of algorithms, such as list processing (find and sort), matrix manipulation (common matrix operations), state machine (determine if an input stream contains valid numbers), and CRC (cyclic redundancy check). Coremark is designed to run on ICs from 8-bit microcontrollers to 64-bit microprocessors. Coremark has specific run and reporting rules, and conclude a single number as benchmark score. It is quite portable to deploy coremark and intuitional to compare the status of the microcontroller periodically.

III. Implementation and Data Analysis

In this section, we demonstrate the feature selection and the diagnostic and prognostic approach of a power convert circuit.

A. mRMR Criteria

Minimum redundancy maximum relevant criteria (mRMR) is a feature selection method based on mutual information. The method chooses the best feature set according to the maximum statistical dependence principle, which can effectively reduce the noise component in the sample, reduce the feature dimension, and improve the efficiency and accuracy of fault identification. The purpose of feature selection is to find m features which have the greatest correlation with the target class and the least redundancy among them from the feature space. We assume that the probability density and joint probability density of two random variablesare $p(x)$, $p(y)$ and $p(x,y)$. The Mutual information is defined as:

$$I = \int p(x,y)\log\frac{p(x,y)}{p(x)p(y)}dxdy \tag{1}$$

Based on mutual information, we can define the minimum redundancy and the maximum correlation between features and class labels. The use of mutual information (MI) is used to measure the degree of similarity between features. The calculation formula (2) gives the minimum redundancy criteria:

$$\min_{E\subset S}\frac{1}{|E|^2}\sum_{i,j\in E} I(f_i, f_j) \tag{2}$$

Here, $|E|$ is the number of features in the feature subset E to be searched; $I(f_i, f_j)$ is the mutual information between feature f_i and f_j , which represents the similarity between the two features; feature space S contains all the alternative features.

The maximum correlation criterion is given by the following formula.

$$\max_{E\subset S}\frac{1}{|E|}\sum_{i\in E} I(c, f_i) \tag{3}$$

Here, $I(c_i, f_i)$ represents the correlation between the feature f_i and the target class $c=\{c_k\}$.

By optimizing the result of formula (4) or formula (5), the feature subset of mRMR can be obtained.

$$\max_{E\subset S}\left\{\sum_{i\in E} I(c, f_i)\Big/\frac{1}{|E|}\sum_{i,j\in E} I(f_i, f_j)\right\} \tag{4}$$

$$\max_{E\subset S}\left\{\sum_{i\in E} I(c, f_i)-\frac{1}{|E|}\sum_{i,j\in E} I(f_i, f_j)\right\} \tag{5}$$

Using the above mRMR algorithm to analyze the parameters of power convert circuit, a specific quantization value can be obtained for each information. The higher the quantization value is, the more important the feature is. Therefore, the feature with high score can be selected as the feature parameter, and the other unimportant features can be discarded, so the most meaningful feature is energy transforming efficiency.

B. Energy Transforming Efficiency

The energy transforming efficiency stand for the ability that the power convert circuit to perform energy conversion. Higher transforming efficiency means better status. With continuously working, the energy transforming efficiency drop gradually.

For power convert circuit, energy transforming efficiency drops meas sustain more voltage, consume more power and generate more heat. It also means something has changed inside the power convert device. This kind of change is inreversible.

In this experiment, the convert efficiency of the 5V-3.3V convert circuit decreased 0.3 percent in no more than 20 days. The convert efficiency change as shown in figure 3.

105 centigrade is the only accelerated stress in this case. We can figure out the acceleration coefficient by honor the standard of GJB-299-C.

By increasing the quantity of the experimental samples, the exact acceleration coefficient can be figure out. And we can deduce the degradation coefficient of the power convert circuit at normal temperature. And base on it, the degradation model of the power convert circuit is built.

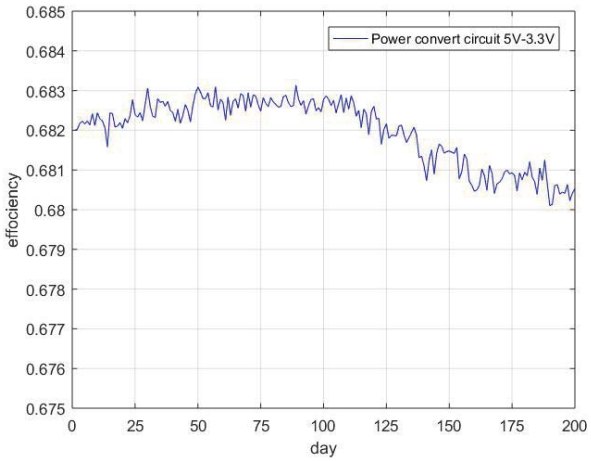

Figure 3. 5V-3.3V energy transforming efficiency

IV. CONCLUSION

PHM methods for complex electronic system have drawn great attention, but there is no widely accepted theory to solve the diagnostic and prognostic issue of complex electronic system. Traditional way is to establish the complicated mathematical model of a certain electronic system, while it is inefficient and hardly accurate.

In this paper, electronic system is split into power convert circuit, analog-digital convert circuit, and information processing circuit. And PHM approach is puts forward for each subsystem respectively. 5V-3.3V power convert circuit has detailed analyzed and a fault diagnostic and prognostic approach has been explained. This paper explored the method to carry out PHM on information process device with coremark testing.

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NOMENCLATURE

FI	fault indicator
DC	direct current
PHM	Prognostics and health management
DoD	Department of Defense
O&S	operation and support
SBT	simulation-before-test

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