An Online Monitoring Scheme of Output Capacitor's ESR for DCM Buck

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***Abstract*—Electrolytic capacitor is widely selected as output capacitor in DC-DC converter, while it has limited reliability. Monitoring the equivalent series resistance (ESR) is an effective method to diagnostic the output capacitor. In this paper, an online monitoring scheme of ESR is present for discontinuous conduction mode (DCM) Buck converters. Based on the output ripple voltage, the model of ESR is established. By sampling the output ripple voltage, the ESR is calculated using the sampled values. The proposed method reduces the current measurement and avoids the change of converter topology. The simulation and experimental results verify the effectiveness of the method.**

Keywords-component; Buck Converter; online monitor; electrolytic capacitor; equisvalent series resistance.

I. INTRODUCTION

The DC-DC converters are widely used in consumer electronics devices as power module. Due to large current and high voltage, the reliability of DC-DC converter is the area that needs to be focused. The degradation of output capacitor is the main reason of Buck converter failure. The equivalent series resistance (ESR) and the capacitance change with the evaporation of electrolyte [1-2]. Due to the change of ESR is more significance than capacitance, monitoring ESR is the main indicator for output capacitor health [3].

In order to estimate the ESR, many methods have been proposed. Those methods mainly include two types: online mode and offline mode. The offline mode should turn off the power module, and injects signal into output capacitor. By analyzing the response with external instrument, the ESR and C can be calculated according to the Discrete Fourier Transformation [4-5]. The offline mode need be done in non-work status and an external instrument which made it not convenience in practice.

The other way is online mode, which monitors the specific signal in Buck converter and constructs the calculation model. The traditional method measures the output voltage and the inductor current by inserting an inductance current sensor. In [6], Buiatti used the output voltage and inductor current to calculate the ESR and C. However, this method is not robust enough, it is sensitive to noise, and has a large variance in measurement results. In order to reduce the noise influence, the Kalman filter, FIR filter is used [7-8]. In [9], the recursive least square algorithm is used based on inductance current and output voltage. Since the inductance current sensor insert, the power efficiency is decrease. To remove the current sensor, Yao Kai et al [10] proposed a method by monitoring the output ripple voltage without current sensor. Although there are many methods to calculate ESR, those methods are focus on continuous conduction mode (CCM). In DCM, the duty cycle of pulse width changes under different resistance loads which make those methods are not suitable.

This paper presents an online monitoring scheme of output capacitor for DCM buck converter. In section II, the failure mechanism of electrolytic capacitor is introduced. Section III analyzes voltage ripple and found the ESR calculation model. The online monitoring scheme is introduced in section IV. The simulation and experimental results are shown in section V.

II. FAILURE MECHANISM

The electrolytic capacitor is composed of two aluminum foils with a dielectric oxide layer in electrolyte, as shown in Fig.1.

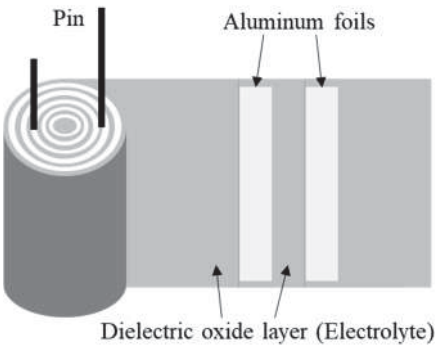

Figure 1. Aluminum electrolytic capacitor

Due to some non-ideal reason, an electrolytic capacitor can be expressed as a capacitor and a series resistor under low frequency, as show in Fig.2. The series resistor is the ESR of the electrolytic capacitor.

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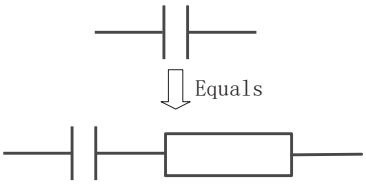

Figure 2. Equivalent circuit of electrolytic capacitor

The alumina medium undergoes a corresponding chemical reaction at the anode and cathode to maintain a dynamic balance of thickness. With the electrolyte evaporating, the chemical reaction is not equivalent. The ESR is continuously increased, and the equivalent capacitance is decreased. When the equivalent capacitance and the ESR are far from the initial value, the DC-DC converter will failure.

Based on (1), the ESR is the key indicator for electrolytic capacitor health. When the ESR_t is the twice of the initial value, the capacitor can be evaluated invalid.

$$\left(\frac{Vol_t}{Vol_0}\right)^2 = \frac{ESR_0}{ESR_t} \tag{1}$$

Where ESR_0 and ESR_t are the ESR at initial time and time t, Vol_0 and Vol_t are the volume of the electrolyte at initial time and time t.

III. Calculation Mode for ESR

Buck converter is the most common used DC-DC converter. Fig.3 shows the buck converter circuit. The electrolyte capacitor is selected as output capacitor and expressed as one resistance R_{ESR} and a capacitor C.

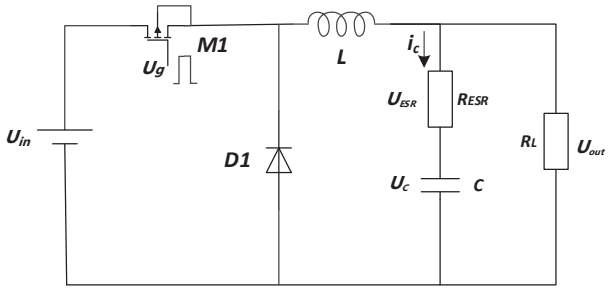

Figure 3. Buck converter

Under DCM, the M1 switches on between $[0, D_1T_S]$. Ts is the switch cycle. The diode D1 turn off. The inductor current increases with the rate of $(\mathrm{U_{in}} - \mathrm{U}_o)/L$. When the M1 switches off and D1 is on, the inductor current decrease with the rate of $-\mathrm{U_o/L}$. When the inductor current is zero, the inductor gets into intermittent state. In one cycle, the inductor current can be expressed as:

$$i_L(t) = \begin{cases} \frac{U_{\mathrm{in}}-U_o}{L}t, & 0 \le t < D_1T_S \\ \frac{-U_o}{L}t + \frac{U_o(D_1+D_2)T_S}{L}, & D_1T_S \le t < (D_1+D_2)T_S \\ 0, & (D_1+D_2)T_S \le t < T_S \end{cases} \tag{2}$$

where U_o is the mean values of output voltage, U_{in} is the input voltage, L is the inductance, T_S is switching cycle, t is the sample time. D_1 and D_2 is the duty cycle and intermittent time of diode current.

The capacitor current is obtained by the inductor current subtracting the mean value of output current, expressed as:

$$I_O = \frac{1}{T_S}\int_0^T i_L\, dt = \frac{U_oD_2(D_1+D_2)}{2L}T_S \tag{3}$$

Based on (2) and (3), the capacitor current is:

$$\mathrm{i_c(t)} = \begin{cases} \frac{\mathrm{U_oD_2}}{\mathrm{LD_1}}\mathrm{t} - \frac{\mathrm{U_oD_2(D_1+D_2)}}{2\mathrm{L}}\mathrm{T_S}, & 0 \le \mathrm{t} < \mathrm{D_1T_S} \\ \frac{-\mathrm{U_o}}{\mathrm{L}}\mathrm{t} + \frac{\mathrm{U_o}}{\mathrm{L}}(\mathrm{D_1}+\mathrm{D_2})\mathrm{T_S} & \\ -\frac{\mathrm{U_oD_2(D_1+D_2)}}{2\mathrm{L}}\mathrm{T_S}, & \mathrm{D_1T_S} \le \mathrm{t} < (\mathrm{D_1}+\mathrm{D_2})\mathrm{T_S} \\ -\frac{\mathrm{U_oD_2(D_1+D_2)}}{2\mathrm{L}}\mathrm{T_S}, & (\mathrm{D_1}+\mathrm{D_2})\mathrm{T_S} \le \mathrm{t} < \mathrm{T_S} \end{cases} \tag{4}$$

The ESR voltage is:

$$u_{\mathrm{ESR}}(t) = R_{\mathrm{ESR}}.i_c(t) = \begin{cases} R_{\mathrm{ESR}}\left[\frac{U_oD_2}{LD_1}t - \frac{U_oD_2(D_1+D_2)}{2L}T_S\right], & 0 \le t < D_1T_S \\ R_{\mathrm{ESR}}[\frac{-U_o}{L}t + \frac{U_o}{L}(D_1+D_2)T_S & \\ -\frac{U_oD_2(D_1+D_2)}{2L}T_S], & D_1T_S \le t < (D_1+D_2)T_S \\ R_{\mathrm{ESR}}\left[-\frac{U_oD_2(D_1+D_2)}{2L}T_S\right], & (D_1+D_2)T_S \le t < T_S \end{cases} \tag{5}$$

The relation between $u_c(t)$ and $i_c(t)$ is:

$$u_c(t) = U_C(t_0) + \frac{1}{C}\int_{t_0}^{t} i_C\, dt = \begin{cases} U_C(0) + \frac{t^2D_2U_o}{2LCD_1} - \frac{tT_SD_1D_2U_o}{2LC} & \\ -\frac{tT_SD_2^2U_o}{2LC}, & 0 \le t < D_1T_S \\ U_C(D_1T_S) - \frac{t^2U_o}{2LC} + \frac{tT_SD_1U_o}{LC} - \frac{{T_S}^2D_1^2U_o}{2LC} + \frac{tT_SD_2U_o}{LC} & \\ -\frac{tT_SD_1D_2U_o}{2LC} - \frac{{T_S}^2D_1D_2U_o}{LC} + \frac{{T_S}^2D_1^2D_2U_o}{2LC} - \frac{tT_SD_2^2U_o}{2LC} & \\ +\frac{{T_S}^2D_1D_2^2U_o}{2LC}, & D_1T_S \le t < DT_S \\ U_C(DT_S) - \frac{T_SD_2}{2LC}[(D_1+D_2) & \\ \big(t - T_S(D_1+D_2)\big)U_o], & DT_S \le t < T_S \end{cases} \tag{6}$$

where: $D = D_1 + D_2$, $U_C(0)$, $U_C(D_1T_S)$ and $U_C(DT_S)$ is the capacitor voltage at begin time, D_1T_S and DT_S.

Based on (6), the capacitor voltage is

$$U_C(D_1T) = U_C(0) + \frac{T^2D_1D_2U_o - T^2D_1^2D_2U_o - T^2D_1D_2^2U_o}{2CL} \tag{7}$$

$$U_C(DT) = U_C(0) - \frac{T^2D_1^2U_o + T^2D_1D_2U_o + T^2D_1D_2(D_1+D_2)U_o}{2CL} + \frac{T^2(D_1+D_2)^2U_o}{CL} - \frac{T^2D_2^2(D_1+D_2)U_o}{2CL} - \frac{T^2(D_1+D_2)^2U_o}{2CL} \tag{8}$$

The mean of output voltage U_o is:

$$U_o = \frac{1}{T_S}\int_0^{T_S} u_C(t)\, dt + \frac{1}{T_S}\int_0^{T_S} u_{\mathrm{ESR}}(t)\, dt \tag{9}$$

From (9), the capacitor voltage $U_C(0)$ at begin time is calculated.

$$U_C(0) = \frac{U_o}{12CL}(12CL + 4T_S{}^2D_1^2D_2 - 3T_S{}^2D_2^2 + 2T_S{}^2D_2^3 + 3T_S{}^2D_1D_2(-1+2D_2)) \quad (10)$$

The output voltage $u_O(t)$ is the sum of $u_c(t)$ and $u_{\mathrm{ESR}}(t)$. The alternating voltage can be expressed as:

$$\tilde{u}_o(t) = u_O(t) - U_o = u_c(t) + u_{\mathrm{ESR}}(t) - U_o =$$

$$\begin{cases} A + \frac{t^2D_2U_o}{2LCD_1} - \frac{tT_SD_1D_2U_o}{2LC} - \frac{tT_SD_2^2U_o}{2LC} \\ +R_{\mathrm{ESR}}\left[\frac{U_oD_2}{LD_1}t - \frac{U_oD_2(D_1+D_2)}{2L}T_S\right] - U_o, 0 \le t < D_1T_S \\ \mathrm{A} + \frac{T_S{}^2D_1D_2U_o}{2CL} - \frac{T_S{}^2D_1^2D_2U_o}{2CL} - \frac{T_S{}^2D_1D_2^2U_o}{2CL} - \frac{t^2U_o}{2LC} \\ + \frac{tT_SD_1U_o}{LC} - \frac{T_S{}^2D_1^2U_o}{2LC} + \frac{tT_SD_2U_o}{LC} - \frac{tT_SD_1D_2U_o}{2LC} \\ - \frac{T_S{}^2D_1D_2U_o}{LC} + \frac{T_S{}^2D_1^2D_2U_o}{2LC} - \frac{tT_SD_2^2U_o}{2LC} + \frac{T_S{}^2D_1D_2^2U_o}{2LC} \\ +R_{\mathrm{ESR}}[\frac{-U_o}{L}t + \frac{U_o}{L}(D_1+D_2)T_S \\ - \frac{U_oD_2(D_1+D_2)}{2L}T_S] - U_o, D_1T_S \le t < \mathrm{D}T_S \\ \mathrm{A} - \frac{T_S{}^2D_1^2U_o}{2CL} - \frac{T_S{}^2D_1D_2U_o}{2CL} + \frac{T_S{}^2D_1(D_1+D_2)U_o}{CL} \\ + \frac{T_S{}^2D_2(D_1+D_2)U_o}{CL} - \frac{T_S{}^2D_1D_2(D_1+D_2)U_o}{2CL} - \frac{T_S{}^2D_2^2(D_1+D_2)U_o}{2CL} \\ - \frac{T_S{}^2(D_1+D_2)^2U_o}{2CL} - \frac{T_SD_2(D_1+D_2)(t-T_S(D_1+D_2))U_o}{2LC} \\ +R_{\mathrm{ESR}}\left[-\frac{U_oD_2(D_1+D_2)}{2L}T_S\right] - U_o, \mathrm{D}T_S \le t < T_S \end{cases} \quad (11)$$

where:

$$A = \frac{\left(12CL + 4T_S{}^2D_1^2D_2 - 3T_S{}^2D_2^2 + 2T_S{}^2D_2^3 + 3T_S{}^2D_1D_2\left(-1+2D_2\right)\right)U_o}{12CL} \quad (12)$$

At time 0 and D_1T_s, the alternating part of output voltage can be expressed as:

$$\tilde{u}_o(0) = \frac{U_o}{12CL}[3T_S{}^2D_1D_2\left(-1+2D_2\right) + 12CL + 4T_S{}^2D_1^2D_2 - 3T_S{}^2D_2^2 + 2T_S{}^2D_2^3] + R_{\mathrm{ESR}}\left[-\frac{D_2\left(D_1+D_2\right)U_o}{2L}T_S\right] - U_o \quad (13)$$

$$\tilde{u}_o\left(D_1T_S\right) = \frac{T_S{}^2D_1D_2U_o}{2CL} - \frac{T_S{}^2D_1^2D_2U_o}{2CL} - \frac{T_S{}^2D_1D_2^2U_o}{2CL} - U_o + R_{\mathrm{ESR}}\left[\frac{T_SD_2U_o}{L} - \frac{T_SD_2\left(D_1+D_2\right)U_o}{2L}\right] + \frac{U_o}{12CL}[12CL - 3T_S{}^2D_2^2 + 4T_S{}^2D_1^2D_2 + 2T_S{}^2D_2^3 + 3T_S{}^2D_1D_2\left(-1+2D_2\right)] \quad (14)$$

Based on (13) and (14), the ESR can be get:

$$R_{\mathrm{ESR}} = -L\left[\tilde{u}_o\left(0\right)\left(D_1-D_2\right)\left(2D_1+2D_2-3\right) + \tilde{u}_o\left(D_1T_S\right)\left(D_1+D_2\right)\left(4D_1+2D_2-3\right)\right] / \left[D_2T_SU_o\left(3D_2 - 2D_2{}^2 + 3D_1 - 9D_2D_1 + 3D_2{}^2D_1 - 7D_1{}^2 + 6D_2D_1{}^2 + 3D_1{}^3\right)\right] \quad (15)$$

where: $D_2 = \left(\frac{U_{in}}{U_O} - 1\right)D_1$.

Based on (15), the $\tilde{u}_o(0)$ and $\tilde{u}_o(D_1T_S)$ are needed to calculate ESR.

Base on the above analysis, the M1 gate control signal U_g, inductor current i_L, capacitor current i_C, capacitor voltage u_C, ESR voltage u_{ESR} and output voltage u_O is shown in Fig.4.

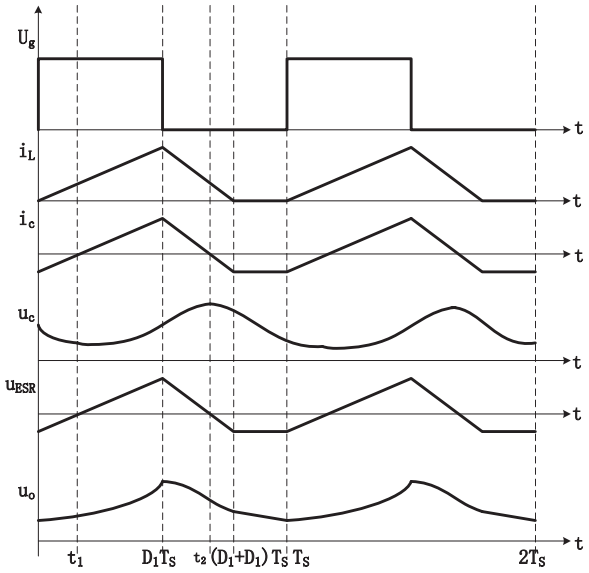

Figure 4. Signal under DCM

IV. Online Monitoring Scheme

As shown in Fig. 5, an online monitoring scheme is built to monitor the output capacitor ESR in DCM. The system consists of Buck circuit, isolation amplification module, sampling module, controller and calculation analysis module. The control signal is generated to control the switch status and trigger the sampling point. The Buck module realizes the DC-DC converter. The isolation amplification module amplifies the alternating part of output voltage. The ADC chip controlled by the trigger signal samples the amplified voltage signal. The calculation analysis module calculates the ESR by using the sampling voltage according to (15).

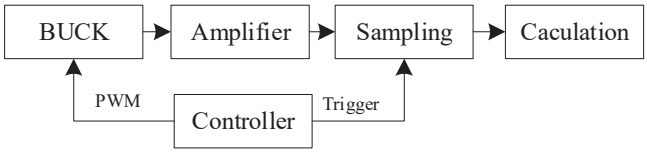

Figure 5. Online Monitoring Scheme

The isolation amplifier circuit is composed of an isolation circuit and an amplification circuit, as shown in Fig. 6. The isolation part consists of a transformer and a coupling capacitor for extracting the output ripple voltage from the Buck circuit. The amplification Part is the series-type composite amplifier circuit, amplifier op1 has low input offset voltage, low input

bias current, low noise performance and low input offset current to avoid introducing DC offset and noise interference in the ripple signal to be measured, amplifier op2 has a high gain bandwidth product to maintain high gain at the switching frequency, and the amplified signal is used for sampling.

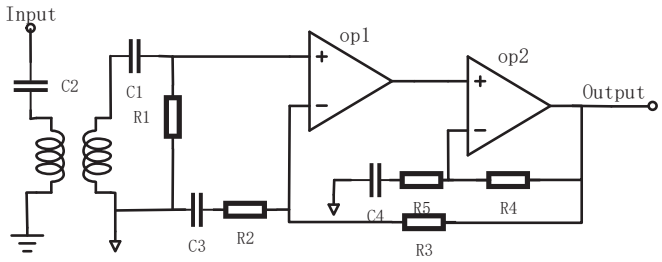

Figure 6. The isolation amplification module

According to (15), the sampling point is the state change point of the PWM single, so the trigger signal is generated based on the PWM signal. By the built monitoring system, the ESR of the output capacitor can be easily monitored.

V. EXPERIMENTAL

Buck simulation circuit is built using MATLAB, and changes the load resistance to make circuit into DCM. The condition of simulation model is that: input voltage: 30V, output voltage: 10V, inductance: 1mH, switching frequency: 10kHz, Output capacitance: 220uF, ESR: 168mΩ. The alternating part of output voltage is sampled at time 0 and D_1T_s. Based on (15), the ESR is calculated. The results are shown in Table I. The simulation results are close to the output capacitance simulation parameter setting values, which confirms the effectiveness of the proposed scheme.

TABLE I. SIMULATED ESR

Load(Ω)	D_1	D_2	$\tilde{u}_o(0)$(V)	$\tilde{u}_o(D_1T)$(V)	ESR(Ω)
50	0.27	0.53	-0.0476	0.0485	0.171
100	0.19	0.38	-0.0288	0.0415	0.169
500	0.08	0.17	-0.0072	0.0235	0.167
1000	0.06	0.12	-0.0039	0.0175	0.167
2000	0.04	0.08	-0.0021	0.0128	0.176

The Buck circuit is built and the monitoring prototype is built. The parameters of the switching power supply module are: output voltage 5V, MOS tube is Si7846, diode is SBRD10200, output inductance is 100uH, period is 25us (switching frequency 40kHz), output load 100Ω, the output capacitor is selected from electrolytic capacitors 56μF/50V, 100μF/50V and 330μF/50V and is used as the experimental object.

Using the built-in monitoring prototype, the ESR is calculated by equation (15). Table II shows the experimental results when the output capacitance is 56μF/50V.Using the LCR meter (HEWLETT 4284A), the ESR of the output capacitors of 56μF/50V at 40kHz is 190 mΩ. As shown in Table II, the calculated values are close to the LCR measured values.

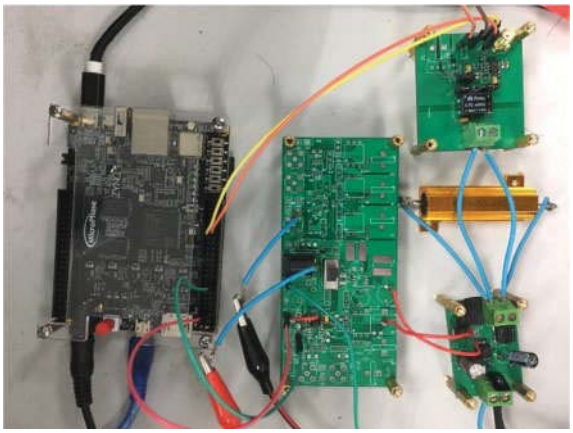

Figure 7. Online Monitoring System

TABLE II. ESR ESTIMATE FOR 56UF/50V

D_1	D_2	$\tilde{u}_o(0)(mV)$	$\tilde{u}_o(D_1T)$(mV)	ESR(Ω)
0. 2	0. 2175	-14. 1895	35. 7200	0. 1672
0. 3	0. 1836	-13. 0114	30. 9289	0. 1708
0. 4	0. 1552	-12. 7797	27. 8171	0. 1823
0. 7	0. 1036	-8. 7532	20. 0483	0. 1692
0. 8	0. 096	-7. 0478	16. 8745	0. 1728

To mimic the aging of the capacitor (56μF/50V), the capacitor is connected in series with a 500mΩ resistor. The output voltage of the switching power supply module is 10V with keeping the other experimental conditions unchanged. The output capacitor ESR is calculated using the built-in monitoring circuit. Table III shows the experimental results of the output capacitors 56μF/50V with series resistors. Using the LCR meter to measure the output capacitor 56μF/50V with the series resistors at 40 kHz, the ESR is 701mΩ.

By comparing with the calculated values given in Tables I-III, the calculated values are close to the measured values.

TABLE III. ESR ESTIMATE FOR 56UF/50V

D_1	D_2	$\tilde{u}_o(0)(mV)$	$\tilde{u}_o(D_1T)$(mV)	ESR(Ω)
0. 2	0. 2036	-100. 1431	300. 2248	0. 7396
0. 3	0. 1734	-99. 5299	250. 5620	0. 7290
0. 4	0. 1500	-99. 5299	216. 8404	0. 7265
0. 7	0. 1036	-75. 5232	115. 5661	0. 7259
0. 8	0. 0824	-58. 9975	105. 4425	0. 7332

VI. CONCLUSION

Electrolytic capacitor decay is an important cause of switching power supply failure. Online monitoring ESR is an effective way to reflect the status of aluminum electrolytic capacitor. This paper proposes a monitoring scheme of the ESR for Buck circuit. By deducing the ESR calculation equation, the method calculates the output voltage ESR by sampling the Buck circuit output ripple voltage under the trigger signal. In this paper, the monitoring scheme is designed and built. The proposed circuit structure is given which avoid change of circuit topology that can be widely used in practice.

ACKNOWLEDGMENT

This work was supported by The National Key Research and Development Program of China(2018YFB0407503), Fund of the Key Laboratory(JAB1728220).

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