Project - mini_cpu

디지털 논리회로

전기공학부

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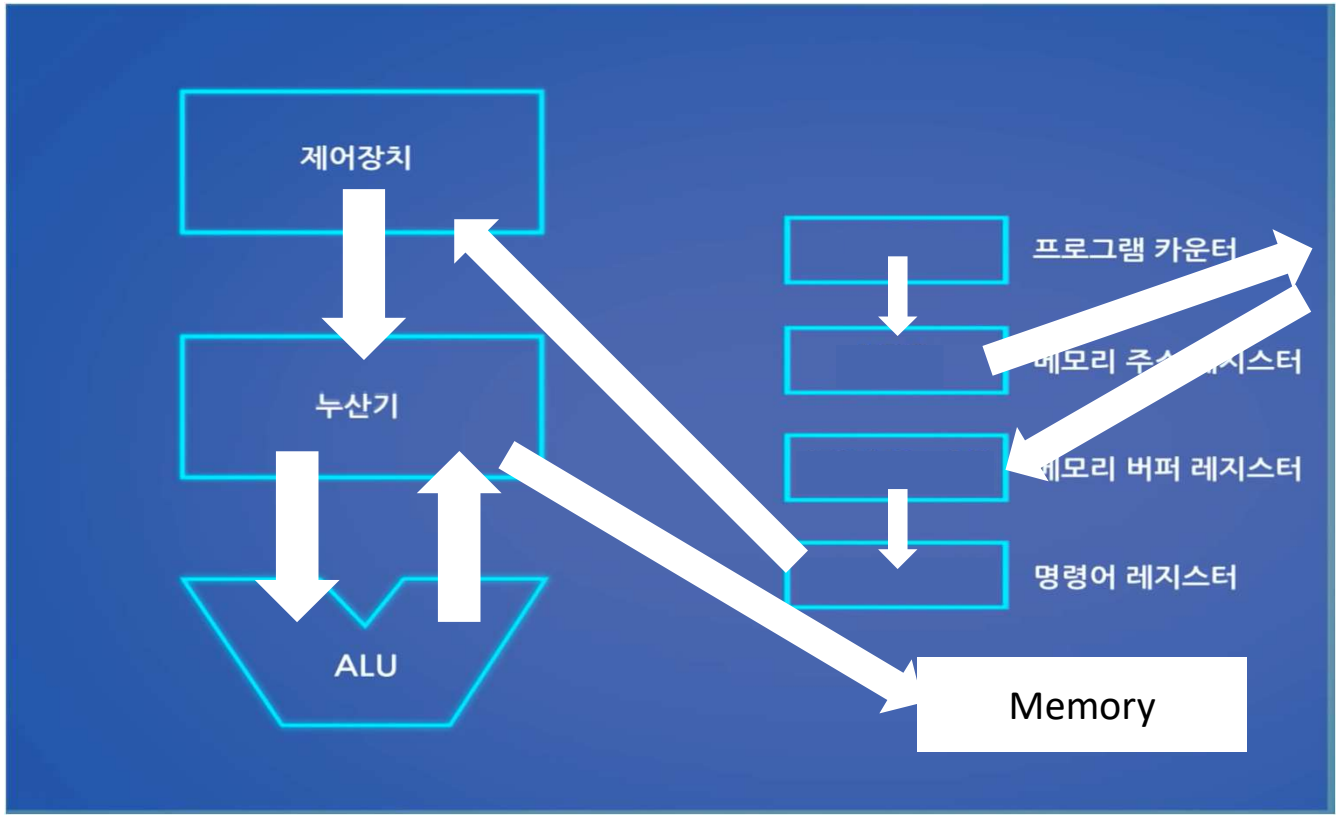
프로젝트 목표

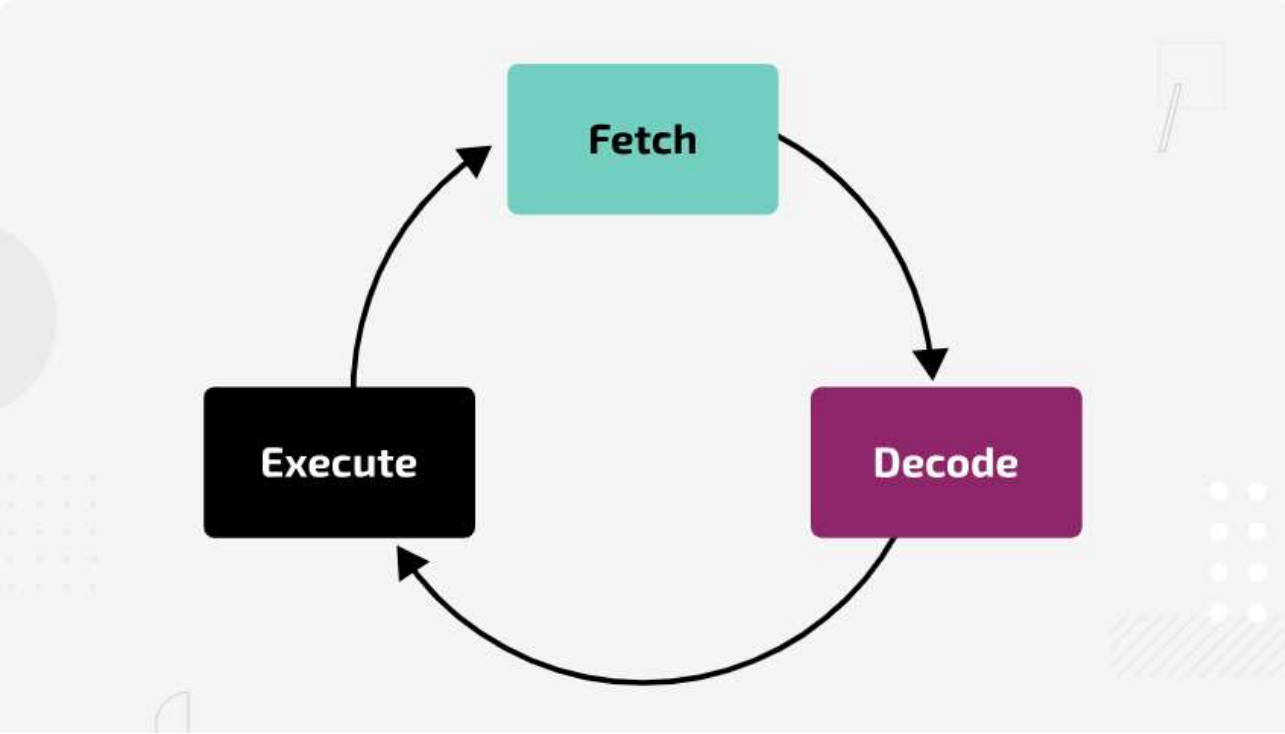
1. HDL(Hardware Description Language) 언어에 대한 이해를 높인다.
2. CPU의 동작 원리를 학습한다.
3. Verilog를 사용하여 간단한 ALU 동작을 구현하는 mini CPU를 설계한다.
4. Place&Route 과정을 통해 결과를 분석한다.

CPU 동작 원리

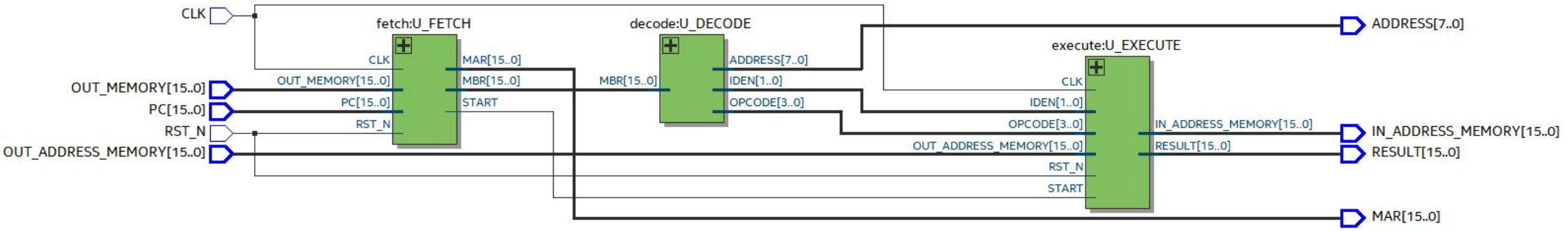


Memory

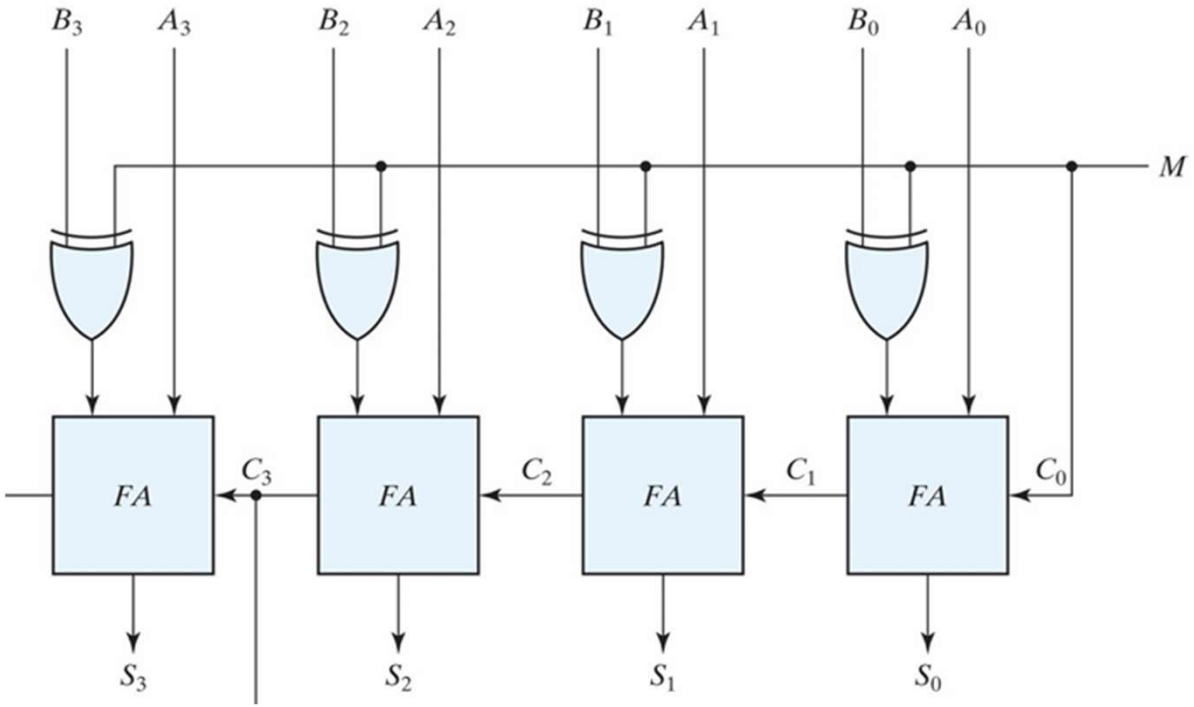
CPU 동작 원리



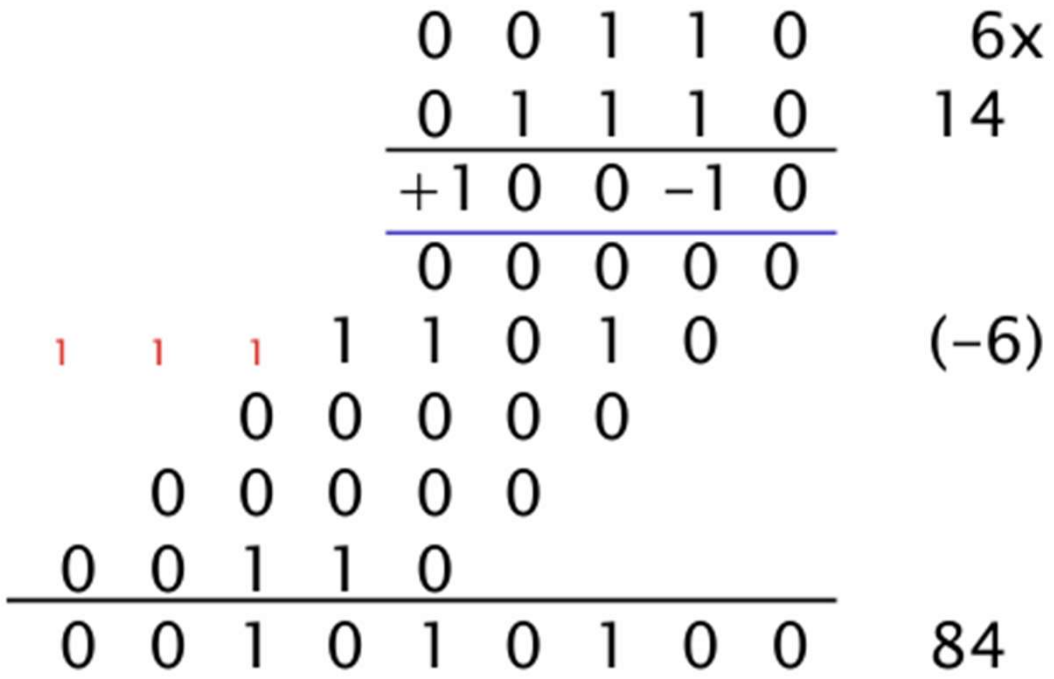
CPU RTL 회로도


CLK
OUT_MEMORY[15..0]
PC[15..0]
RST_N
OUT_ADDRESS_MEMORY[15..0]
fetch:U_FETCH
CLK
OUT_MEMORY[15..0]
PC[15..0]
RST_N
MAR[15..0]
MBR[15..0]
START
decode:U_DECODE
MBR[15..0]
ADDRESS[7..0]
IDEN[1..0]
OPCODE[3..0]
execute:U_EXECUTE
CLK
IDEN[1..0]
OPCODE[3..0]
OUT_ADDRESS_MEMORY[15..0]
RST_N
START
IN_ADDRESS_MEMORY[15..0]
RESULT[15..0]
ADDRESS[7..0]
IN_ADDRESS_MEMORY[15..0]
RESULT[15..0]
MAR[15..0]

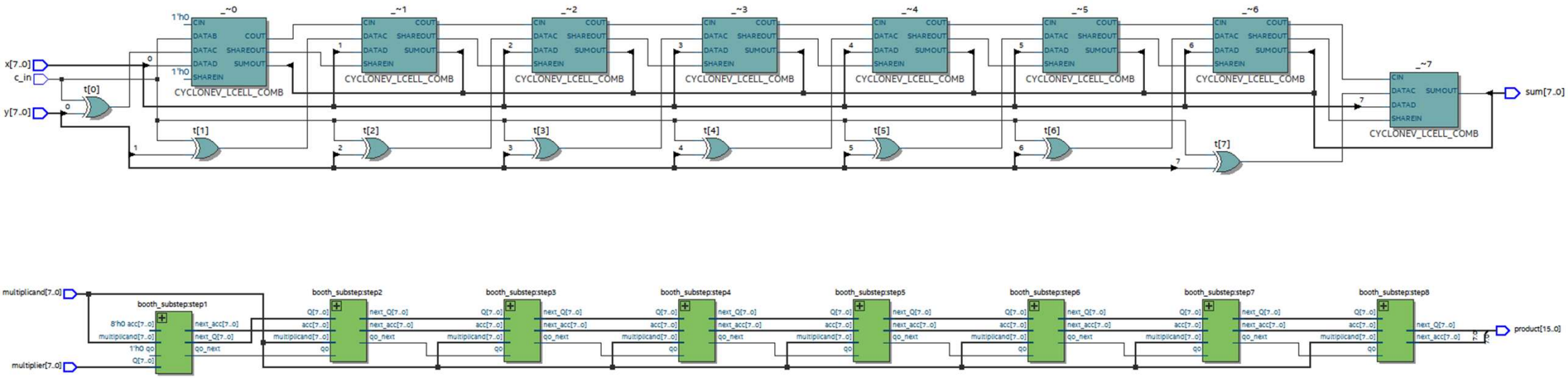
ADD_SUB



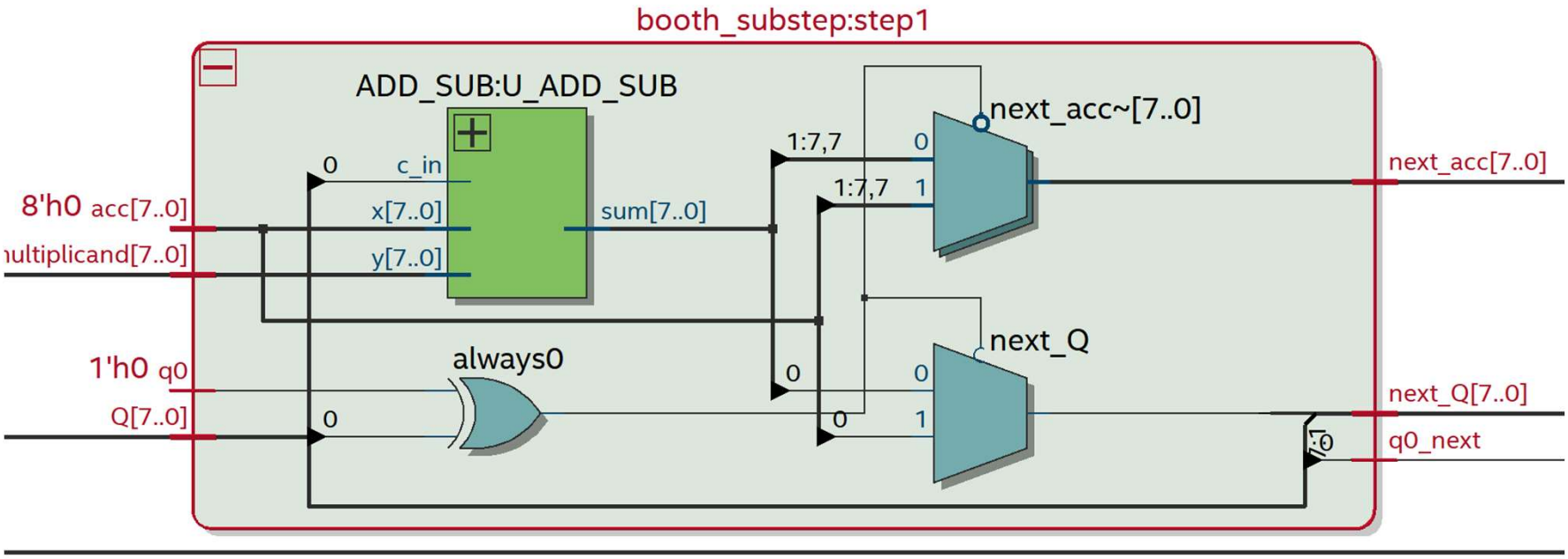
Booth_Mul


0 0 1 1 0 6x
0 1 1 1 0 14
+1 0 0 -1 0
0 0 0 0 0
1 1 1 1 1 0 1 0 (-6)
0 0 0 0 0
0 0 0 0 0
0 0 1 1 0
0 0 1 0 1 0 1 0 0 84

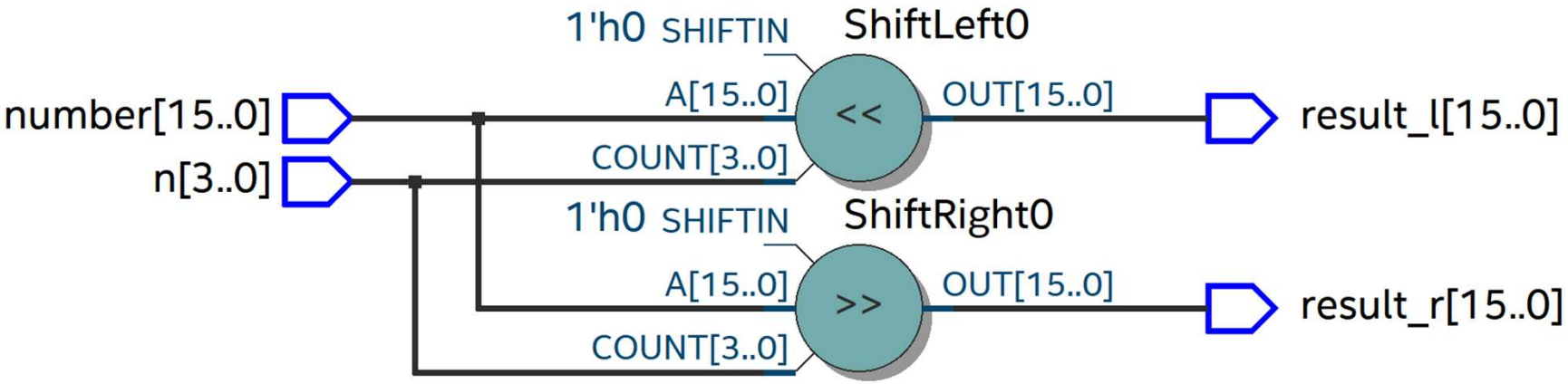
ADD_SUB/Booth_MUL



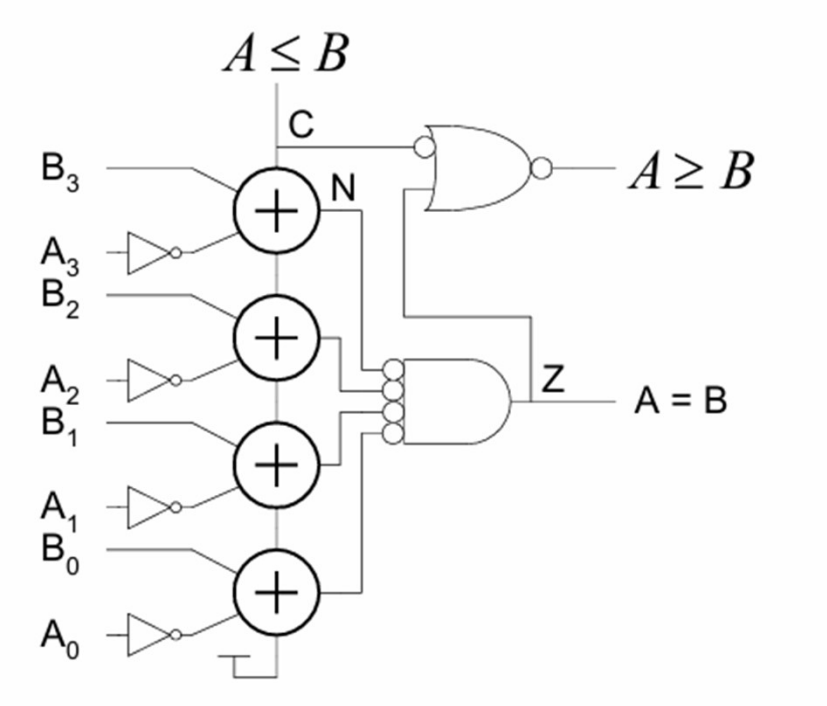
Booth_Sub


booth_substep:step1
ADD_SUB:U_ADD_SUB
c_in
x[7..0]
y[7..0]
sum[7..0]
8'h0 acc[7..0]
ultiplicand[7..0]
1'h0 q0
Q[7..0]
always0
1:7,7
1:7,7
next_acc~[7..0]
next_Q
next_acc[7..0]
next_Q[7..0]
q0_next

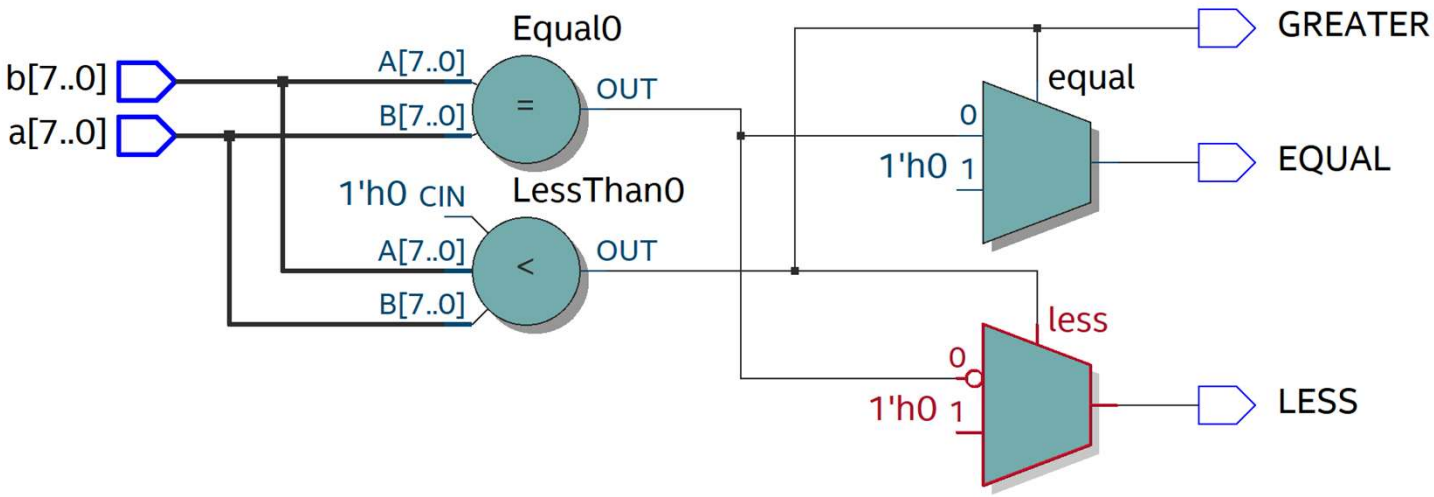
Barrel_Shifter



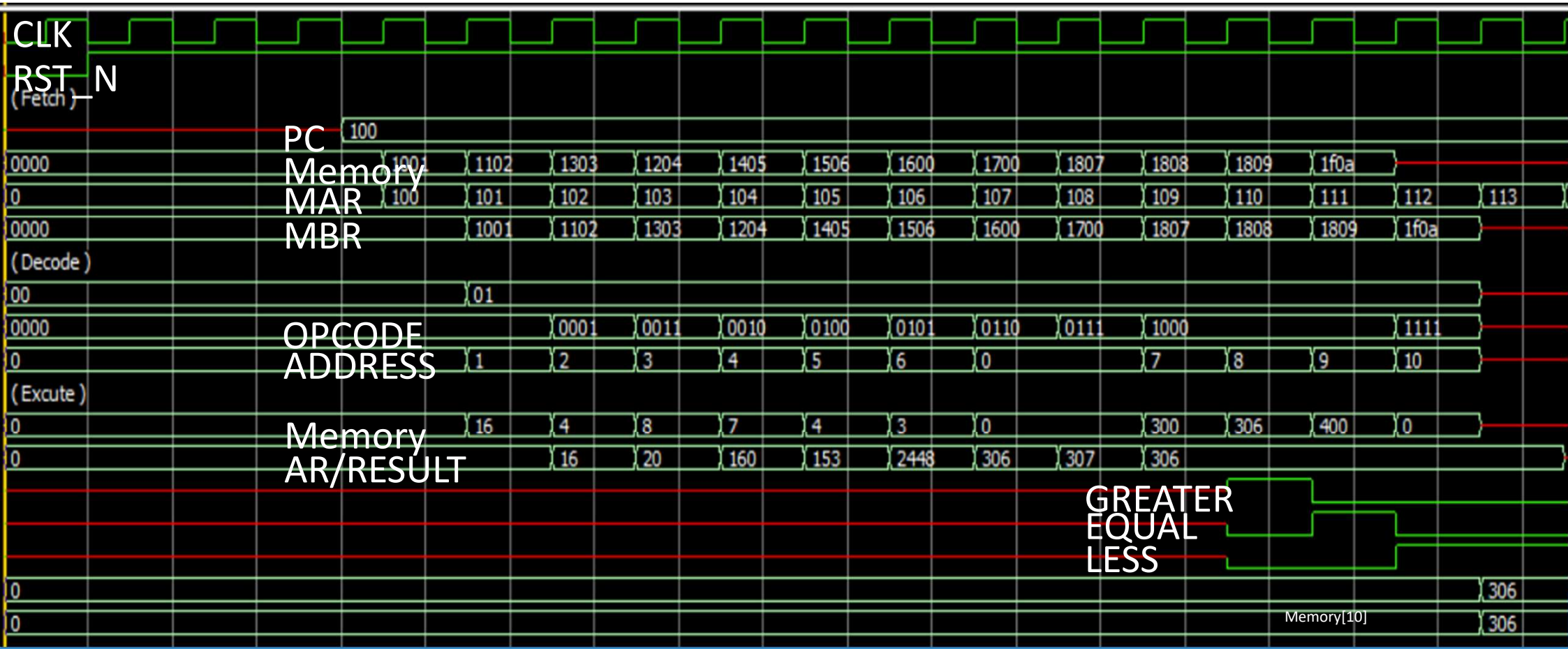
Comparator



Comparator


b[7..0]
a[7..0]
Equal0
A[7..0]
B[7..0]
=
OUT
1'h0 CIN
LessThan0
A[7..0]
B[7..0]
<
OUT
equal
0
1'h0 1
less
0
1'h0 1
GREATER
EQUAL
LESS

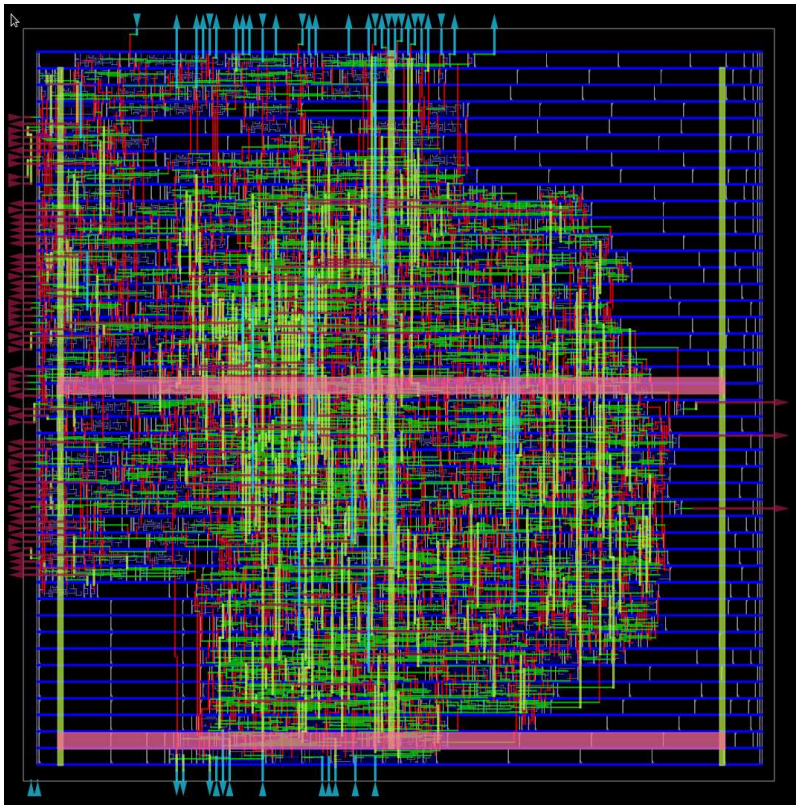
전체 **Simulation**



Result & Assembly

```
// instruction
mem[100] = 16'b0001_ mov.b  mem[1],ar   // ar = 16
mem[101] = 16'b0001_ add.b  mem[2],ar   // ar = 16 + 4 = 20
mem[102] = 16'b0001_ mul.w  mem[3],ar   // ar = 20 * 8 = 160
mem[103] = 16'b0001_ sub.w  mem[4],ar   // ar = 160 - 7 = 153
mem[104] = 16'b0001_ shl.w  mem[5],ar   // ar = 153 << 4 = 153 * 16 = 2448
mem[105] = 16'b0001_ shr.w  mem[6],ar   // ar = 153 >> 3 = 153 / 8 = 306
mem[106] = 16'b0001_ inc.w  ar          // ar = 306 + 1 = 307
mem[107] = 16'b0001_ dec.w  ar          // ar = 307 - 1 = 306
mem[108] = 16'b0001_ cmp.w  mem[7],ar   // great = 1
mem[109] = 16'b0001_ cmp.w  mem[8],ar   // equal = 1
mem[110] = 16'b0001_ cmp.w  mem[9],ar   // less = 1
mem[111] = 16'b0001_ mov.w  ar,mem[10]  // mem[10] = 306
```

Place & Route



```
================================================================
finish report_tns
----------------------------------------------------------------
tns 0.00

================================================================
finish report_wns
----------------------------------------------------------------
wns 0.00

================================================================
finish report_worst_slack
----------------------------------------------------------------
worst slack INF
```

Place & Route

```
============================================================================
finish report_power
----------------------------------------------------------------------------
Group                  Internal  Switching    Leakage      Total
                          Power      Power      Power      Power (Watts)
----------------------------------------------------------------------------
Sequential             3.09e-04   2.65e-04   7.43e-06   5.82e-04   3.4%
Combinational          8.69e-03   7.87e-03   4.32e-05   1.66e-02  96.6%
Clock                  0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.0%
Macro                  0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.0%
Pad                    0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.0%
----------------------------------------------------------------------------
Total                  9.00e-03   8.13e-03   5.06e-05   1.72e-02 100.0%
                          52.4%      47.3%       0.3%
============================================================================
finish report_design_area
----------------------------------------------------------------------------
Design area 2250 u^2 61% utilization.
[WARNING GUI-0076] QStandardPaths: XDG_RUNTIME_DIR not set, defaulting to '/tmp/runtime-root'
Elapsed time: 0:03.37[h:]min:sec. CPU time: user 1.98 sys 0.33 (68%). Peak memory: 195156KB.
```

역할 분담

- 한지윤 : 전반적인 CPU 설계 및 마무리, P & R 결과 분석.
- 전민태 : 자료 조사 및 ALU 기초 설계, 테스트 벤치 실행, P & R 결과 분석.
- 한주헌 : 자료 조사 및 보고서 초안 작성.

참고문헌

bRd 3D. "CPU는 어떻게 작동할까?" YouTube, 2021, https://www.youtube.com/watch?v=Fg00LN30Ezg&t=777s

https://github.com/The-OpenROAD-Project