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Assignment 9

1. $\frac{29.5*10^9 instructions}{1} * \frac{0.55\ cycles}{1\ instruction} * \frac{1\ second}{16*10^9 cycles} = 1.01\ seconds$

2. a. I1 Avg CPI = (3*0.25) + (4*0.25) + (1*0.5) = 2.25
   I2 Avg CPI = (2*0.25) + (2*0.25) + (4*0.5) = 3
   I1 Speed = $\frac{4*10^9 cycles}{1\ second} * \frac{1\ instruction}{2.25\ cycles} = 1.78 * 10^9 instructions/second$
   I2 Speed = $\frac{5*10^9 cycles}{1\ second} * \frac{1\ instruction}{3\ cycles} = 1.67 * 10^9 instructions/second$
   $\frac{1.78*10^9}{1.67*10^9} = 1.07\ or\ \frac{178}{167}$ I1 is 1.07 or 178/167 times faster than I2.

   b. I1 Avg CPI = (3*0.35) + (4*0.4) + (1*0.25) = 2.9
   I2 Avg CPI = (2*0.35) + (2*0.4) + (4*0.25) = 2.5
   I1 Speed = $\frac{4*10^9 cycles}{1\ second} * \frac{1\ instruction}{2.9\ cycles} = 1.38 * 10^9 instructions/second$
   I2 Speed = $\frac{5*10^9 cycles}{1\ second} * \frac{1\ instruction}{2.5\ cycles} = 2 * 10^9 instructions/second$
   $\frac{2*10^9}{1.38*10^9} = 1.45\ or\ \frac{100}{69}$ I2 is 1.45 or 100/69 times faster than I1.

   c. I1 Avg CPI = (3*0.45) + (4*0.2) + (1*0.35) = 2.5
   I2 Avg CPI = (2*0.45) + (2*0.2) + (4*0.35) = 2.7
   I1 Speed = $\frac{4*10^9 cycles}{1\ second} * \frac{1\ instruction}{2.5\ cycles} = 1.6 * 10^9 instructions/second$
   I2 Speed = $\frac{5*10^9 cycles}{1\ second} * \frac{1\ instruction}{2.7\ cycles} = 1.85 * 10^9 instructions/second$
   $\frac{1.85*10^9}{1.6*10^9} = 1.16\ or\ \frac{37}{32}$ I2 is 1.16 or 37/32 times faster than I1.

   d. I1 offers the highest performance on C1.

   e. I2 offers the highest performance on C2.

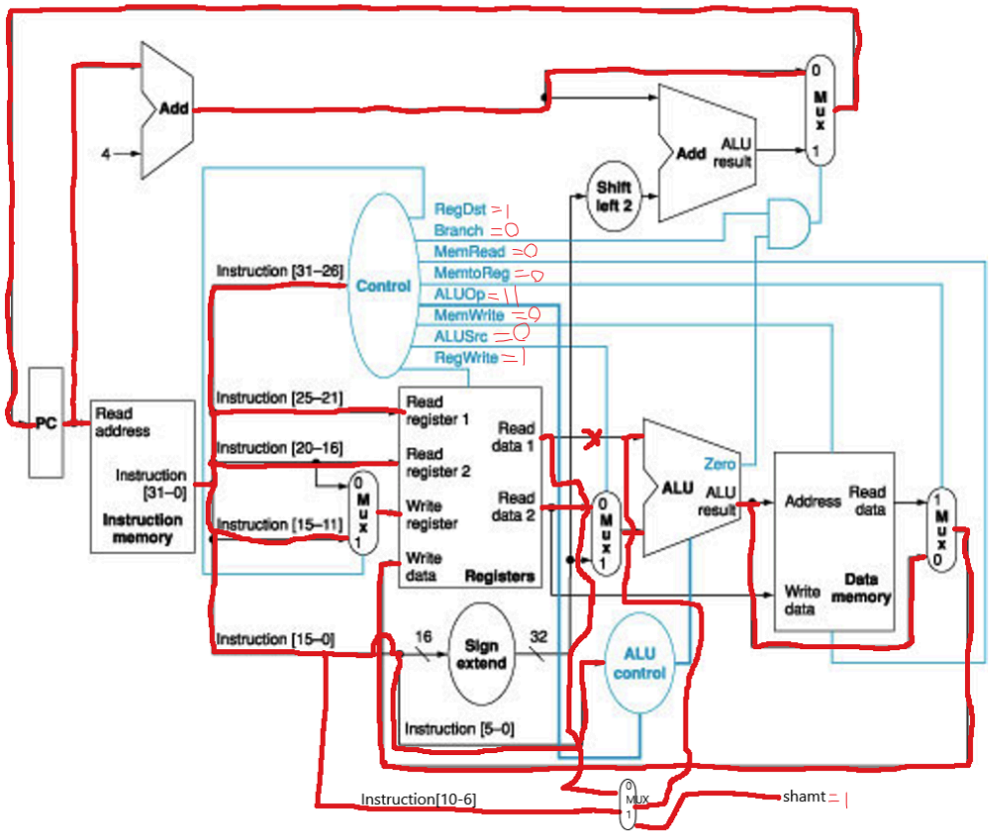
   f. I2 on C2 provides the highest overall performance among all other implementations and compilers.

3. a. lw, sw, and all R-type instructions, except for sub and slt, would cease to work normally. Only subtraction would work for evaluation of sub, beq, and slt instructions. lw, sw, and all other R-type instructions would be unable to perform addition.

b. Only R-type instructions would be affected. This will not permit the output of ALU operations to be written to registers within the register file. This would permit only values read from the main memory to be written to registers for R-type instructions.

c. The sw instruction would not work because both the read and write controls would be enabled at the same time. All other instructions would be unaffected because the control allows the main memory to be read and does not affect whether registers are written. This means that lw and all R-type instructions will still work.

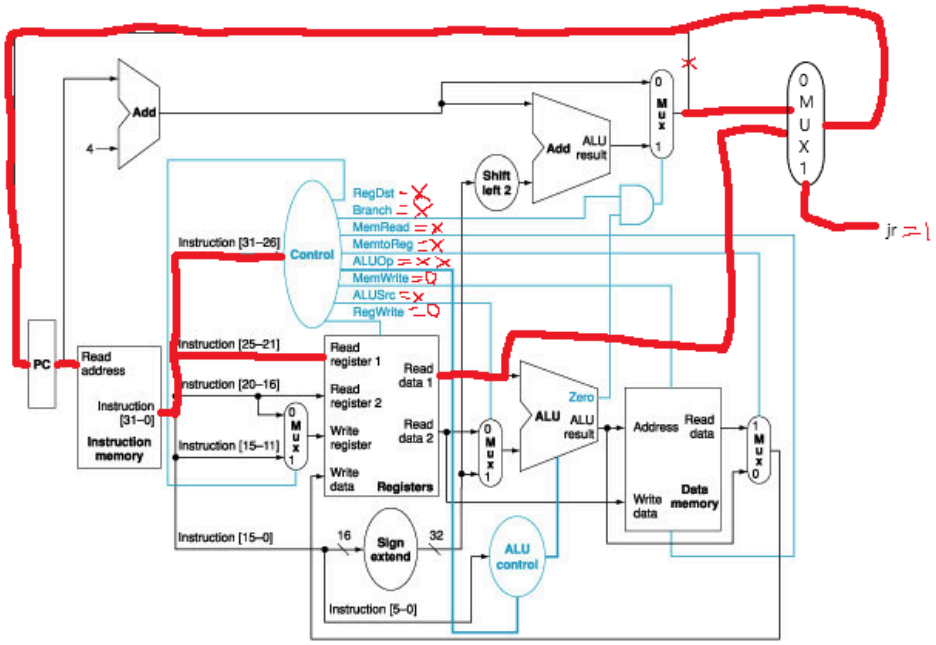
4.



The shamt control is used only for srl and sll instructions because the source register remains unused. The control is 1 for srl and sll instruction and 0 otherwise.

RegDst	1
ALUSrc	0
MemtoReg	0

RegWrite	1
MemRead	0
MemWrite	0
Branch	0
ALUOp1	1
ALUOp0	1
shamt	1



5.

The jr control signal is only used for jr instructions and is 1 only for jr instructions and 0 otherwise.

RegDst	X
ALUSrc	X
MemtoReg	X
RegWrite	0
MemRead	X
MemWrite	0
Branch	0
ALUOp1	X
ALUOp0	X
jr	1