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Assignment 10

1. a. 1 - Instruction 4 requires the value stored in $t7 that is written by Instruction 1.
   2 - Instruction 3 requires the value stored in $t8 that is written by Instruction 2.
   3 - Instruction 4 requires the value stored in $t6 that is written by Instruction 3.
   4 - Instruction 5 requires the value stored in $t6 that is written by Instruction 3.
   5 - Instruction 6 requires the value stored in $t5 that is written by Instruction 5.
   6 - Instruction 7 requires the value stored in $t2 that is written by Instruction 6.

   b. Dependencies 3, 4, and will be resolved by forwarding.

   c. Dependencies 2 and 6 will be resolved by stalls.

2. a. During the 5th cycle, $t3 is being written while $t2 and $t7 are being read.

   b. The forwarding unit checks the Rd values and the RegWrite control values for both EX/MEM and MEM/WB registers against the Rs and Rt values in the ID/EX register.

   ID/EX register contents: Rs = $t1, Rt = $t9 from “sub $t2, $t1, $t9”
   EX/MEM register contents: Rd = $t8, RegWrite = 1 from “add $t8, $t9, $t5”
   MEM/WB register contents: Rd = $t3, RegWrite = 1 from “sub $t3, $t5, $t4”

   $t1 and $t8 will be compared
   $t1 and $t3 will be compared
   $t9 and $t8 will be compared
   $t9 and $t3 will be compared
   $t8 and $t3 will also be checked for whether they will be written

   There is no match, so there will be no forward.

c. The hazard detection unit checks the Rt value and the MemRead control value of the ID/EX register against the Rs and Rt values of the IF/ID register.

IF/ID register contents: Rs = $t7, Rt = $t2 from “sub $t1, $t7, $t2”
ID/EX register contents: Rt = $t9, MemRead = 0 from “sub $t2, $t1, $t9”

$t9 and $t2 will be compared
$t9 and $t7 will be compared
The MemRead control will be checked

There is no match, so there will be no stall.

3. a. Miss

Block	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Addr							38									

b. Miss

Block	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Addr							38		8							

c. Miss

Block	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Addr				19			38		8							

d. Hit

Block	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Addr				19			38		8							

e. Hit

Block	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Addr				19			38		8							

f. Miss

Block	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Addr				19			38		56							

g. Hit

Block	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Addr				19			38		56							

h. Miss

Block	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Addr				19			38		8							

4. a. Miss

Block	0 (00)	1 (01)	2 (10)	3 (11)
Addr			40, 41, 42, 43	

b. Miss

Block	0 (00)	1 (01)	2 (10)	3 (11)
Addr			8, 9, 10, 11	

c. Miss

Block	0 (00)	1 (01)	2 (10)	3 (11)
Addr			40, 41, 42, 43	

d. Miss

Block	0 (00)	1 (01)	2 (10)	3 (11)
Addr		20, 21, 22, 23	40, 41, 42, 43	

e. Miss

Block	0 (00)	1 (01)	2 (10)	3 (11)
Addr		20, 21, 22, 23	8, 9, 10, 11	

f. Hit

Block	0 (00)	1 (01)	2 (10)	3 (11)
Addr		20, 21, 22, 23	8, 9, 10, 11	

g. Hit

Block	0 (00)	1 (01)	2 (10)	3 (11)
Addr		20, 21, 22, 23	8, 9, 10, 11	

h. Miss

Block	0 (00)	1 (01)	2 (10)	3 (11)
Addr	16, 17, 18, 19	20, 21, 22, 23	8, 9, 10, 11	