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DESIGN AND IMPLEMENTATION OF RING OSCILLATOR USING GPDK 90nm

PROJECT REPORT

COURSE NAME: ANALOG ELECTRONICS

COURSE CODE: BEEE208L

Under the guidance of Prof.

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SLOT: A2 **CLASS: TT413**

Submitted by

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ABSTRACT

The project here describes design and implementation of a CMOS ring oscillator using GPDK 90nm technology. A ring oscillator, consisting of an odd number of inverters connected in a closed loop, is widely used in clock generation, frequency synthesis, and performance benchmarking in VLSI circuits. Here a three-stage ring oscillator is designed to produce sustained oscillations. The circuit is designed and simulated in Cadence Virtuoso, where parametric sweep is used to set the dimensions of the MOSFETs, and transient analysis is used to find the frequency of the oscillations. The post layout simulation yields an oscillation frequency of 13.22GHz.

INTRODUCTION

A ring oscillator is a type of oscillator circuit composed of an odd number of inverters connected in a closed loop, generating a continuous oscillating signal without requiring an external clock. The oscillation is sustained due to the inherent delay in each inverter stage, which determines the frequency of the output waveform.

Working Principle

When an initial transition occurs at the input of the first inverter, the signal propagates through the chain of inverters, experiencing a cumulative delay at each stage. Since the circuit consists of an odd number of inverters, the output transitions continuously between high and low states, forming a periodic oscillation. The oscillation frequency f is given by:

$$f = \frac{1}{2 \times n \times T_d}$$

Where T can be written as

$$T_d = \frac{(Tplh + Tphl)}{2}$$

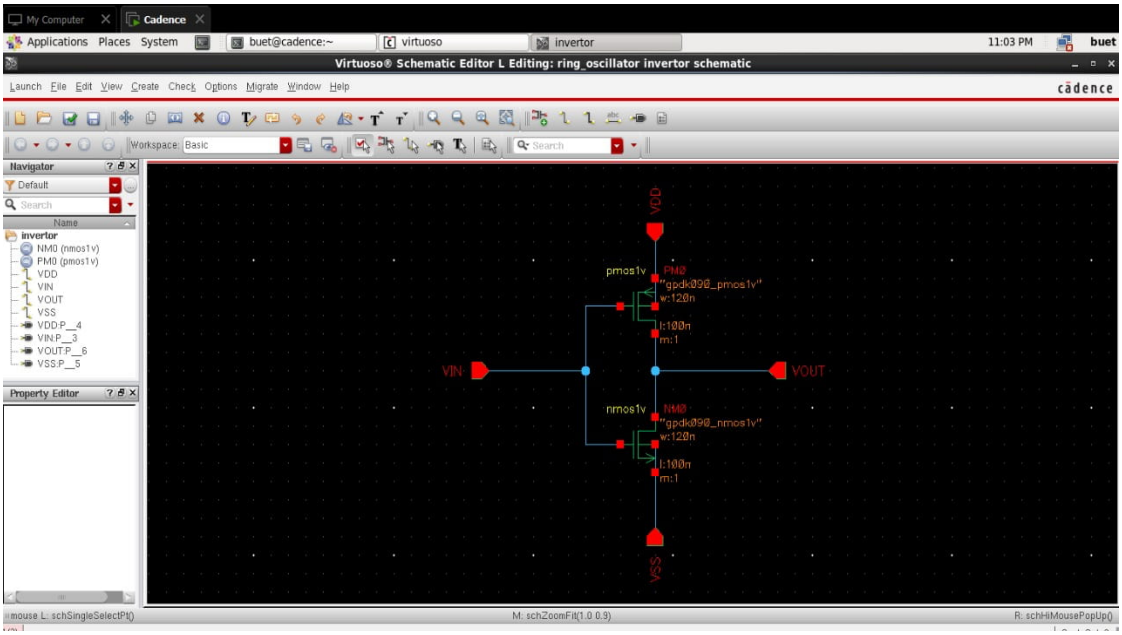
Therefore

$$f = \frac{1}{n \times (Tplh + Tphl)}$$

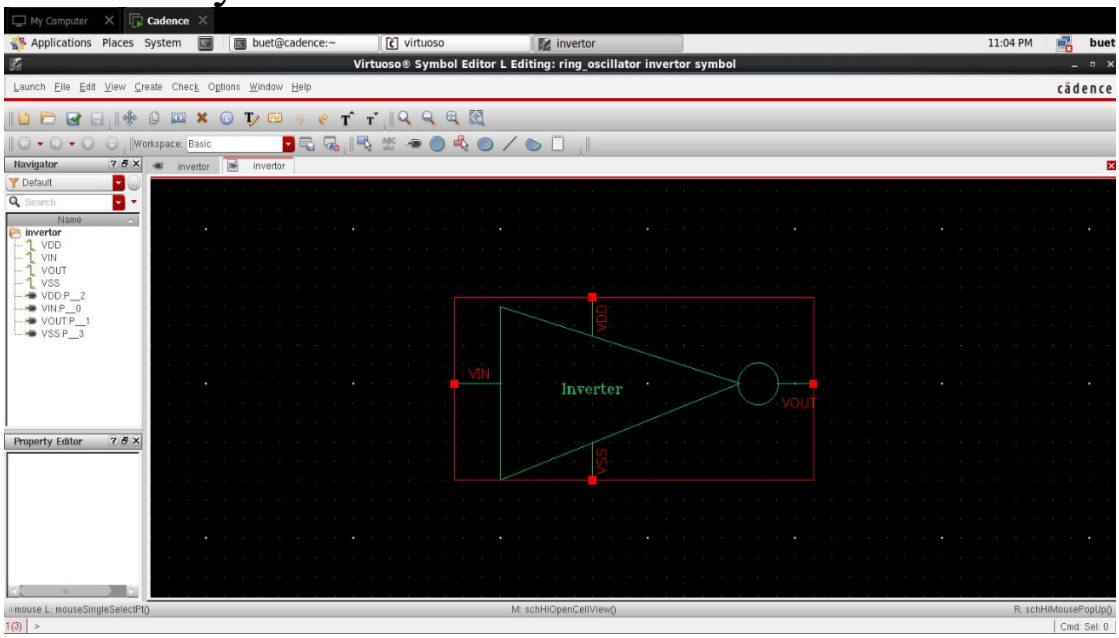
f = frequency of oscillation
n = No. of stages
T_d = Propagation delay of the inverter
T_{plh} = Rise time delay
T_{phl} = Fall time delay

CIRCUIT DIAGRAM

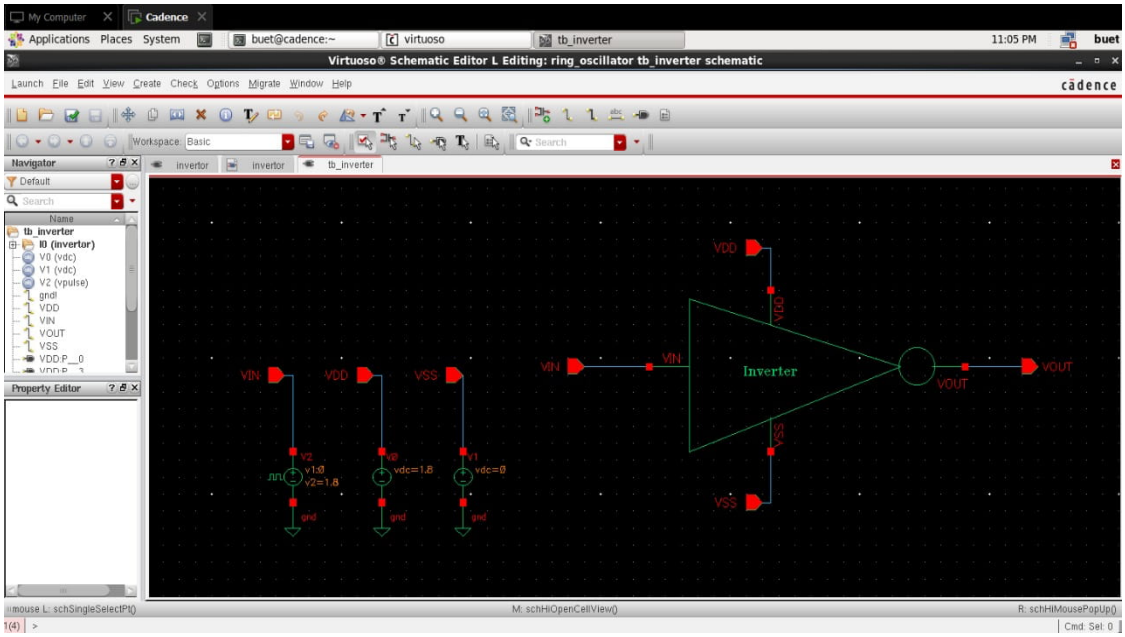
Inverter Schematic



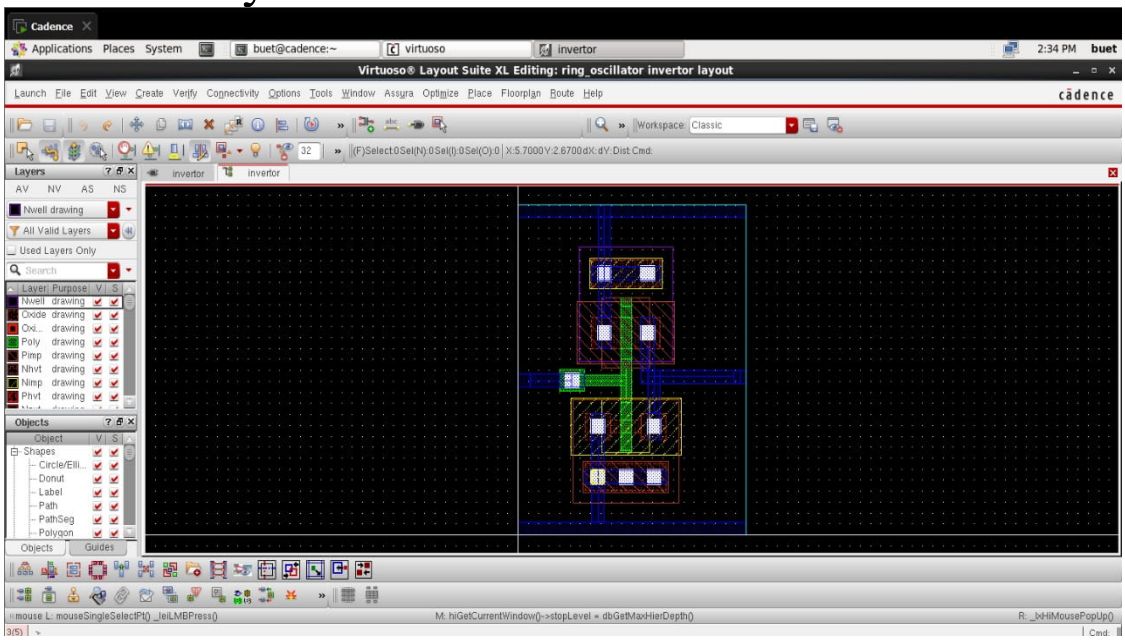
Inverter Symbol



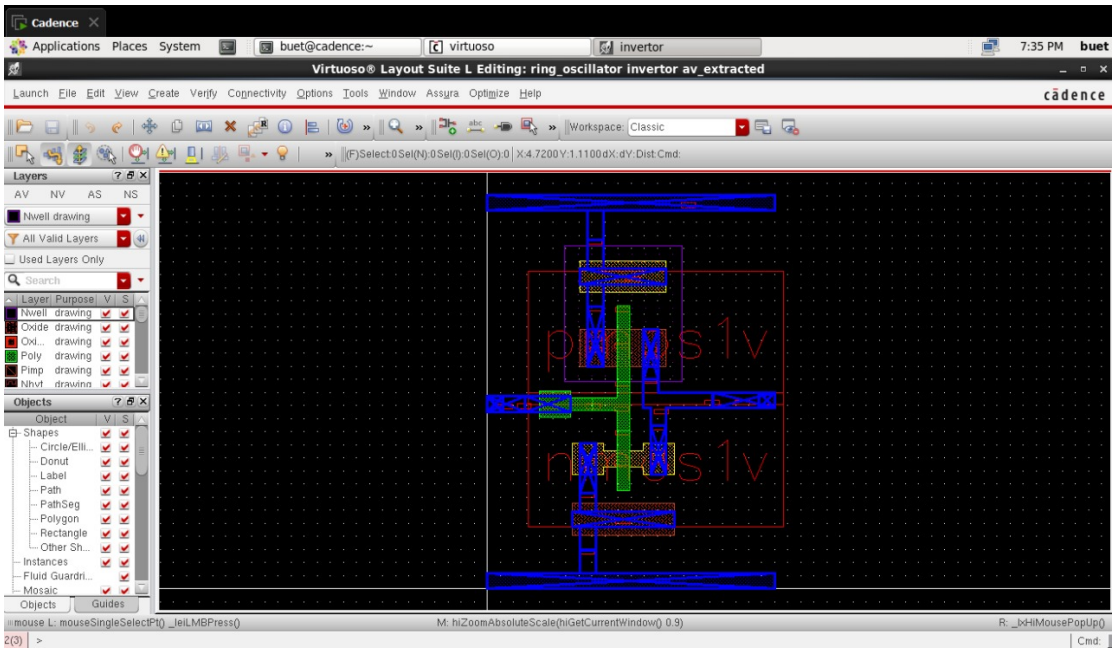
Inverter Testbench



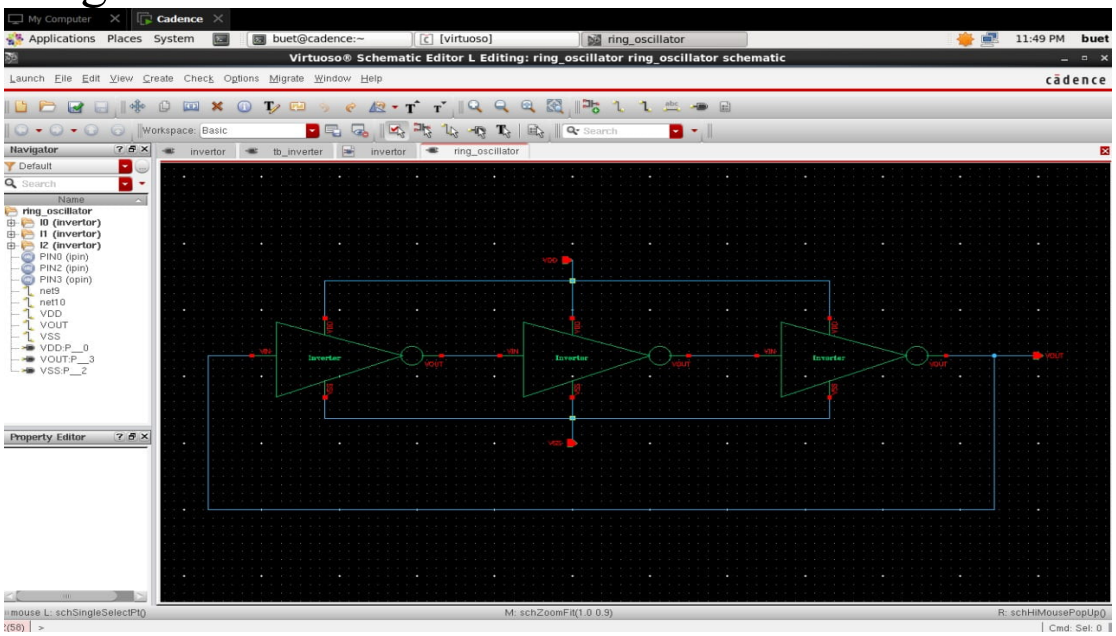
Inverter Layout



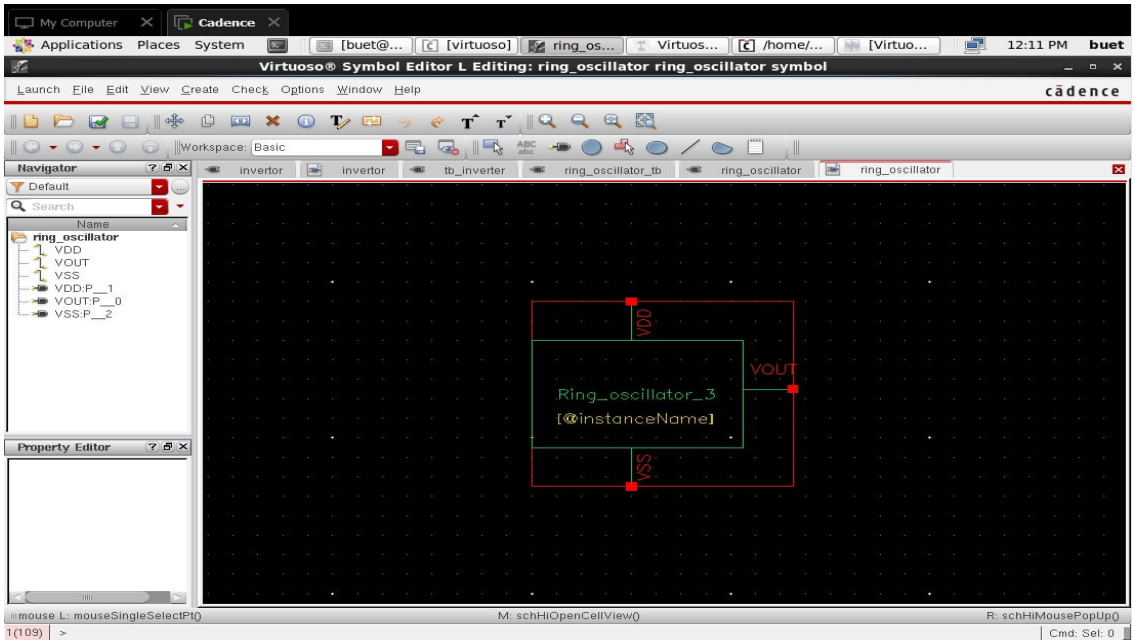
Inverter RC Extracted cell view



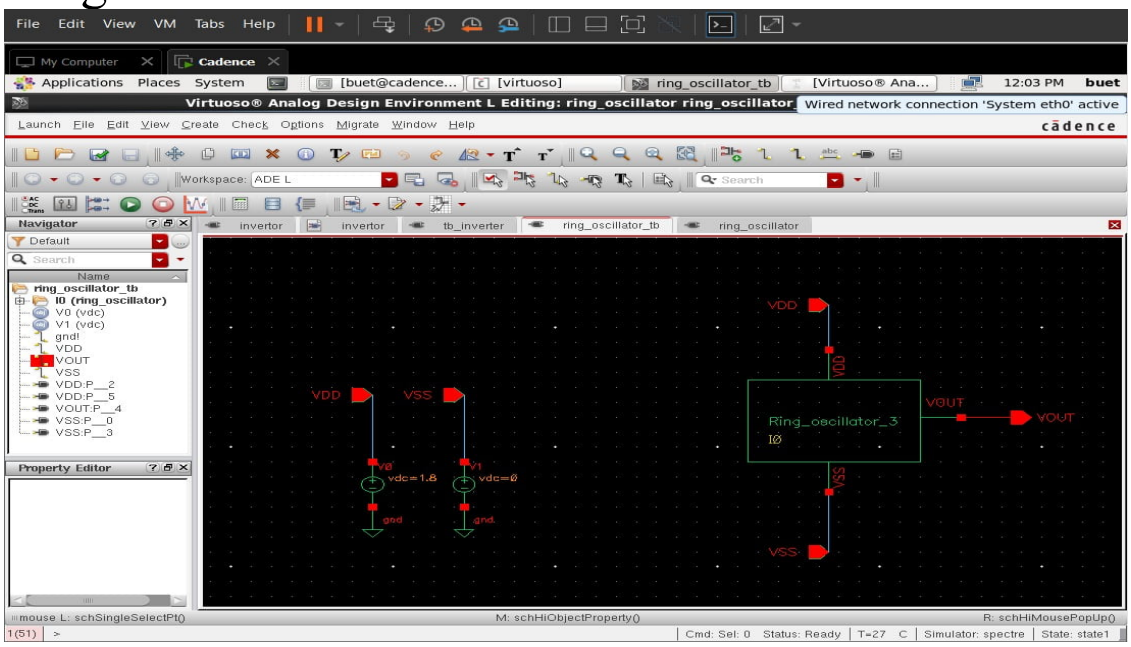
Ring Oscillator Schematic



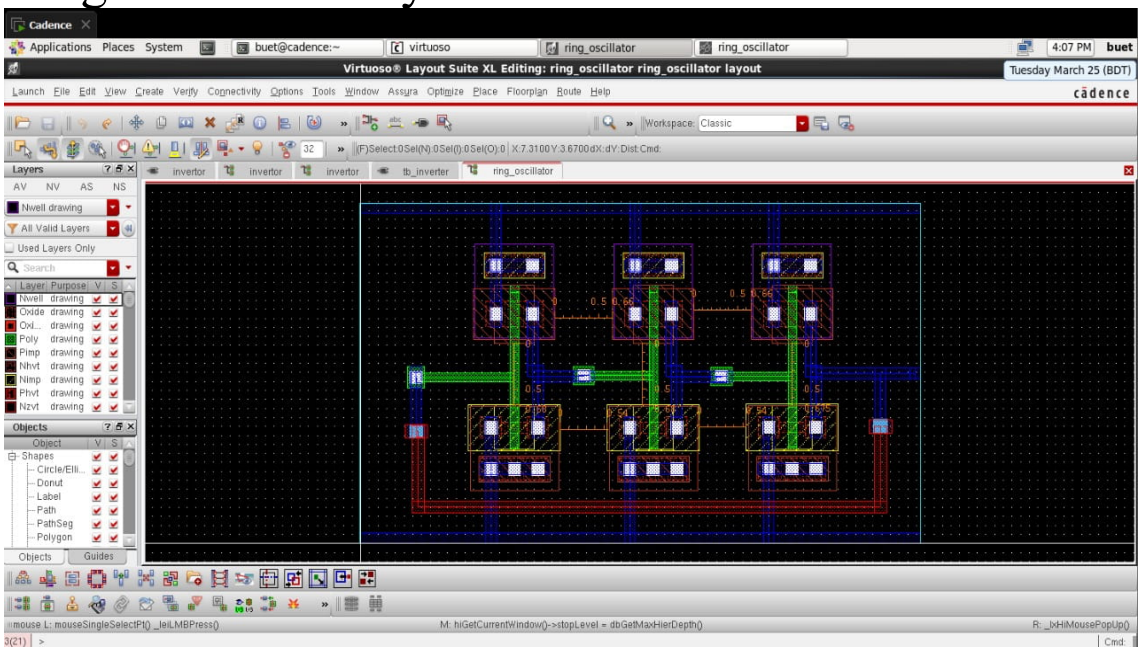
Ring Oscillator Symbol



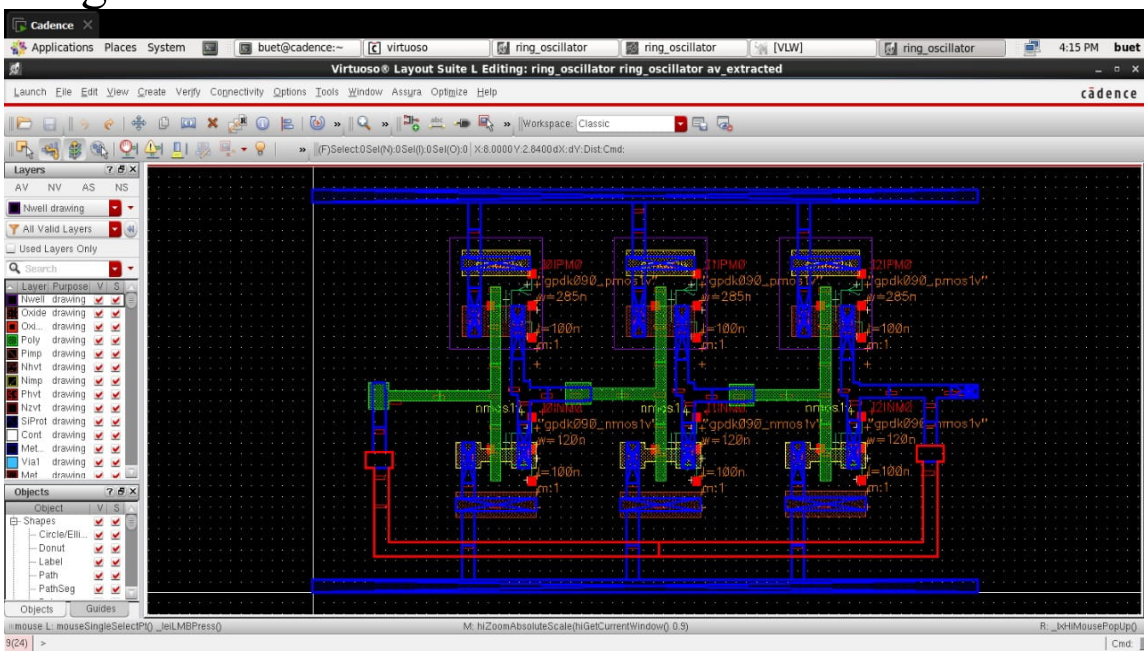
Ring Oscillator Testbench



Ring Oscillator Layout



Ring Oscillator RC Extracted cell view



IMPLEMENTATION

Circuit Overview

The design is implemented using GPDK 90nm technology in Cadence Virtuoso, where transistor dimensions are optimized using parametric sweeps, and transient analysis is performed to determine the oscillation frequency.

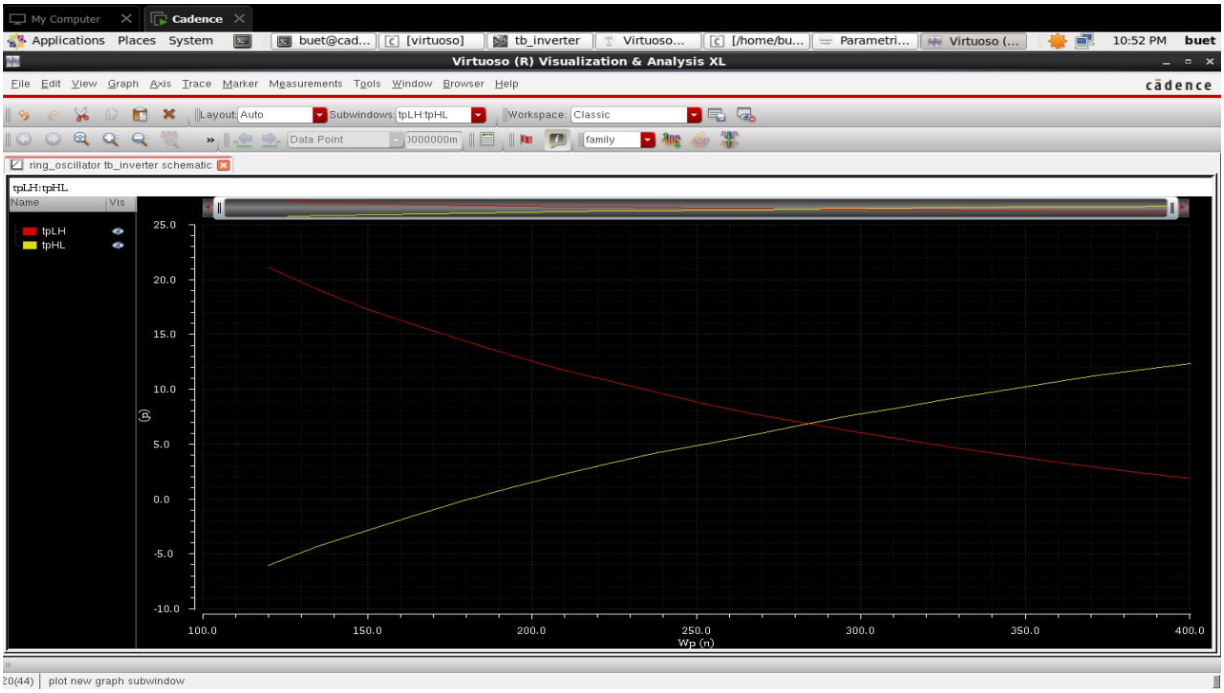
1. **Inverter Schematic connections:**
   The following connections are done to form a CMOS inverter:

- Gate Connection: The gate terminals of PMOS and NMOS are connected together to form the inverter input.
- Drain Connection: The drain terminals of PMOS and NMOS are connected together to form the inverter output.
- Source & Bulk Connections: The PMOS source and bulk are connected to VDD, while the NMOS source and bulk are connected to VSS.

2. **Inverter Optimization:**

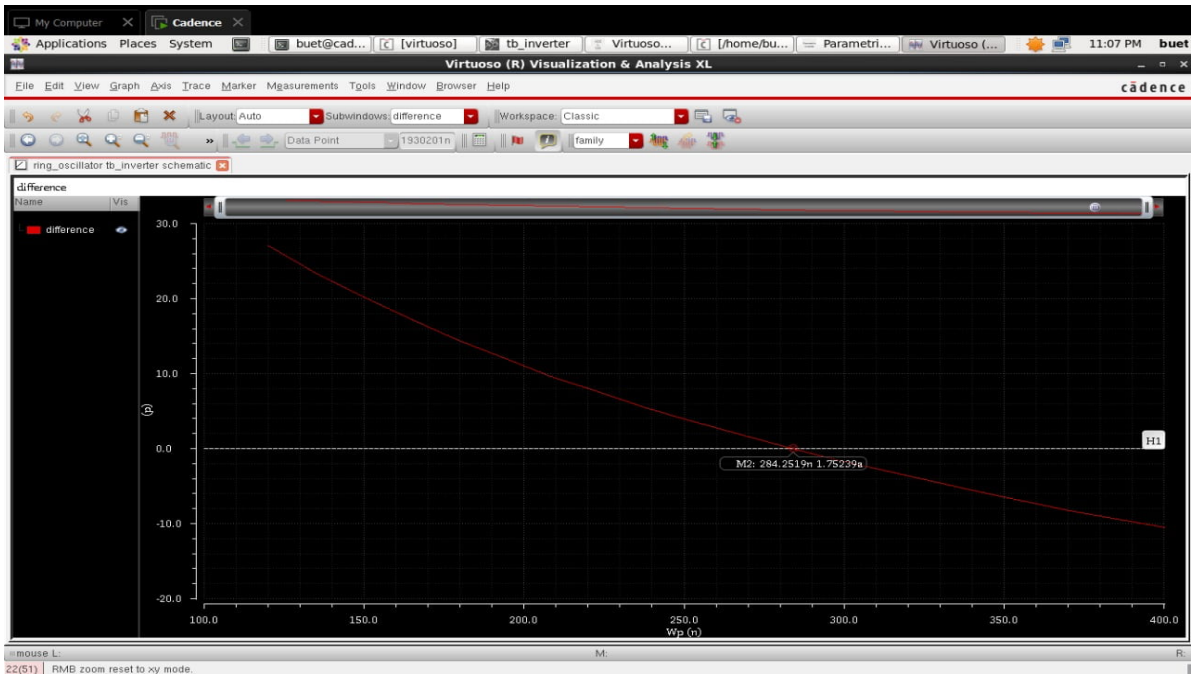
Optimizing the CMOS inverter ie. transistor sizing is crucial for improving the performance of the ring oscillator**,** as the propagation delay per inverter directly affects the oscillation frequency**.**

- The widths of PMOS (Wp) and NMOS (Wn) transistors are adjusted to balance rise and fall times, ensuring symmetric switching**.**
- PMOS transistors generally have lower mobility than NMOS transistors, so the width ratio is increased to compensate.
- Hence, parametric sweep is used, keeping the width of the PMOS as the parameter that is varied. The graph is plotted between the rise time (T_{plh}) and fall time (T_{phl}) delay vs width of PMOS(Wp).



Propagation delay vs PMOS width graph

- Another Parametric sweep is done between the difference (T_{plh} - T_{phl}) vs the width of the PMOS. So that the PMOS width at which the difference between the rise and fall time is 0 ie. rise time and fall time is equal ($T_{plh} = T_{phl}$) .



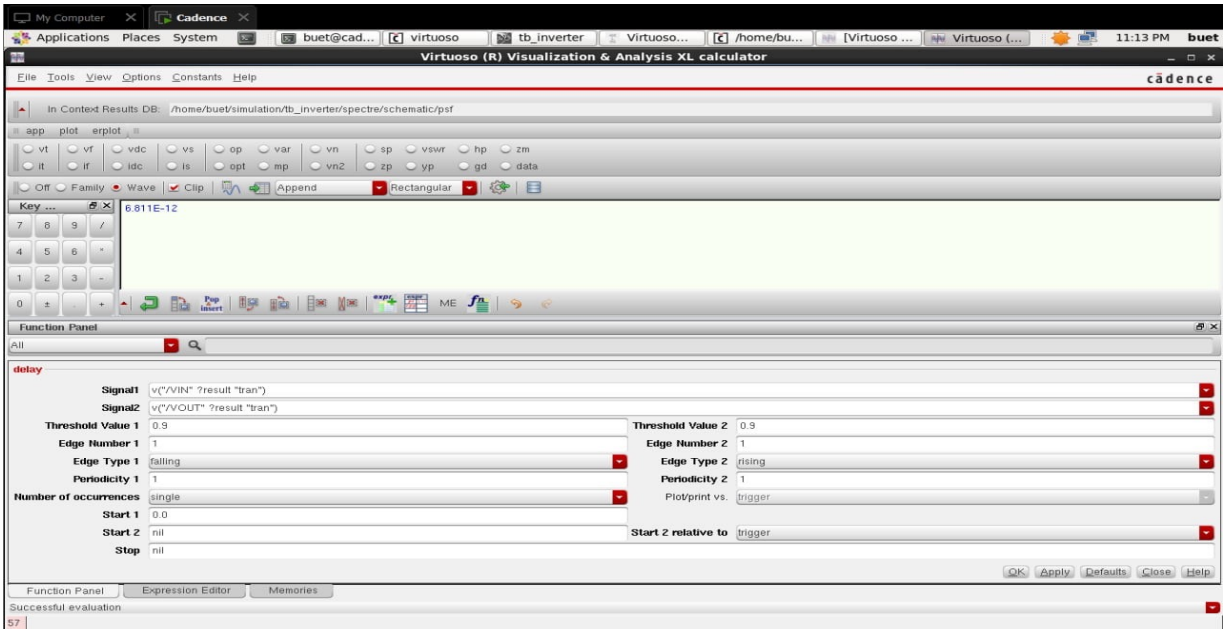
Propagation delay difference vs PMOS width graph

- The width of the PMOS (Wp) at which the the rise and fall time delay are equal is 285nm

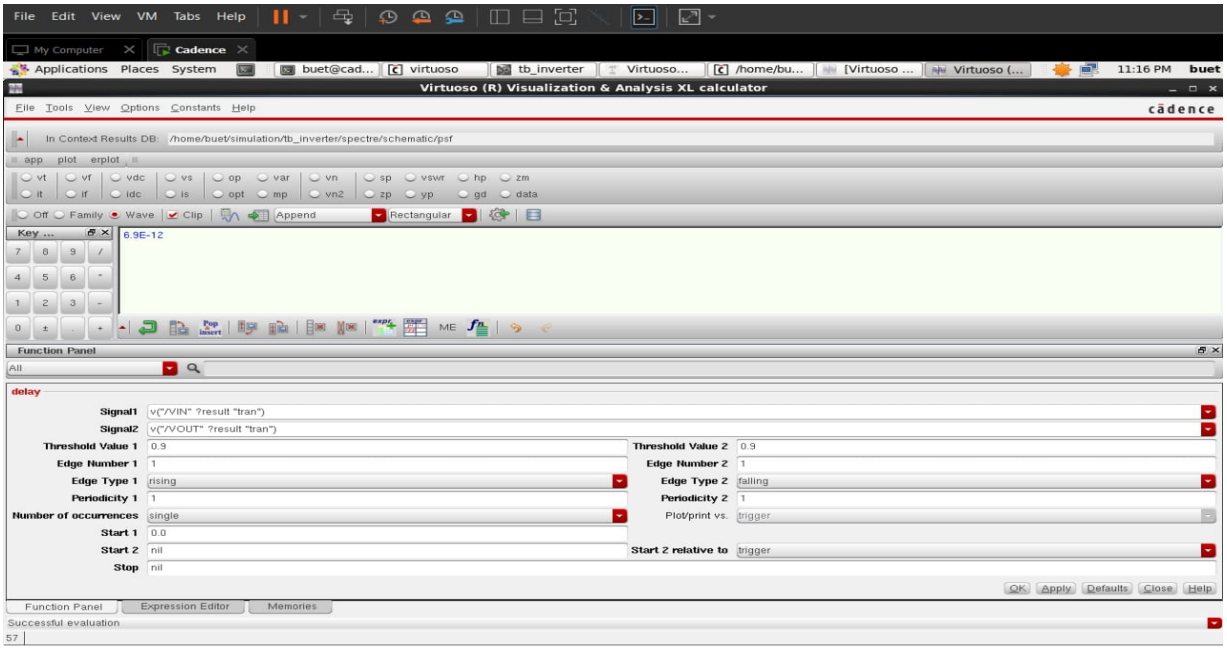
- To verify if the rise (T_{plh}) and fall time (T_{phl}) are equal and also to find the simulated rise and fall time delay transient analysis is done.

Simulation of Inverter Schematic after setting Wp = 285nm

- Rise time (T_{plh}) and fall time (T_{phl}) delay is calculated using the calculator.



Rise time (T_{plh})



Fall time (T_{phl})

- The rise time (T_{plh}) and the fall time (T_{phl}) appear to be almost equal ie 6.811ps ~ 6.9ps.

3. Inverter Layout:

- **Gate Connection --** The gate connection is established by the polysilicon layer, which forms the gate of both PMOS and NMOS transistors. The polysilicon is linked to the input terminal of the inverter through a combination of metal-1 and poly via.
- **Drain Connection --** The drain connection is made by joining the drain diffusion of both the PMOS and NMOS transistors using metal-1, thereby forming the output node.
- **Source & Bulk Connections --** Regarding the source and bulk **connections**, the PMOS source and bulk are connected to VDD using metal-1, while the NMOS source and bulk are connected to VSS using metal-1.

4. Ring Oscillator Schematic Connections:

- **Inverter Chain Formation --** three CMOS inverters are connected in series. The output of each inverter serves as the input for the next inverter in the sequence.
- **Feedback Loop --** A feedback loop is established by connecting the output of the last inverter back to the input of the first inverter. This configuration ensures continuous oscillation due to the inherent delay introduced by each inverter stage.

- **Power and Ground Connections --** For **power and ground connections**, all VDD terminals of the inverters are connected to a 1.8V DC supply, while all VSS terminals are connected to a 0V DC supply.

5. Ring Oscillator Layout Connections:

- **VDD Rail --** The VDD rail is positioned at the top of the layout and is implemented using Metal 1 in blue. This rail supplies the operating voltage to all inverters, ensuring a stable power source for the circuit.

- **PMOS Source Connections** -- The PMOS source connections are directly linked to the VDD rail, guaranteeing that the PMOS transistors receive the necessary supply voltage for proper operation.

- **VSS Rail --** The VSS rail is located at the bottom of the layout and is also implemented using Metal 1 in blue. This rail provides the ground (GND) connection for the circuit, establishing a reference voltage for all components.

- **NMOS Source Connections --** The NMOS source connections are made to the VSS rail using the Metal 1 layer. This configuration ensures that all NMOS transistors have a stable ground reference, allowing them to function correctly.

- **Gate Connections --** The gate connections of each PMOS and NMOS pair are connected together using the poly layer. This forms the input node of each inverter stage, enabling proper signal propagation throughout the circuit.

- **Drain Connections --** The drain connections of each PMOS and NMOS pair are joined together using the Metal 1 layer, forming the output node of each inverter stage. This connection ensures that the voltage transitions are properly transmitted between inverters.

- **Drain to Gate Connections --** For drain-to-gate connections, the drain of each PMOS-NMOS pair is connected to the gate terminal of the next inverter. This is achieved using Metal 1 for the drain connection, followed by a Metal 1 to Poly via to transition to the gate terminal, since the gate is implemented using Poly. This setup forms the cascading link between successive inverters, allowing the oscillation to propagate.

- **Feedback Connection –** The feedback connection, linking the last inverter to the first inverter, is implemented using Metal 1 for the initial drain connection. A Metal 1 to Metal 2 via is used to transition to Metal

2, followed by a Metal 2 to Metal 1 via to transition back to Metal 1. Finally, a Metal 1 to Poly via ensures proper connection to the gate of the first inverter. Metal 2 is used in this process to prevent shorting between the NMOS source-VSS connection and the feedback path, while also reducing resistance and minimizing delay, thereby improving the oscillation speed.

- **Output Connection --** The output connection is established by connecting the drain of the last PMOS-NMOS pair to the output pin. This provides the oscillating signal as the final output of the ring oscillator, which can be utilized in clock generation and other applications.

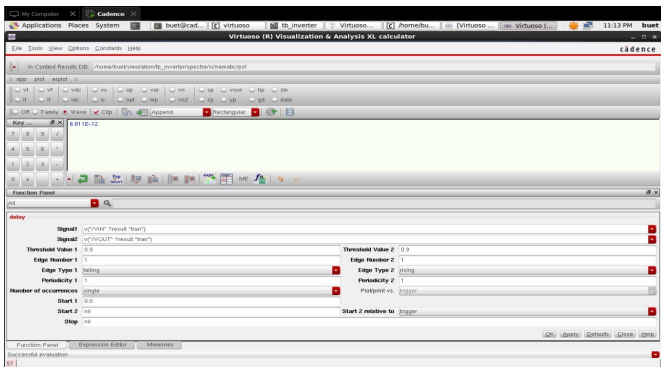
Frequency Calculation:

1. From Inverter Schematic:

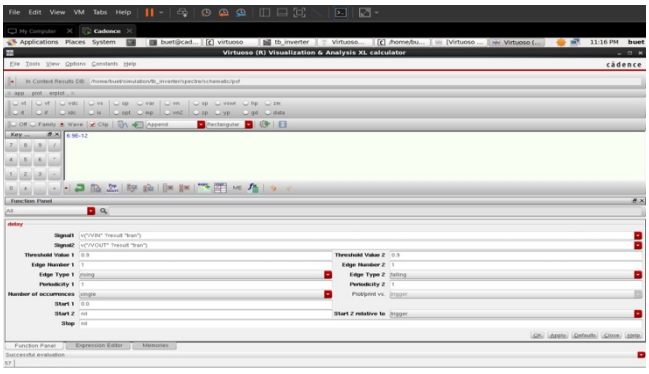
- The frequency of the oscillations produced by ring oscillator using this inverter can be calculated using the rise and fall time delay.

$$T_d = \frac{(Tplh + Tphl)}{2} = \frac{6.811ps + 6.9ps}{2} = 6.855ps$$

$$f = \frac{1}{2 \times n \times T_d} = \frac{1}{2 \times 3 \times 6.855ps} = 24.3GHz$$



Rise time (T_{plh})

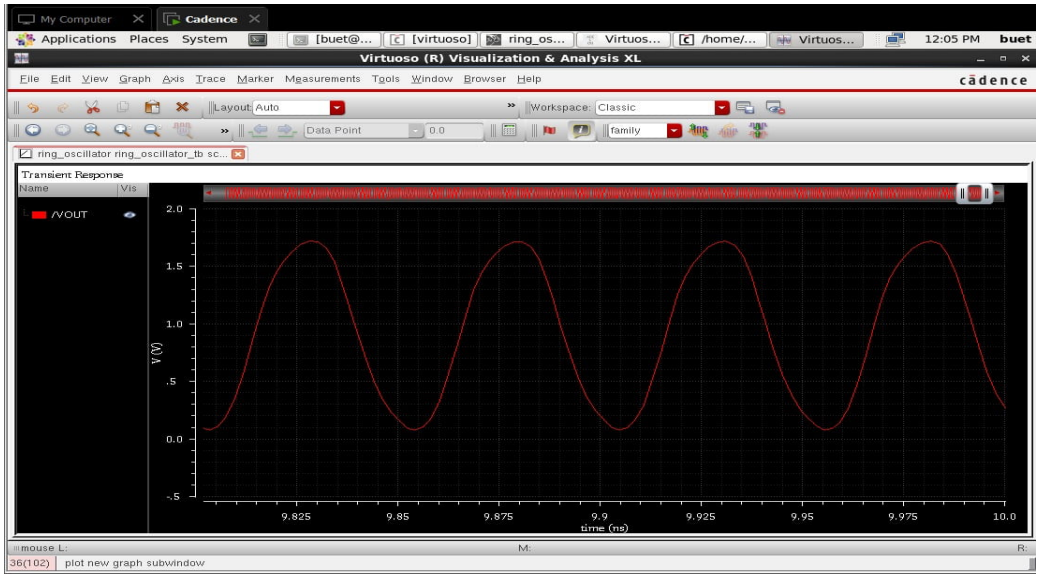


Fall time (T_{phl})

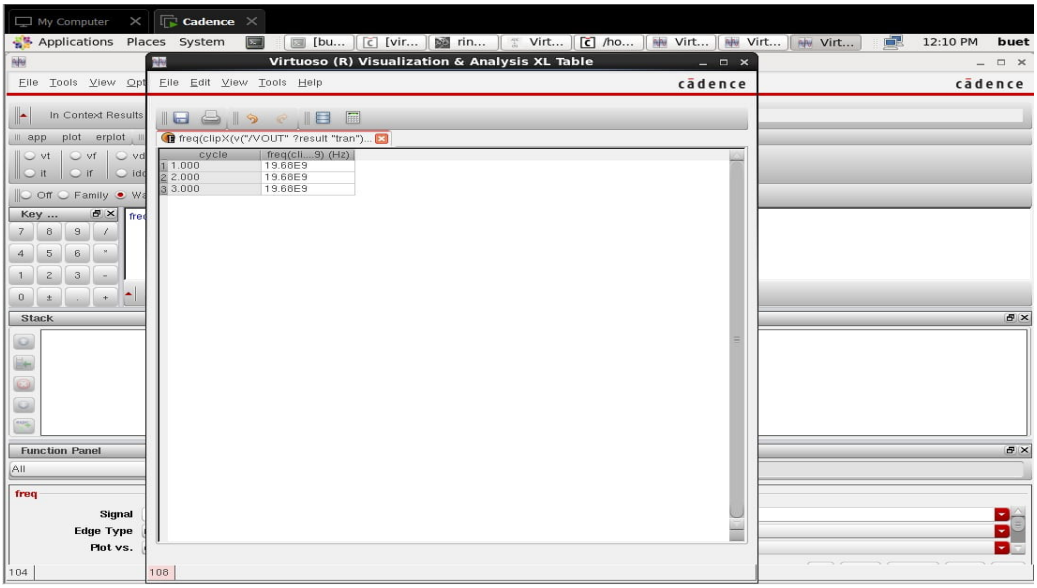
2. From Ring Oscillator Schematic:

- The frequency of the simulated oscillations produced by ring oscillator using the inverters can be found using the calculator available in the simulation window.

$$f = 19.68GHz$$



Simulated Oscillation



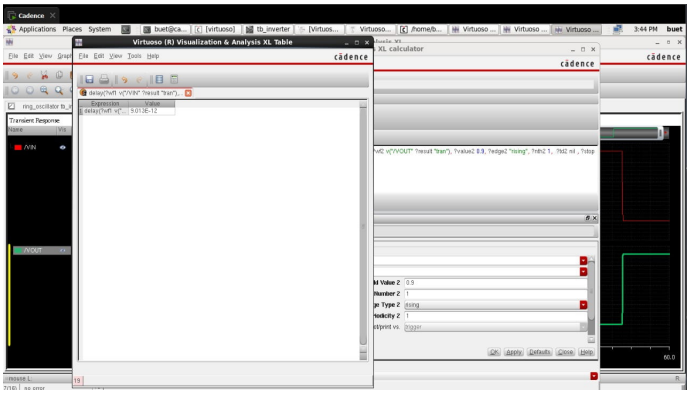
Simulated frequency

3. From Inverter Layout:

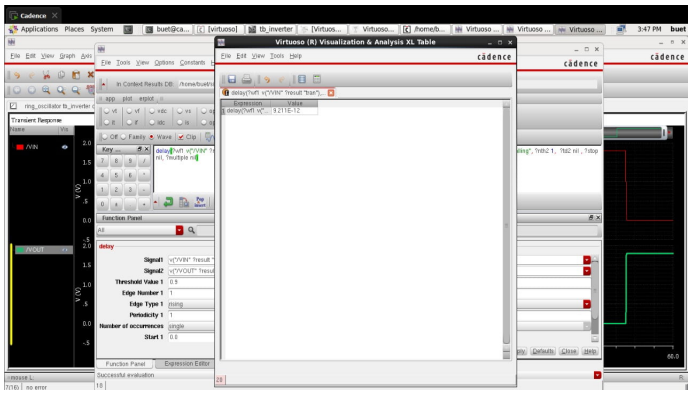
- The frequency of the oscillations produced by ring oscillator using this inverter can be calculated using the rise and fall time delay.

$$T_d = \frac{(Tplh + Tphl)}{2} = \frac{9.013ps + 9.211ps}{2} = 9.112ps$$

$$f = \frac{1}{2 \times n \times T_d} = \frac{1}{2 \times 3 \times 9.112ps} = 18.29GHz$$



Rise time (T_{plh})

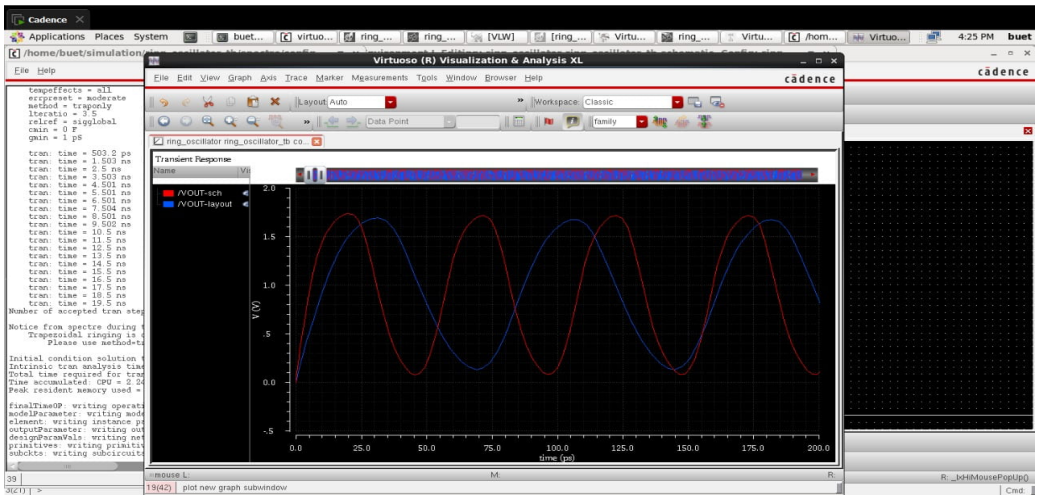


Fall time (T_{phl})

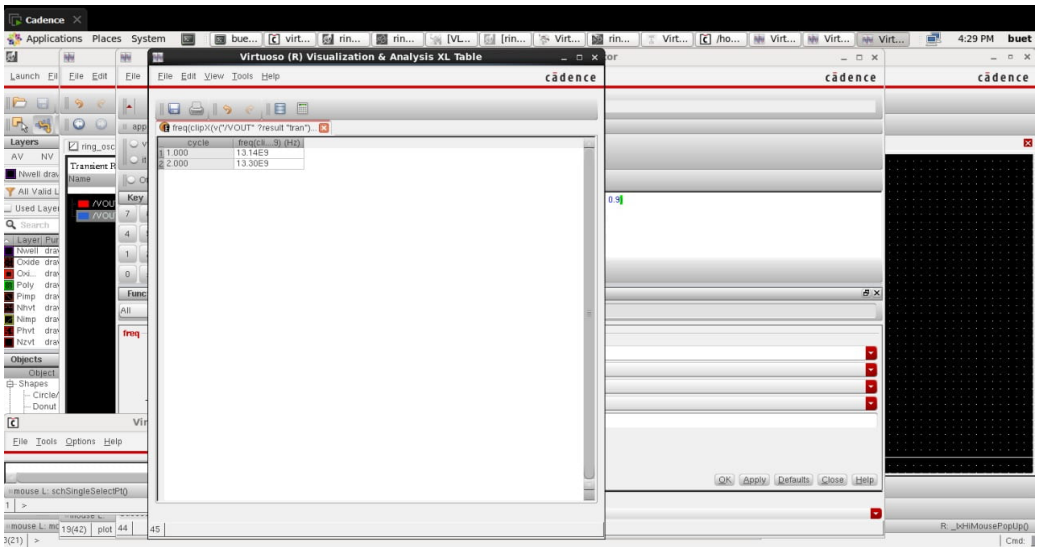
4. From Ring Oscillator Layout:

- The frequency of the simulated oscillations produced by ring oscillator using the inverters can be found using the calculator available in the simulation window.

$$f = 19.68GHz$$



Simulated Oscillation



Simulated Frequency

TABULATION:

INVERTER				RING OSCILLATOR			
SCHEMATIC		LAYOUT		SCHEMATIC		LAYOUT	
W_p	285nm	W_p	285nm	W_p	285nm	W_p	285nm
W_n	120nm	W_n	120nm	W_n	120nm	W_n	120nm
L_p	100nm	L_p	100nm	L_p	100nm	L_p	100nm
L_n	100nm	L_n	100nm	L_n	100nm	L_n	100nm
T_{plh}	6.811ps	T_{plh}	9.013ps	calculated Frequency	24.3GHz	calculated Frequency	18.29GHz
T_{phl}	6.9ps	T_{phl}	9.211ps	Simulated Frequency	19.68GHz	Simulated Frequency	13.22GHz
T_{pd}	6.855ps	T_{pd}	9.112ps	%deviation	19.01	%deviation	27.72

CONCLUSION

The CMOS ring oscillator designed using GPDK 90nm technology provides a compact, efficient, and high-frequency solution for generating clock signals. The layout incorporates Metal 1 and Metal 2 layers strategically to prevent shorting and reduce resistance, improving performance. With a frequency of 13.22GHz achieved in post-layout simulations, the oscillator demonstrates reliable operation despite minor parasitic effects.

The use of Metal 2 in the feedback path reduces delay by lowering resistance compared to Metal 1, enhancing the overall speed of the circuit. The layout is

optimized with seamless connections using poly, Metal 1, and Metal 2 layers, ensuring stable and consistent oscillations.

Although the oscillator achieves high-frequency performance, minor discrepancies from the calculated frequency highlight the influence of parasitic. Despite this, the design offers an effective and scalable solution for use in high-speed digital circuits, clock generation, and signal processing applications.

For future improvements, reducing parasitic capacitance can help further enhance the oscillator's frequency. Exploring advanced interconnect strategies, such as using higher metal layers with lower resistance, can also contribute to reducing delays. Additionally, implementing different circuit topologies, such as current-starved inverters or tuning techniques, may improve frequency control. These enhancements can make the design even more suitable for high-speed digital applications, including clock generation and signal processing.

REFERENCES:

1. https://youtu.be/S0cvOUzhuzU?si=iq_vTaXR3bdtGGrA
2. https://youtu.be/tK9St35jATA?si=SPjjySiNm5wn2jlj
3. https://youtu.be/yjw56v3Oigo?si=6FbMkMkAtEUCXg-9
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5. https://youtu.be/ZOd8JkrM8sY?si=JNt9G6OHKOTsbrX5
6. https://youtu.be/PX4R9CA6fWg?si=FG0hRDH9coNtSbv3