Group 47
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G47_VGA: vga generator for display

Circuit name: g47_VGA
Input(s): clock (1 bit), reset (1 bit)
Output(s): BLANKING (1 bit), ROW (10 bit), COLUMN (10 bit), HSYNC (1 bit), VSYNC (1 bit)
Component(s): 2 instances of the lpm_counter from the lpm library

Description:

The circuit takes 2 1-bit signals, clock and reset, as input. The outputs ROW and COLUMN signals gives the coordinates of the currently active pixel. There are two lpm_counters in the circuit, HCounter and VCounter, use to count the horizontal position, in pixels, relative to start of the line and the vertical position relative to the frame respectively.

The outputs of the two counters are represented by the signals hcount (11 bit) and vcount (10 bit), when hcount reaches 1039 (end of line) it clears the HCounter, when vcount reaches 665 (end of frame) it clears both counters. The ROW output is equal to (vcount - 43) to give ROW=0 at the top edge of the visible area. ROW value is 599 for all vcount < 43 and vcount > 642. Similarly, the COLUMN output is set to (hcount - 176), to get COLUMN=0 at the left edge of the visible area. COLUMN value is 799 when hcount < 176 or hcount > 975.

The Vsync is 0 when 0 <= vcount < 6, else it is 1. Likewise Hsync is 0 when 0 <= vcount < 120, else it is 1. BLANKING is 0 when vcount < 43 or vcount > 642 or when hcount <176 or hcount > 975. Otherwise, BLANKING is set to 1.

Symbol Diagram:

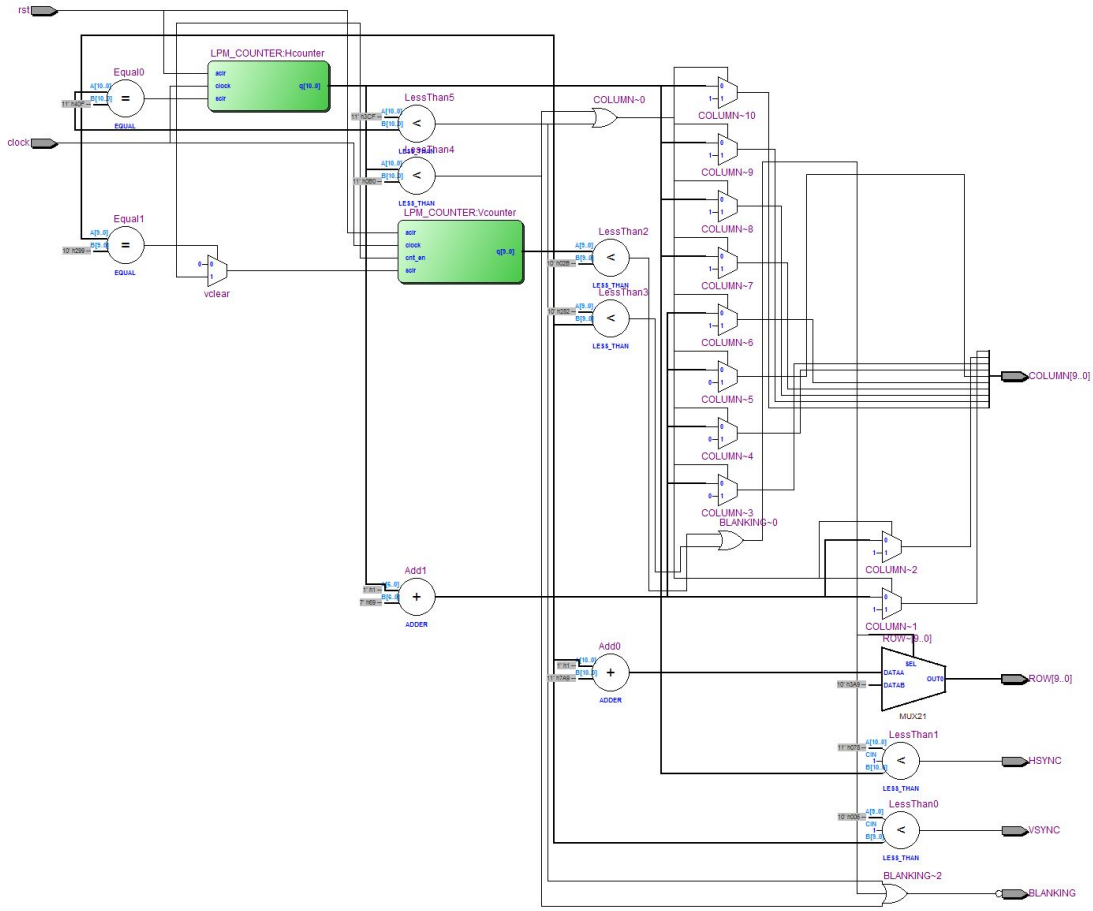


Fig 1. Symbol Diagram

Testing & Representative Simulation

We are using Modelsim to test the circuit. We used ModelSim to see if the the circuit behaves as defined in the description. This results are provided in the screenshots below.

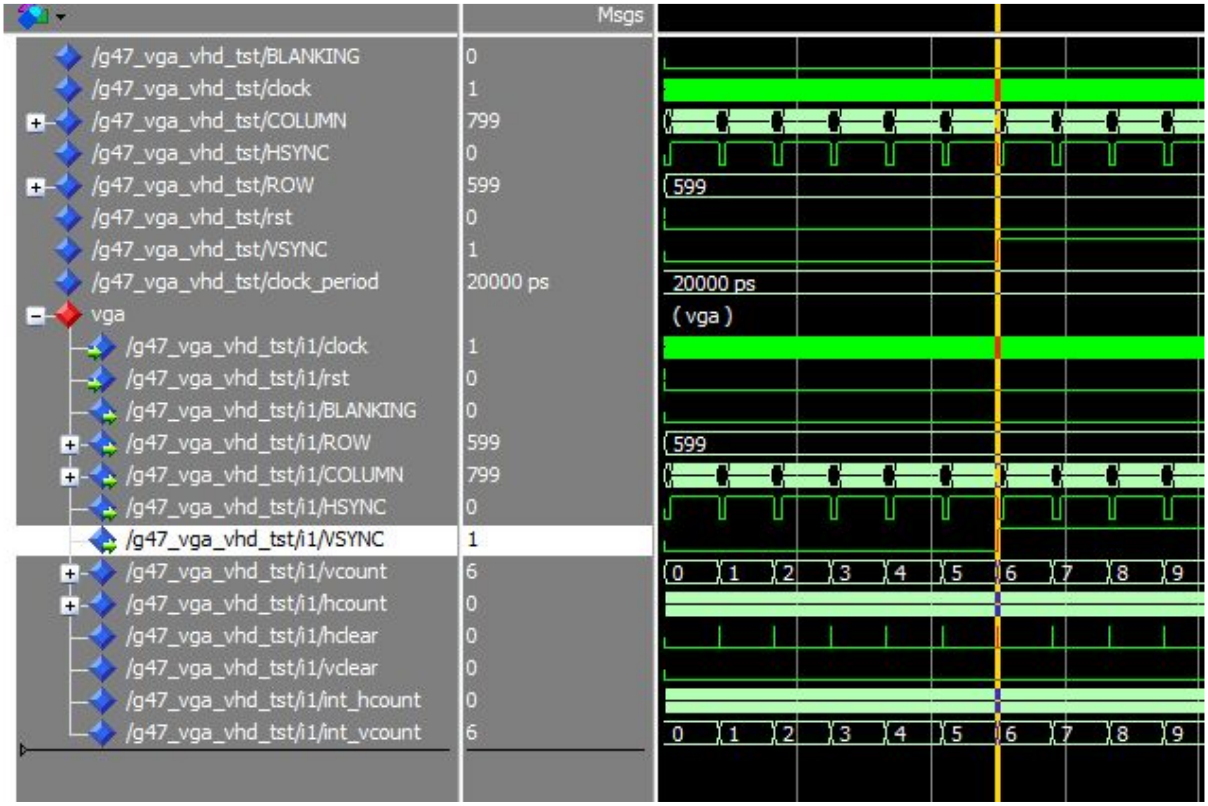


Fig 2. VSYNC value is 1 when vcount reaches 6, 0 before

From figure 2 we can see that the VSYNC value is 0 for vcount value 0-6 and it goes up to 1 when the vcount value reaches which is what we expect. On Fig 3 (see below), it can be seen that VSYNC remains high until vcount value is 665, once it reaches 666 the count is cleared and has value 0 and VSYNC goes back to being to being low. Also both ROW and COLUMN have the proper range (0 to 799 for COLUMN and 0 to 599 for the ROW).

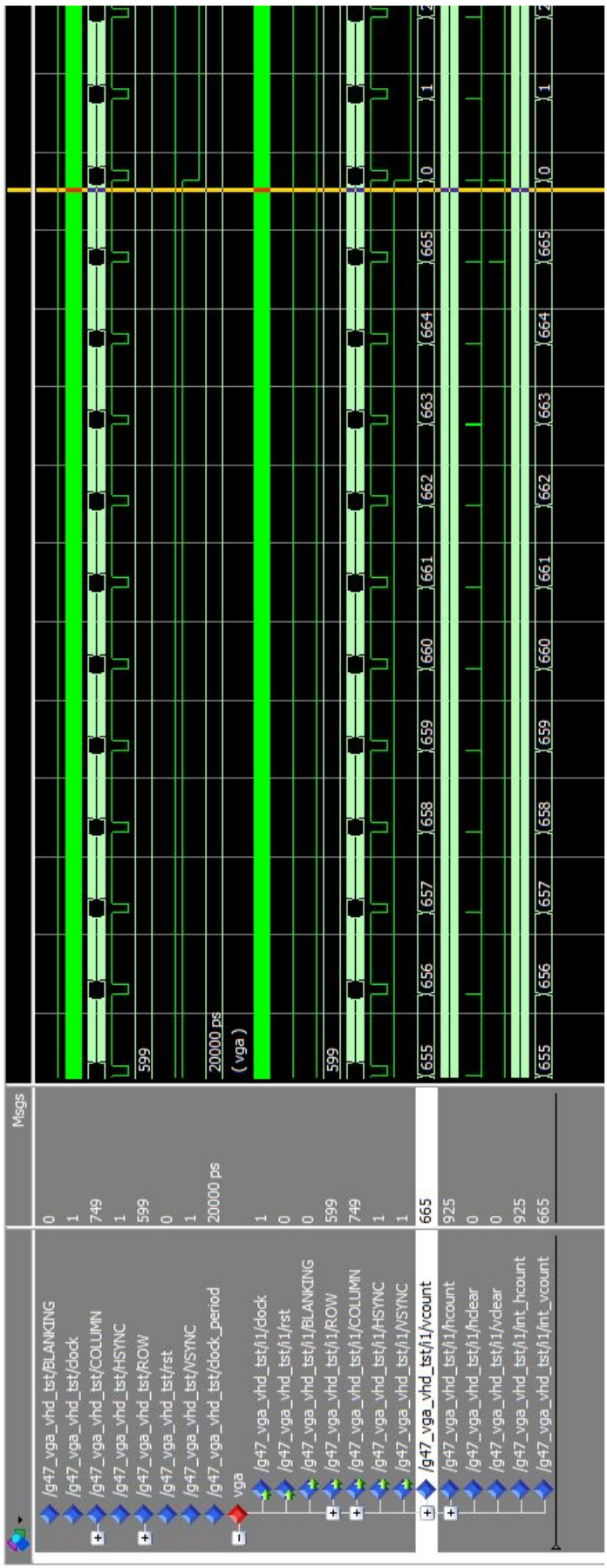


Fig 3. VSYNC remains high before 666

Similarly, Fig 4 and 5 shows the shows the behaviour of the HSYNC with respect to the Hcount values. we can see that HSYNC is for hcount value 0 and until it reaches 120. When HCount reaches 120, HSYNC is high.

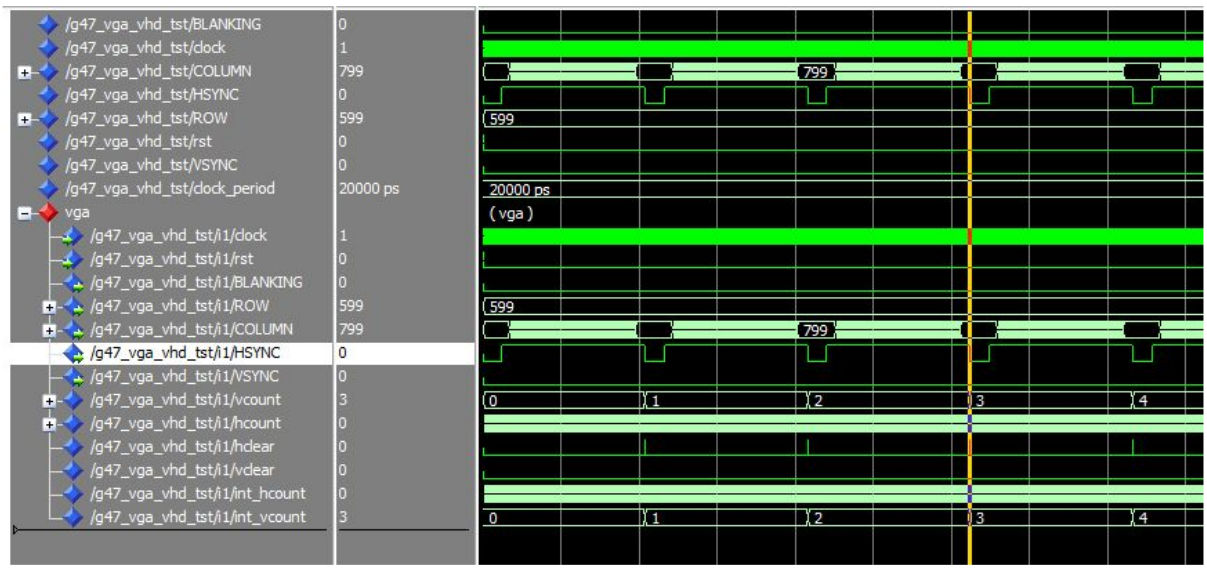


Fig 4

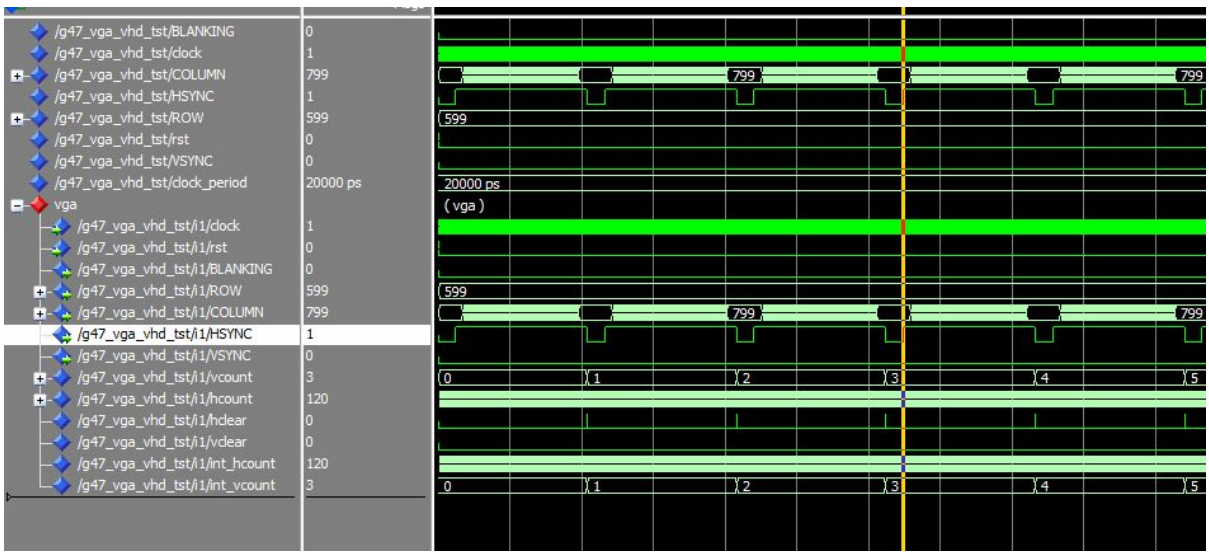


Fig 5

Figure 6, 7 and 8 shows the behaviour of the BLANKING signal regarding to visible area. We can see that BLANKING is low when vcount = 0 or hcount = 0 (Fig 6). It is high when vcount = 43 or hcount = 176 (fig 7). It is low again when vcount = 43 and hcount = 976 (Fig 8), note that in the last case it is the hcount value that triggers the BLANKING value to become low.

We also tested out the circuit using SignalTap II logic analyzer, show in Fig 9 and it too shows the expected outcomes.

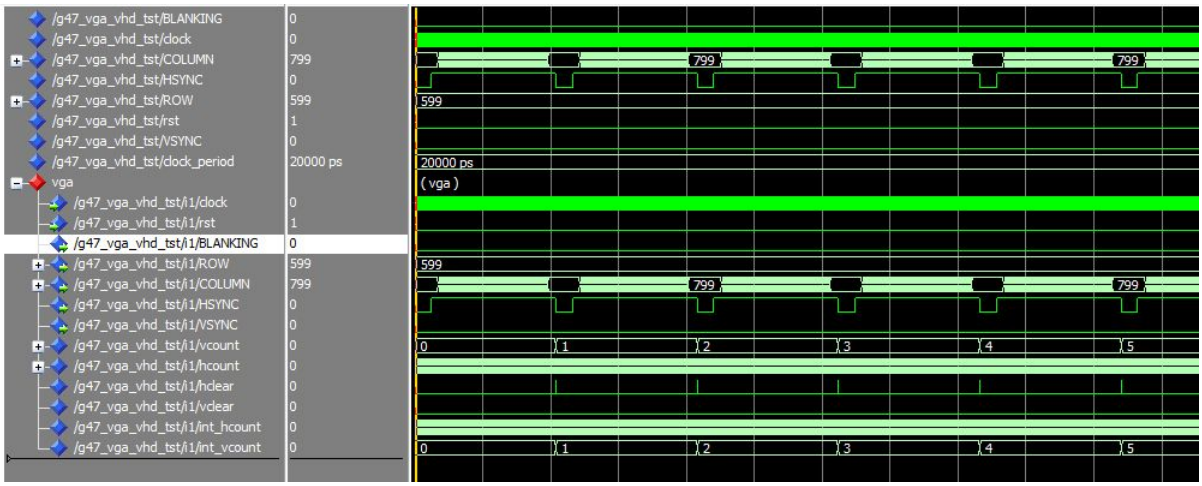


Fig 6

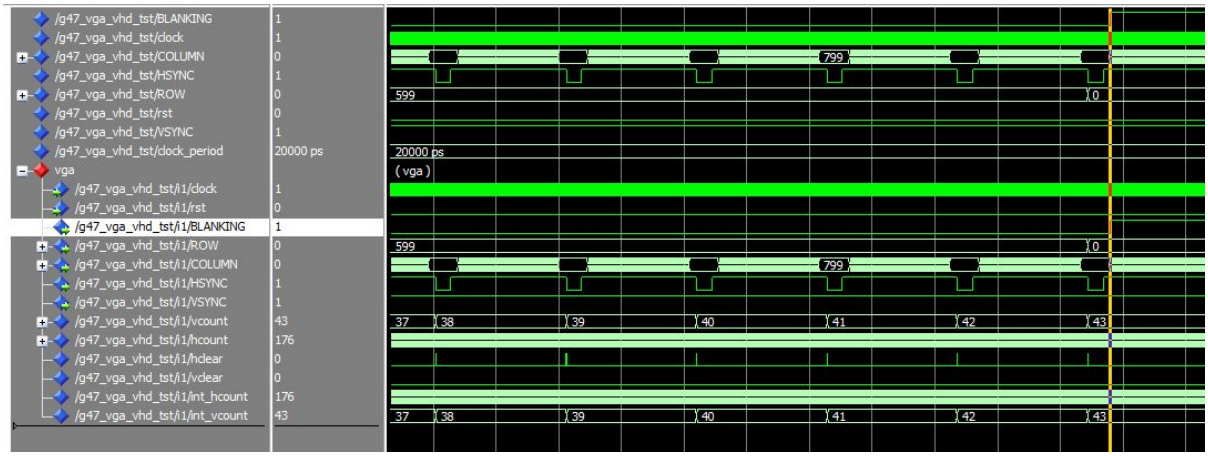


Fig 7

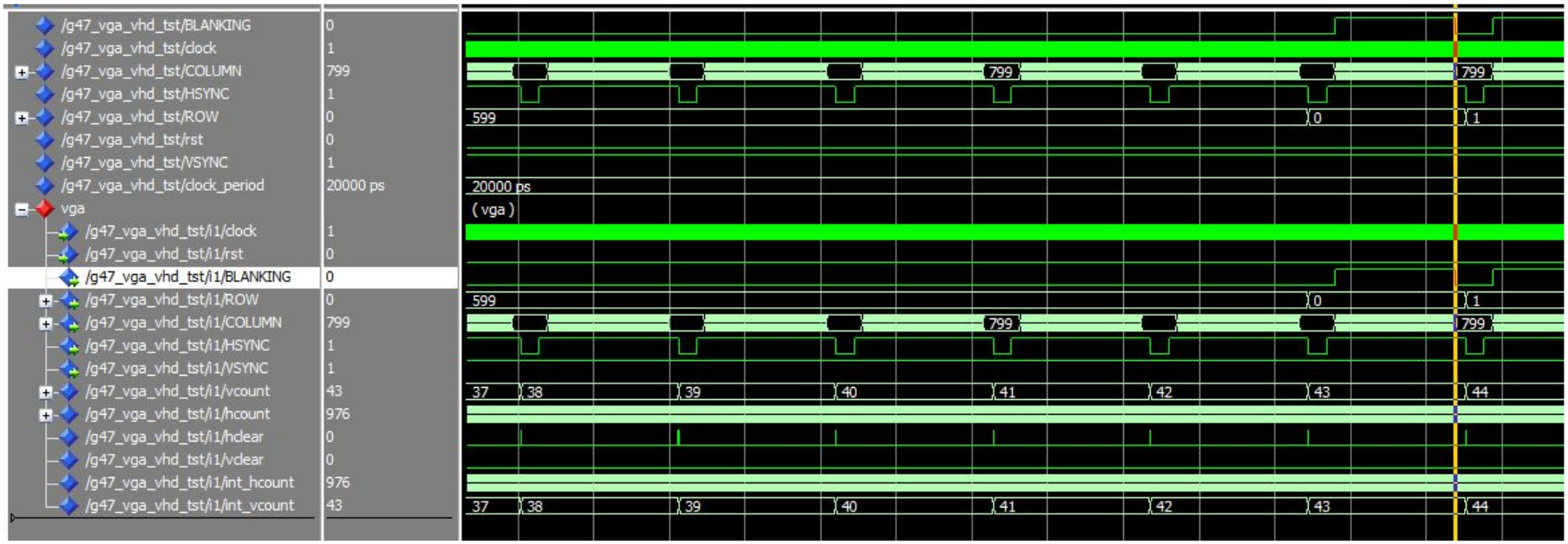
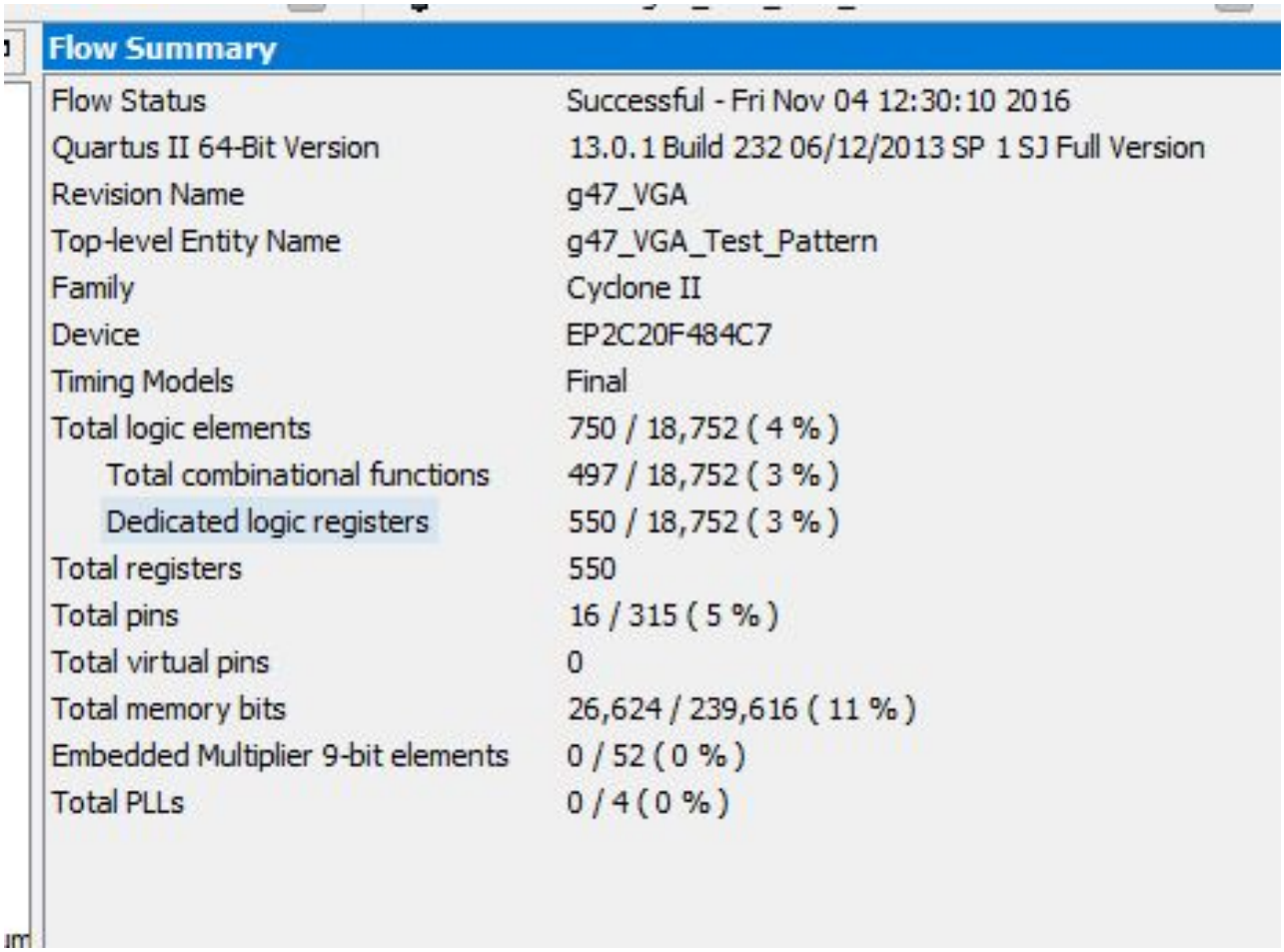

/g47_vga_vhd_tst/BLANKING
/g47_vga_vhd_tst/clock
/g47_vga_vhd_tst/COLUMN
/g47_vga_vhd_tst/HSYNC
/g47_vga_vhd_tst/ROW
/g47_vga_vhd_tst/rst
/g47_vga_vhd_tst/VSYNC
/g47_vga_vhd_tst/clock_period
vga
/g47_vga_vhd_tst/i1/clock
/g47_vga_vhd_tst/i1/rst
/g47_vga_vhd_tst/i1/BLANKING
/g47_vga_vhd_tst/i1/ROW
/g47_vga_vhd_tst/i1/COLUMN
/g47_vga_vhd_tst/i1/HSYNC
/g47_vga_vhd_tst/i1/VSYNC
/g47_vga_vhd_tst/i1/vcount
/g47_vga_vhd_tst/i1/hcount
/g47_vga_vhd_tst/i1/hclear
/g47_vga_vhd_tst/i1/vclear
/g47_vga_vhd_tst/i1/int_hcount
/g47_vga_vhd_tst/i1/int_vcount
0
1
799
1
0
0
1
20000 ps
1
0
0
0
799
1
1
43
976
0
0
976
43
599
799
20000 ps
(vga)
37
38
39
40
41
42
43
44

Fig 8


log: 2016/11/03 19:05:52 #0
click to insert time bar
Type
Alias
Name
-256
-128
0
128
256
384
512
640
768
896
1024
1152
1280
1408
1536
1664
1792
rst
BLANKING
COLUMN
31Fh
31Fh
ROW
257h
VSYNC
HSYNC

Fig 9

Summary of the FPGA resource utilization:



Flow Summary

Flow Status	Successful - Fri Nov 04 12:30:10 2016
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Full Version
Revision Name	g47_VGA
Top-level Entity Name	g47_VGA_Test_Pattern
Family	Cyclone II
Device	EP2C20F484C7
Timing Models	Final
Total logic elements	750 / 18,752 (4 %)
Total combinational functions	497 / 18,752 (3 %)
Dedicated logic registers	550 / 18,752 (3 %)
Total registers	550
Total pins	16 / 315 (5 %)
Total virtual pins	0
Total memory bits	26,624 / 239,616 (11 %)
Embedded Multiplier 9-bit elements	0 / 52 (0 %)
Total PLLs	0 / 4 (0 %)

Fig 9

Figure 9 shows the summary of FPGA resource utilization.

Grade Sheet for Lab #3

Fall 2016.

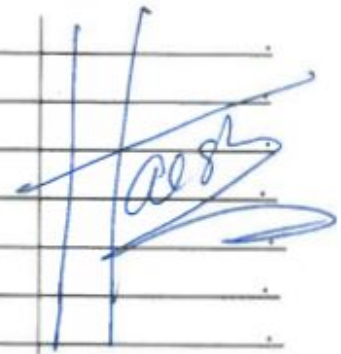
Group Number: 48

Group Member Name: SADNAN SAQUIF. Student Number: 260499660

Group Member Name: YIJIE ZHOU. Student Number: 260622641

Marks		
2	1.	VHDL for the VGA circuit
2	2.	Functional simulation of the VGA circuit
2	3.	Signal Tap II testing of the VGA circuit
2	4.	VHDL for the VGA test pattern generator
2	5.	Functional simulation of the VGA test pattern generator
2	6.	SignalTap II testing of the VGA test pattern generator
2	7.	Demonstration of the test pattern generator on a monitor

TA Signatures



Each part should be demonstrated to one of the TAs who will then give a grade and sign the grade sheet. Grades for each part will be either 0, 1, or 2. A mark of 2 will be given if everything is done correctly. A grade of 1 will be given if there are significant problems, but an attempt was made. A grade of 0 will be given for parts that were not done at all, or for which there is no TA signature.