ECSE 323 - Lab 4 Report

Group 47

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Description and Pinout/Symbol Diagram

Circuit name: g47_lab4 (this is modified VGA Test Pattern Circuit from lab 3)

Input(s): clock (1 bit), rst (1 bit), level (3 bit), life (3 bit)

Output(s): R, G, B (4 bit), HSYNC, VSYNC

Components: g47_VGA (lab 3), g47_Text_Address_Genenrator, g47_Text_generator, fontRom (given by professor), g47_VGA_Overlay and 2 instances of lpm_counter to generate score.

The name of the circuit is g47_lab4. The purpose of the circuit is to implement the score, level and life values on the screen. The circuit makes use of several components which are g47_VGA (lab 3), g47_Text_Address_Genenrator, g47_Text_generator, fontRom (given by professor) and the g47_VGA_Overlay. The purpose each of the components is described below. Fig. 2 shows how all the components are connected.

The circuit uses the components (described below) to generate the line of score, level and life. The score is also being generated and incremented here. This is done using 2 lpm_counters. The first counter goes from 0 to 2^24, and second goes from 0 to 2^16 (the max score value). Each time the first counter reaches its max value, the second counter is incremented by 1. This way the score increments slowly as the output of the second counter is set to be the score value. Also to take care of timing problems that make the output look ragged, a register was implemented here that makes sure that the required input is only updated on a rising clock edge, thus avoiding timing problems and making the output look smooth.

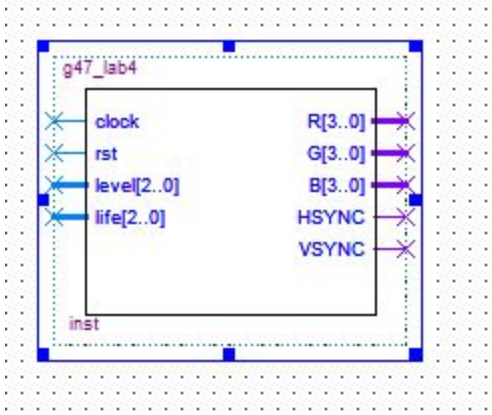


Fig. 1 Symbol Diagram

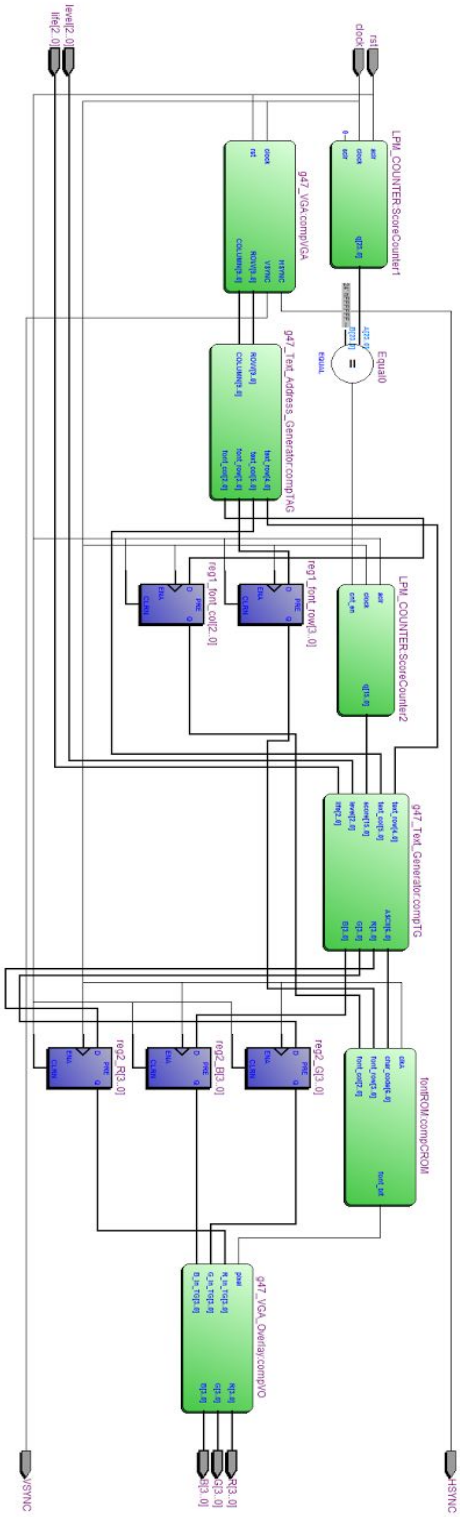


Fig. 2 Connection of all components

Component name: g47_VGA (from lab 3)

Input(s): clock (1 bit), reset (1 bit)

Output(s): BLANKING (1 bit), ROW (10 bit), COLUMN (10 bit), HSYNC (1 bit), VSYNC (1 bit)

Component(s): 2 instances of the lpm_counter from the lpm library

The purpose of g47_VGA has been explained in the previous lab 3 report.

Component name: g47_Text_Address_Generator

Input(s): ROW (10 bit), COLUMN (10 bit)

Output(s): text_row (5 bit), text_col (6 bit), font_row (4 bit), font_col (3 bit)

This divides the screen in a 19x50 grid. The formulas used to generate the text_row, text_col, font_row and font_col were given to us. Since the formulas were all divisions and modulus of powers of 2, we used bit operations instead of integer arithmetic to optimize our circuit. For example text_row =((ROW/2)%16) =((ROW/2^1)%2^4) which is the equivalent of right shifting the COLUMN by 1 spot and then taking the 4 LSB. Similar operations are carried on text_col, font_row and font_col.

Component name: g47_Text_Generator

Input(s): text_row (5 bit), text_col (6 bit), score (16 bit), level (3 bit), life (3 bit)

Output(s): ASCII (7 bit), R, G, B (4 bit)

The text generator is generating the text and values for score, life and level. It simply uses the text_row nad text_col to output the correct ASCII characters with the correct R,G,B values. It first checks if we are on text_row = 17 then it outputs the right ASCII-character on the screen by checking the text_col value. If text_row is not 17 it simply outputs space and the color black onto the screen.

Component name: frontRom (Given by prof.)

Input(s): clkA, char_code (7 bit), font_row (4 bit), font_col (4 bit)

Output(s): font_bit

This was given to us by the professor, it takes in the ASCII value from text generator circuit and it outputs the font_bit (pixel value) for the ASCII character.

Component name: g47_VGA_Overlay

Input(s): pixel, R_in_TG, G_in_TG, B_in_TG (4 bit)

Output(s): R, G, B (4 bit)

This circuit simply works like a mux for the R,G,B values using the pixel (font_bit) from the fontROM as the selection line. If the pixel bit is high it sets the R,G,B values to ones from the text generator otherwise it sets their values to “0000” which would simply give the colour black on the screen.

Testing:

The ModelSIM simulation below (Fig 3) was used to check to see if we get expected output values as we iterate through ROW and COLUMN values in the g47_Text_Address_Generator circuit. We got the expected results

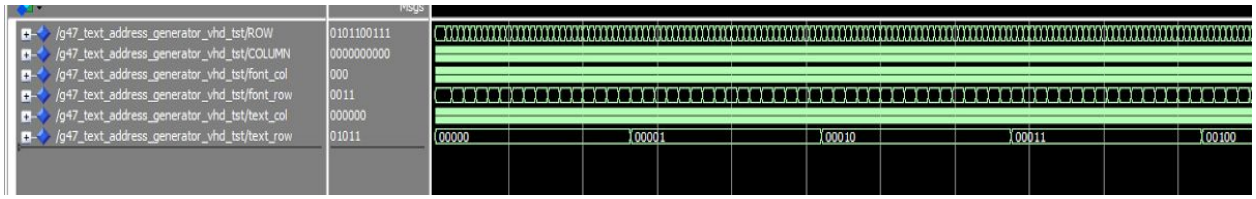


Fig. 3

We tested out rest of the circuit using the Altera DE1 board. The pin planner for which is shown below on Fig 4.

Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard	Reserved	Current Strength	Differential Pair
B[3]	Output	PIN_B10	3	B3_N0	PIN_B10	3.3-V LV...default)		24mA (default)	
B[2]	Output	PIN_A10	3	B3_N0	PIN_A10	3.3-V LV...default)		24mA (default)	
B[1]	Output	PIN_D11	3	B3_N0	PIN_D11	3.3-V LV...default)		24mA (default)	
B[0]	Output	PIN_A9	3	B3_N0	PIN_A9	3.3-V LV...default)		24mA (default)	
clock	Input	PIN_L1	2	B2_N1	PIN_L1	3.3-V LV...default)		24mA (default)	
G[3]	Output	PIN_A8	3	B3_N0	PIN_A8	3.3-V LV...default)		24mA (default)	
G[2]	Output	PIN_B9	3	B3_N0	PIN_B9	3.3-V LV...default)		24mA (default)	
G[1]	Output	PIN_C10	3	B3_N0	PIN_C10	3.3-V LV...default)		24mA (default)	
G[0]	Output	PIN_B8	3	B3_N0	PIN_B8	3.3-V LV...default)		24mA (default)	
HSYNC	Output	PIN_A11	3	B3_N0	PIN_A11	3.3-V LV...default)		24mA (default)	
level[2]	Input	PIN_V12	7	B7_N1	PIN_V12	3.3-V LV...default)		24mA (default)	
level[1]	Input	PIN_M22	6	B6_N0	PIN_M22	3.3-V LV...default)		24mA (default)	
level[0]	Input	PIN_L21	5	B5_N1	PIN_L21	3.3-V LV...default)		24mA (default)	
life[2]	Input	PIN_U11	8	B8_N0	PIN_U11	3.3-V LV...default)		24mA (default)	
life[1]	Input	PIN_U12	8	B8_N0	PIN_U12	3.3-V LV...default)		24mA (default)	
life[0]	Input	PIN_W12	7	B7_N1	PIN_W12	3.3-V LV...default)		24mA (default)	
R[3]	Output	PIN_B7	3	B3_N1	PIN_B7	3.3-V LV...default)		24mA (default)	
R[2]	Output	PIN_A7	3	B3_N1	PIN_A7	3.3-V LV...default)		24mA (default)	
R[1]	Output	PIN_C9	3	B3_N1	PIN_C9	3.3-V LV...default)		24mA (default)	
R[0]	Output	PIN_D9	3	B3_N0	PIN_D9	3.3-V LV...default)		24mA (default)	
rst	Input	PIN_L22	5	B5_N1	PIN_L22	3.3-V LV...default)		24mA (default)	
VSYNC	Output	PIN_B11	3	B3_N0	PIN_B11	3.3-V LV...default)		24mA (default)	
<<new node>>									

Fig. 4

The test results are shown below. In Fig 5 we see the score incremented to 106 from 0. We used the switches to set the level to 1 and lives to 7 (shown by the pink heart symbols).

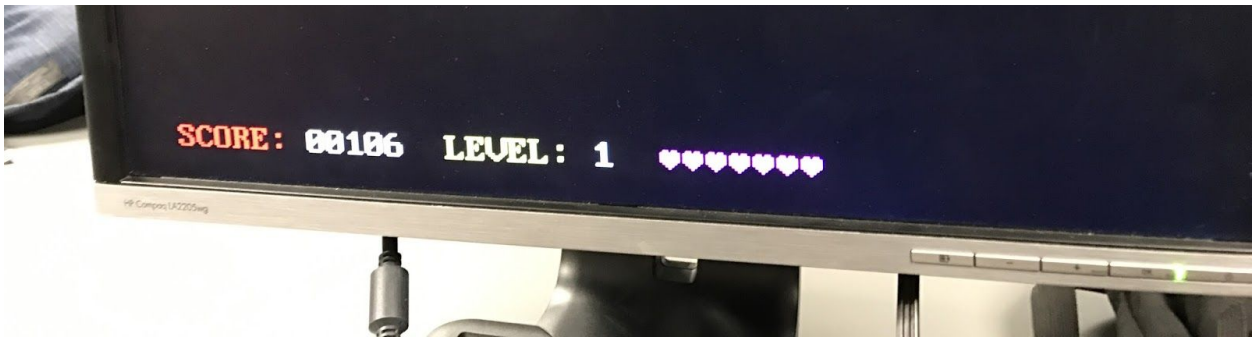


Fig. 5

In Fig 6 we see the score still increasing. We used the switches to set the level to 2 and lives to 6.

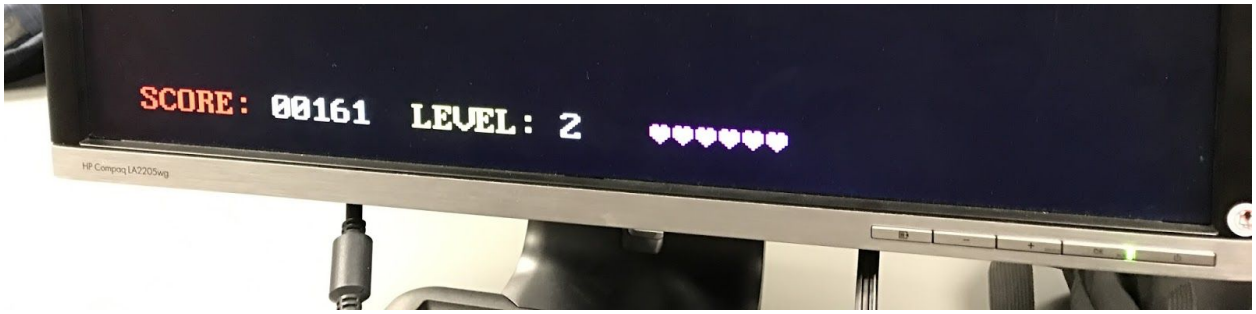


Fig. 6

In Fig 7 we see the score still increasing. We used the switches to set the level to 3 and lives to 5.

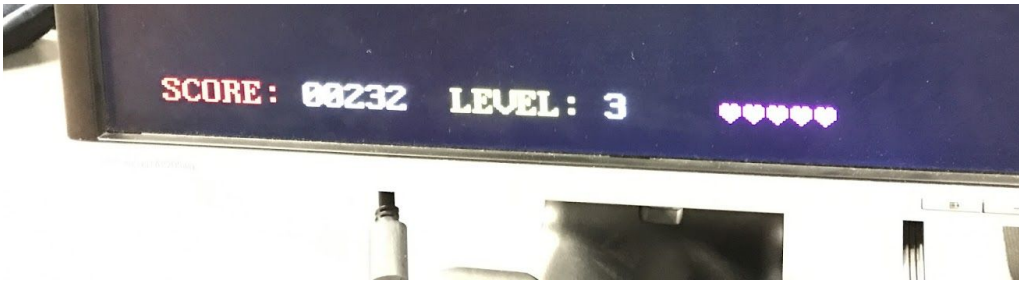


Fig. 7

In Fig 8 we see the score still increasing. We used the switches to set the level to 4 and lives to 4.

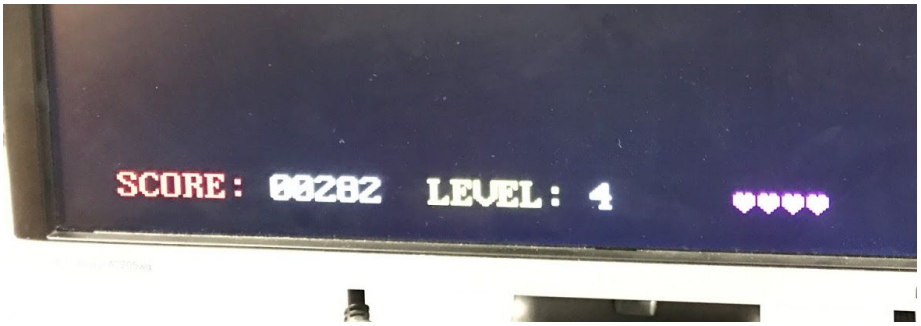


Fig. 8

In Fig 9 we see the score still increasing. We used the switches to set the level to 5 and lives to 3.

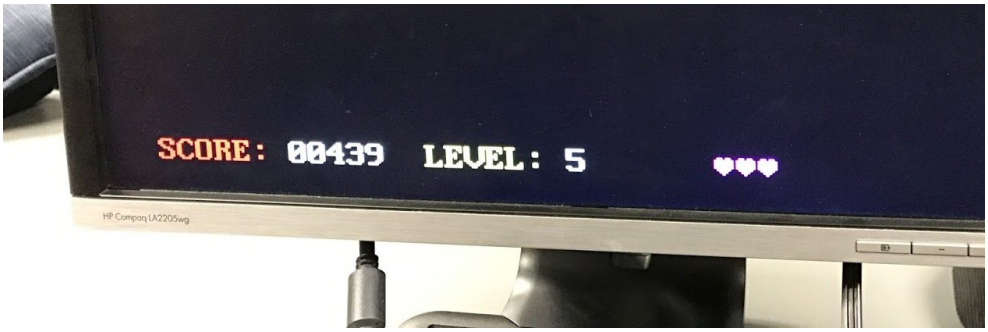


Fig. 9

In Fig 10 we see the score still increasing. We used the switches to set the level to 6 and lives to 2.

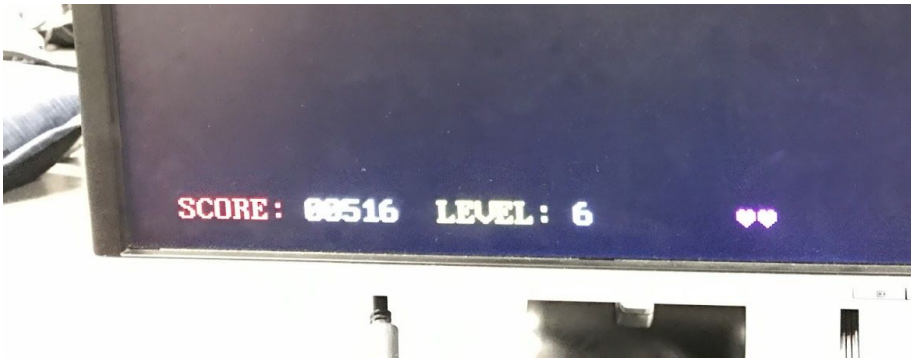


Fig. 10

In Fig 11 we see the score still increasing. We used the switches to set the level to 7 and lives to 1.

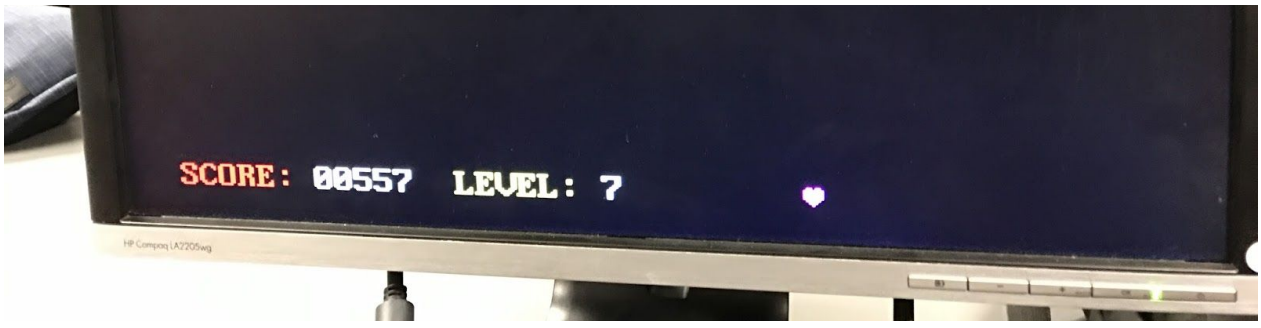


Fig. 11

In Fig 12 we see the score still increasing. We used the switches to set the level to 7 and no lives.

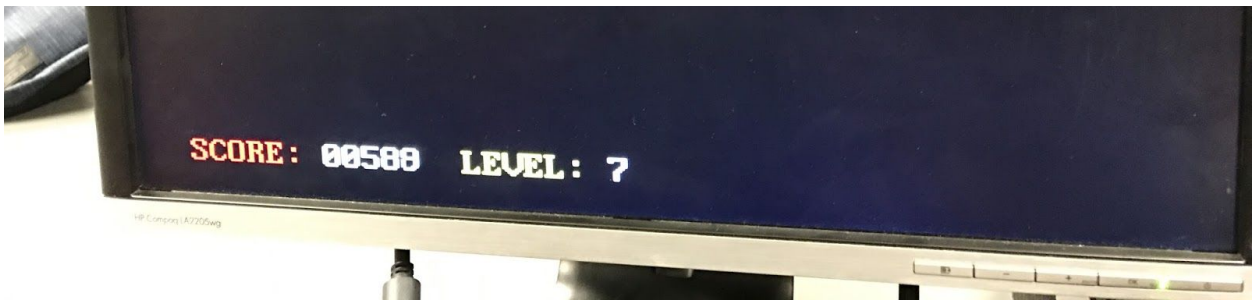
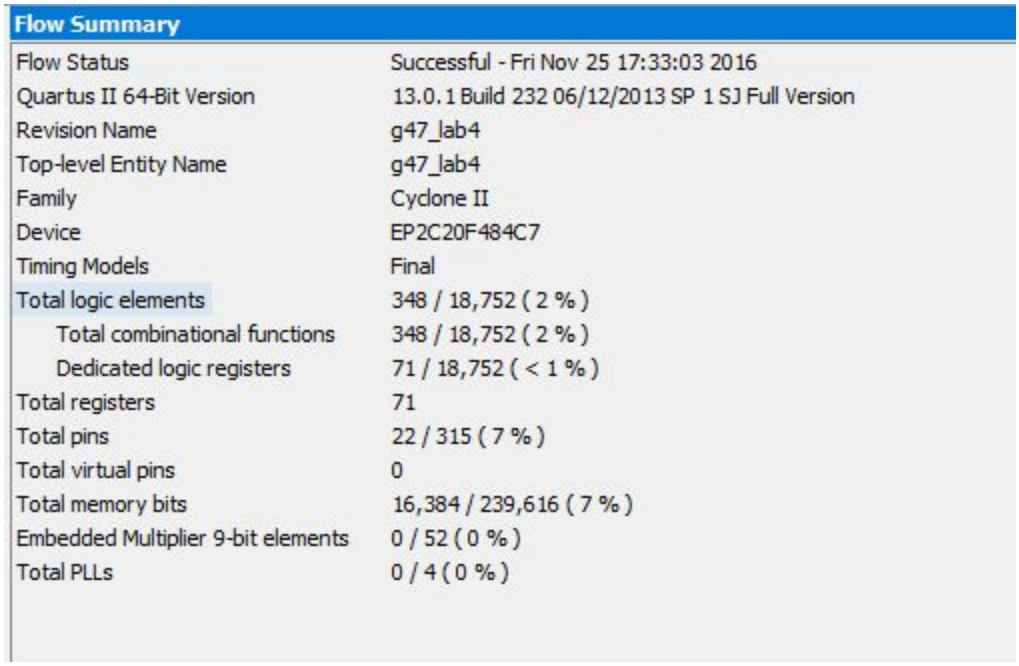


Fig. 12

Summary of the FPGA resource utilization:



Flow Summary	
Flow Status	Successful - Fri Nov 25 17:33:03 2016
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Full Version
Revision Name	g47_lab4
Top-level Entity Name	g47_lab4
Family	Cyclone II
Device	EP2C20F484C7
Timing Models	Final
Total logic elements	348 / 18,752 (2 %)
Total combinational functions	348 / 18,752 (2 %)
Dedicated logic registers	71 / 18,752 (< 1 %)
Total registers	71
Total pins	22 / 315 (7 %)
Total virtual pins	0
Total memory bits	16,384 / 239,616 (7 %)
Embedded Multiplier 9-bit elements	0 / 52 (0 %)
Total PLLs	0 / 4 (0 %)

Fig. 13

Summary of the timing performance:

Slack values are positive, and Fmax value is greater than 50 MHz (which is our clock speed).

Fast Model Hold Summary			
	Clock	Slack	End Point TNS
1	clock	0.243	0.000

Fig. 14

Slow Model Setup Summary			
	Clock	Slack	End Point TNS
etach	clock	1.313	0.000

Fig. 15

Slow Model Fmax Summary				
	Fmax	Restricted Fmax	Clock Name	Note
1	53.51 MHz	53.51 MHz	clock	

Fig. 16

Grade Sheet for Lab #4

Fall 2016.

Group Number: 47

Group Member Name: Sadman Sequif Student Number: 260499660

Group Member Name: Yijie Zhao Student Number: 260622641

Marks			TA Signatures
2	1.	VHDL description of the text address generator circuit	Arash
2	2.	Simulation of the text address generator circuit	Arash
2	3.	VHDL description of the text generator circuit	AL
2	4.	VHDL description of the modified test pattern generator	AL
2	5.	VGA monitor display from modified test pattern generator	[illegible]
2	6.	TimeQuest timing analysis results	Arash
2	7.	Money savings due to using lower speed grade	

Each part should be demonstrated to one of the TAs who will then give a grade and sign the grade sheet. Grades for each part will be either 0, 1, or 2. A mark of 2 will be given if everything is done correctly. A grade of 1 will be given if there are significant problems, but an attempt was made. A grade of 0 will be given for parts that were not done at all, or for which there is no TA signature.