Group 47
Yijie zhou 260622641
Sadnan Saquif 260499660

G47_keyboard_encoder: encodes an array of 64 bit data into 7 bits

Circuit name: g47_keyboard_encoder
Input(s): keys (64 bits)
Output(s): ASCII_CODE: (7 bits)
Component(s): g47_64_6_encoder

Description:
The function of the keyboard encoder is to take the value of the 64 bit input and map it onto a 7 bit output. This is done via a 64:6 encoder that the keyboard encoder uses as its component.
First we know that only one bit can be high, have a value of 1, in our input. Hence we can have 64 distinct valid values for our input. The 64 values represent the numeric values 0 to 63 and that can be represented by 6 bits. Therefore we take the 64 inputs pass it into our 64:6 encoder and and get a 6 bit output. Now we have to convert this 6 bit intermediary output to a 7 bit output. From the given 7 bit ascii table in the slides (Fig 1), we had to map the 64 possible output values to the 64 keys represented by columns 2,3,4 and 5 and rows 0 -15 (F). To do this, we reserve the first 3 bits for the column number and the last 4 bits for the row number. For example: a 6 bit input of ‘000000’ represents column 2 row 0, therefore the output should be ‘0100000’, where 010 represents column 2 and ‘0000’ represents row 0. On further inspection we can see that the possible values for the first 3 bits are ‘010’, ’011’, ‘100’ and ‘101’ which are columns 2,3,4 and 5 respectively. Hence if the msb is ‘0’, we set the leftmost 2 bits to ‘01’ else if msb is ‘1’ we set it to ‘10’ and then concatenate the remaining 5 bits to the end of it. This completes our code for the keyboard encoder.

	0	1	2	3	4	5	6	7
0	NUL	DLE	SP	0	@	P	`	p
1	SOH	DC1	!	1	A	Q	a	q
2	STX	DC2	"	2	B	R	b	r
3	ETX	DC3	#	3	C	S	c	s
4	EOT	DC4	$	4	D	T	d	t
5	ENQ	NAK	%	5	E	U	e	u
6	ACK	SYN	&	6	F	V	f	v
7	BEL	ETB	'	7	G	W	g	w
8	BS	CAN	(	8	H	X	h	x
9	HT	EM	)	9	I	Y	i	y
A	LF	SUB	*	:	J	Z	j	z
B	VT	ESC	+	;	K	[	k	{
C	FF	FS	,	<	L	\	l	|
D	CR	GS	-	=	M	]	m	}
E	SO	RS	.	>	N	^	n	~
F	SI	US	/	?	O	_	o	DEL

Fig 1

Symbol diagram:

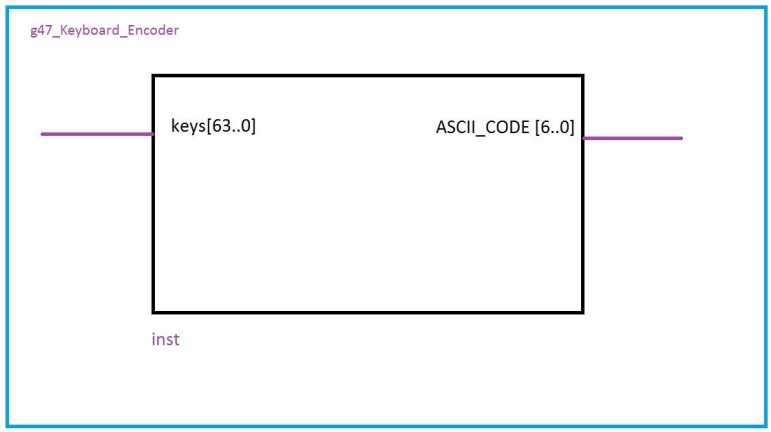

Fig 2

Gate level schematic diagrams

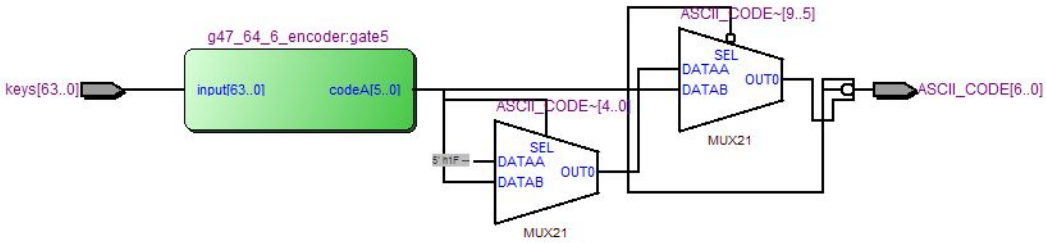

Fig 3

Testing:

First we test to see if we get the expected outcome with the valid inputs for the 64:6 encoder, i.e. there is only one bit with value 1 in the 64-bit input sequence. This is done using a for loop. Then we checked one 1s in the 64 bit input sequence. Show in the figure below.

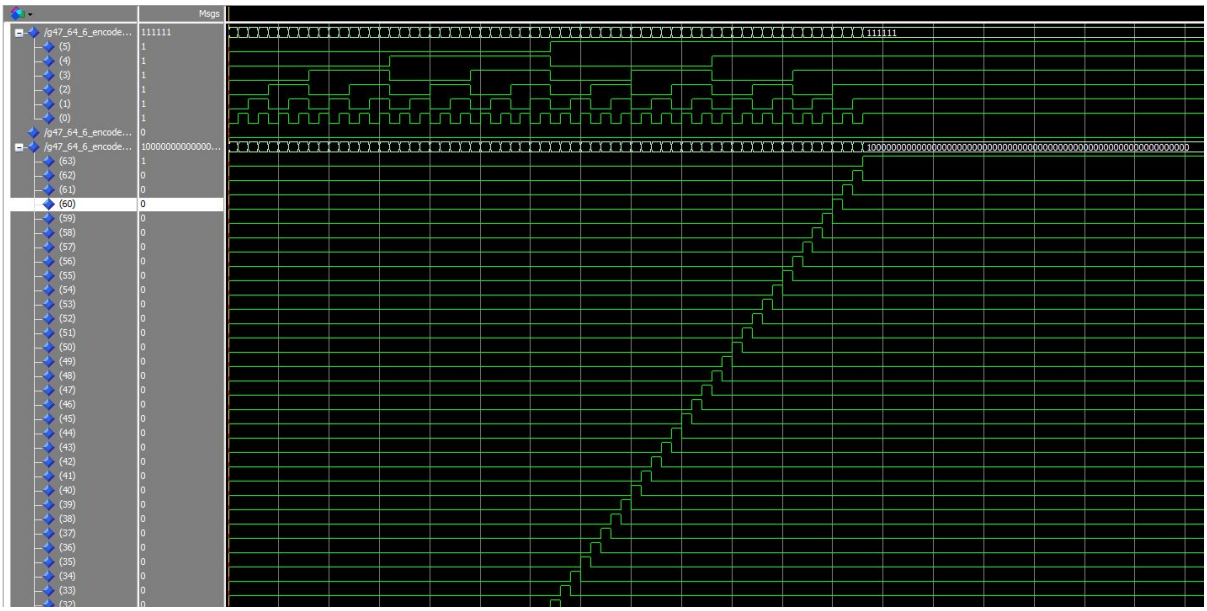

Fig 4

We implemented a similar loop for testing the keyboard encoder, the loop generates all 64 valid values and the encoder should then convert them as described above. We also test to see what happens if our initial input has more than 1 bit with value 1. The bit with the lowest index is considered as expected. The expected outcome is produced and can be seen in figure 5.

We tested the encoder on the DE1 board using a selected signal assignment (code in g47_7_segment_decode.vhd). We use a selected signal assignment to hard code the 36 values (10 numerics and 26 letters) so that they can be correctly represented in the LED display. Since there are only 10 switches on the board, we decided to use them to represent the numbers 0 - 9. To do so we kept the first 38 bits and the last 16 bits to 0 and took the middle 10 bits from the input lines (code in g47_7_ALTERA_segment_decoder). This 10 values represent the numbers 0-9 and when the code is uploaded into the ALTERA DE1 board, and turn on the switches, the numbers 0 to 9 is shown on the LED display, depending on the switch with the lowest index that is on.

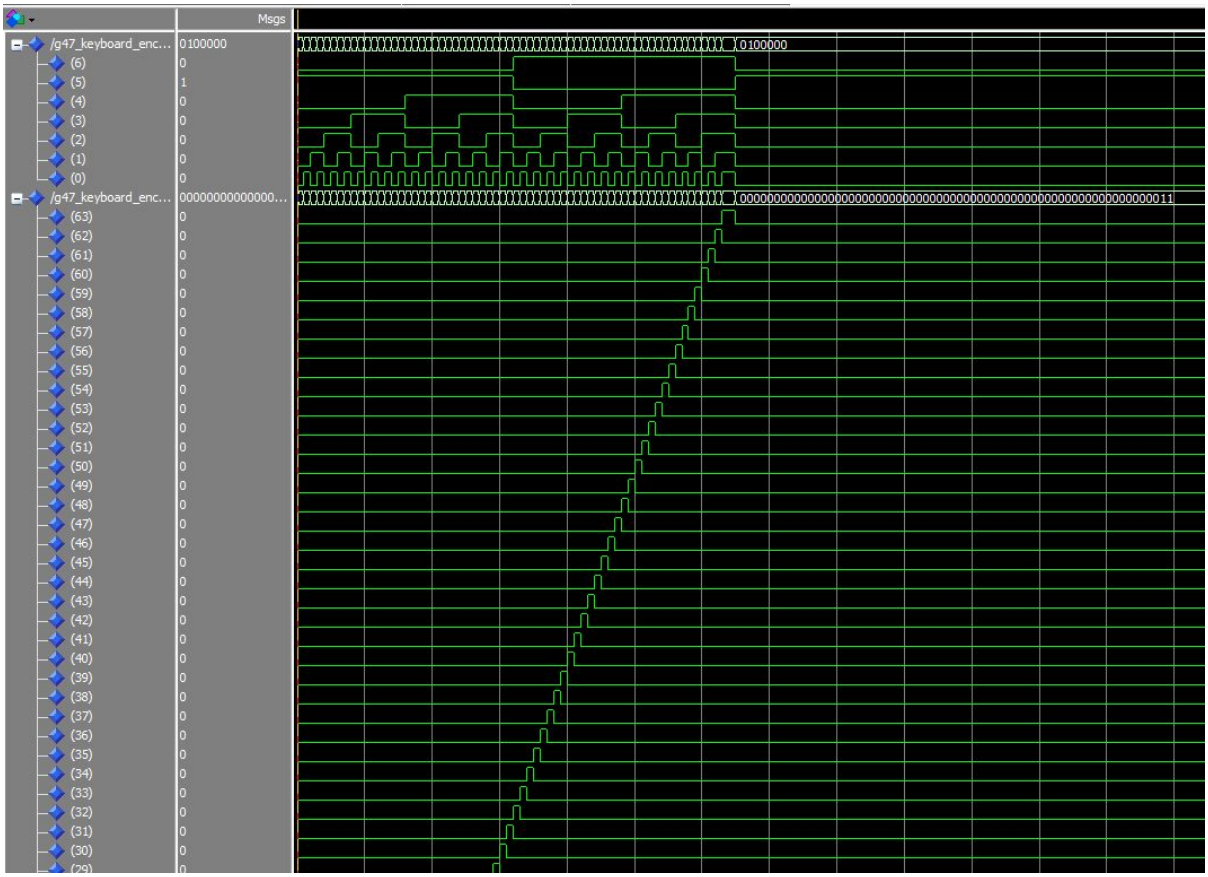
Msgs
/g47_keyboard_enc...
0100000
(6)
(5)
(4)
(3)
(2)
(1)
(0)
/g47_keyboard_enc...
00000000000000...
(63)
(62)
(61)
(60)
(59)
(58)
(57)
(56)
(55)
(54)
(53)
(52)
(51)
(50)
(49)
(48)
(47)
(46)
(45)
(44)
(43)
(42)
(41)
(40)
(39)
(38)
(37)
(36)
(35)
(34)
(33)
(32)
(31)
(30)
(29)
0100000
00000000000000000000000000000000000000000000000000000000000011

Fig 5

Grade Sheet for Lab #2

Fall 2016.

Group Number: 47

Group Member Name: Sadhan Saquef. Student Number: 260499660

Group Member Name: Yijie Zhou. Student Number: 260622641

Marks		
2	1.	VHDL code for the *64:6 encoder* circuit
2	2.	Simulation of the *64:6 encoder* circuit
2	3.	VHDL code for the *keyboard encoder* circuit
2	4.	Simulation of the *keyboard encoder* circuit
2	5.	VHDL code for the *7_segment_decoder* circuit
2	6.	Simulation of the *7_segment_decoder* circuit
2	7.	Testing of the *7_segment_decoder* circuit on the DE1 board

TA Signatures

Each part should be demonstrated to one of the TAs who will then give a grade and sign the grade sheet. Grades for each part will be either 0, 1, or 2. A mark of 2 will be given if everything is done correctly. A grade of 1 will be given if there are significant problems, but an attempt was made. A grade of 0 will be given for parts that were not done at all, or for which there is no TA signature.