Ryerson University

Department of Electrical, Computer, & Biomedical Engineering
Faculty of Engineering & Architectural Science

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Instructor:	Khalid Abdel Hafeez

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Assignment/Lab Title:	Data Memory Module

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Student LAST Name	Student FIRST Name	Student Number	Section	Signature*
Sarim	Shahwar	501109286	12	SS

*By signing above you attest that you have contributed to this written lab report and confirm that all work you have contributed to this lab report is your own work. Any suspicion of copying or plagiarism in this work will result in an investigation of Academic Misconduct and may result in a "0" on the work, an "F" in the course, or possibly more severe penalties, as well as a Disciplinary Notice on your academic record under the Student Code of Academic Conduct, which can be found online at: http://www.ryerson.ca/senate/current/pol60.

Lab Objective:

Data memory is a crucial part of the CPU architecture. The primary objective of this lab is to design, implement, simulate, and test the data memory system. The memory unit is capable of reading and writing data within a clock cycle. The data memory functions are listed below:

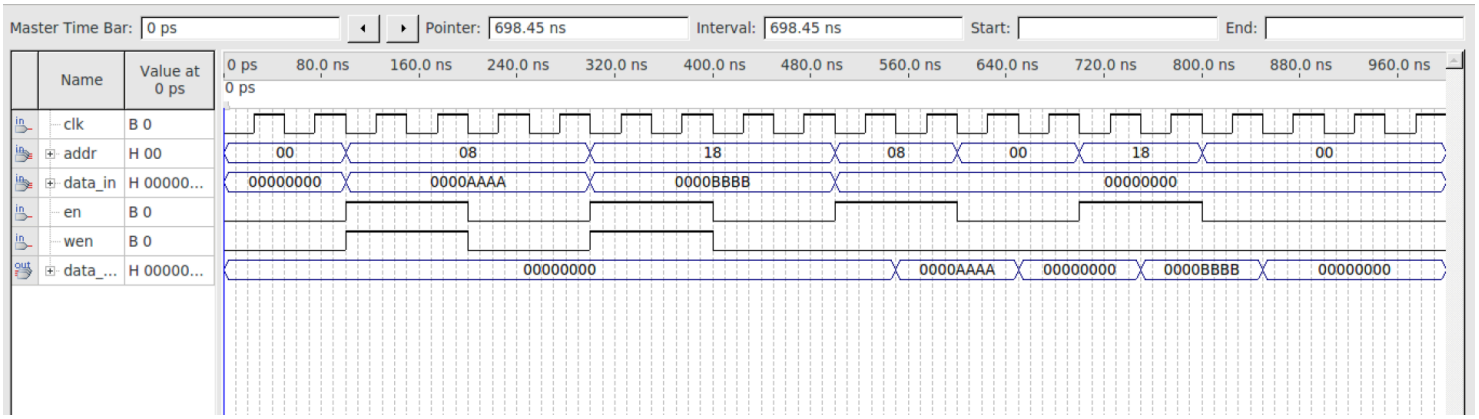
en (Enable Signal Input)	wen (Write Enable Signal)	Function	data_out (Data Output)
0	X	N/A	0
1	0	Read	M[addr]
1	1	Write M[addr] <= data_in	0

Experiment Details:

Data-Memory VHDL: The program below is the VHDL code for a data memory module. This program functions using 32 bits. The address is allocated with 8 bits, while the data input and output are allocated with 32 bits. The RAM is an array with 256 32-bit data memory space but is set to 32 bits as the system is running a 32-bit process. The program consists of a few “if” and “else” statements. In summary, the program checks if there is a rising edge on the clock and enables the “en” function, which is the enable signal input. The “wen” function is the write enable signal input, which means if there is data in the input, the “wen” function will write the data input into a set address. The “en” function is like a call function, where if “en” is enabled over a certain memory location, it will display the input set in that memory location in the data output.

```
1   library ieee;
2   use ieee.std_logic_1164.all;
3   use ieee.numeric_std.all;
4
5   entity data_mem is
6   port(
7       clk, wen, en    :  in std_logic; --clock, Wirte enable signal input, enable signal input
8       addr            :  in unsigned(7 downto 0); --address 8-bit
9       data_in         :  in std_logic_vector(31 downto 0);
10      data_out        :  out std_logic_vector(31 downto 0)
11  );
12  end data_mem;
13
14  architecture Behavior of data_mem is
15      type RAM is array (0 to 255) of std_logic_vector(31 downto 0); --256 32-bit data memory space
16      signal DATAMEM    : RAM; -- actual data memory space
17  begin
18      process(clk, en, wen)
19      begin
20           if(clk'event and clk='0') then --Checks if there is a rising edge on the clock
21          if(en = '0') then --enable en if a rising edge
22              data_out <= (others => '0'); --else sets data_out as all 0's
23          else
24              if(wen = '0') then --If wen = 0: read mode
25                  data_out <= DATAMEM(to_integer(addr));
26              end if;
27              if(wen = '1') then --if wen = 1: write mode
28                  DATAMEM(to_integer(addr)) <= data_in;
29                  data_out <= (others => '0');
30              end if;
31          end if;
32          end if;
33      end process;
34  end Behavior;
35
```

Results: The waveform below displays the function of the Data memory VHDL code. The waveform includes the clock, the data address, the data input, the enable signal input, the write enable signal and the data output. The data addresses which are given from the lab manual are the following: 00,08,18. In addition, the data inputs given include the hexadecimal values of “00000000”, “0000AAAA” and “0000BBBB”.



Discussion:

Data memory is a crucial function which exists within a CPU. Its main function is to store program data at various data addresses and display the stored data when the input signal is enabled. The waveform has a clock that is at a constant interval. The data addresses are set as “00”, “08”, and “18”. The data input of “0000AAAA” is under the data address of “08,” while the input of “0000BBBB” is under the data address of “08”. The value of “0000AAAA” is stored at the data address of “08” as the write enable signal is high. This is repeated at the data address of “18” where the value of “0000BBBB” is stored. For the output section, the enabled input signal is on the rising edge over the data address of “08” and “18”, which basically calls the data store at those data addresses and displays it in the data output section. Since there was no value stored in the data addresses of “0”, the output will always be set to “0”.