

Course Title:	Computer Organization and Architecture
Course Number:	COE628
Semester/Year (e.g.F2016)	W2024

Instructor:	Khalid Abdel Hafeez
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Assignment/Lab Number:	6
Assignment/Lab Title:	The Complete CPU

Submission Date:	2024/04/11
Due Date:	2024/04/12

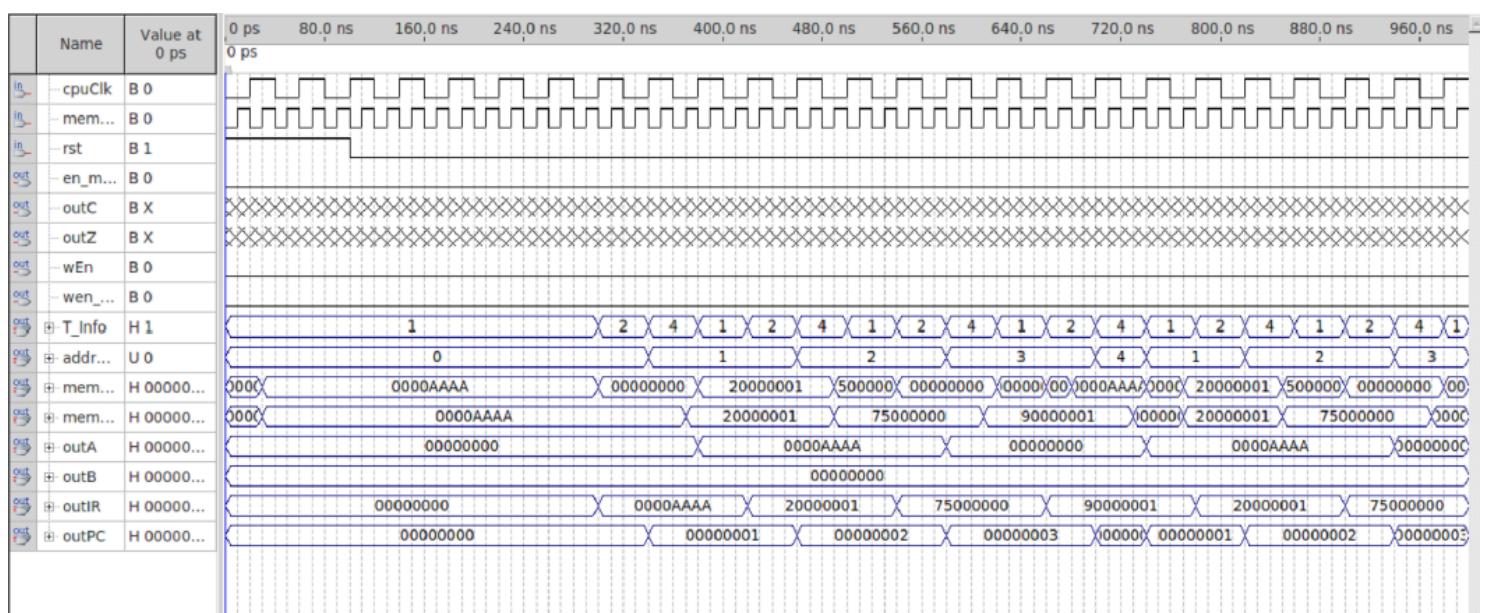
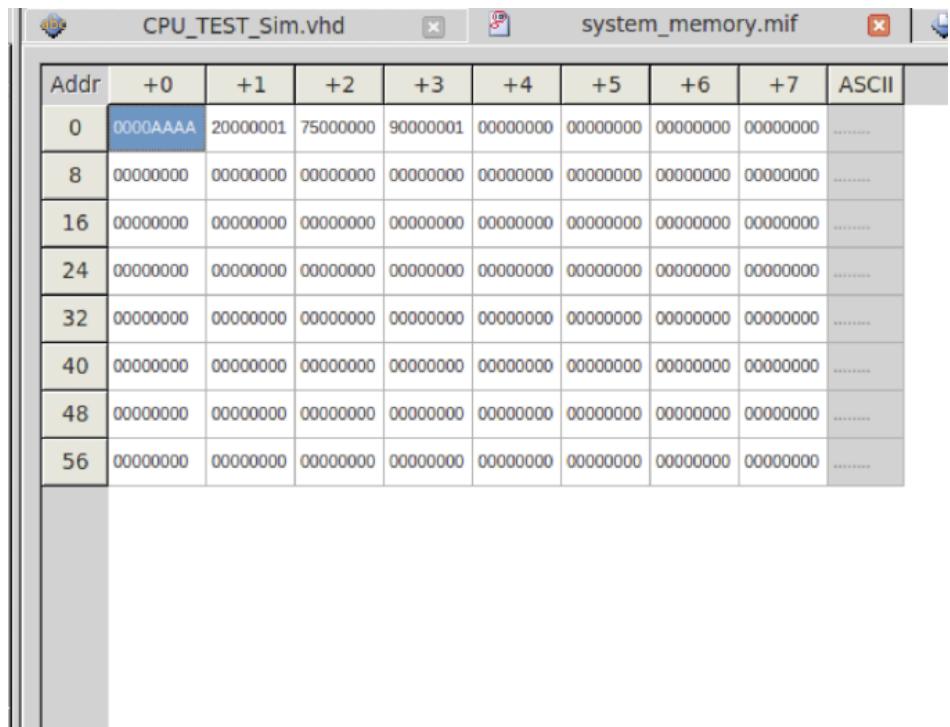
Student LAST Name	Student FIRST Name	Student Number	Section	Signature*
Sarim	Shahwar	501109286	12	SS

*By signing above you attest that you have contributed to this written lab report and confirm that all work you have contributed to this lab report is your own work. Any suspicion of copying or plagiarism in this work will result in an investigation of Academic Misconduct and may result in a “0” on the work, an “F” in the course, or possibly more severe penalties, as well as a Disciplinary Notice on your academic record under the Student Code of Academic Conduct, which can be found online at: <http://www.ryerson.ca/senate/current/pol60>.

Lab Objective:

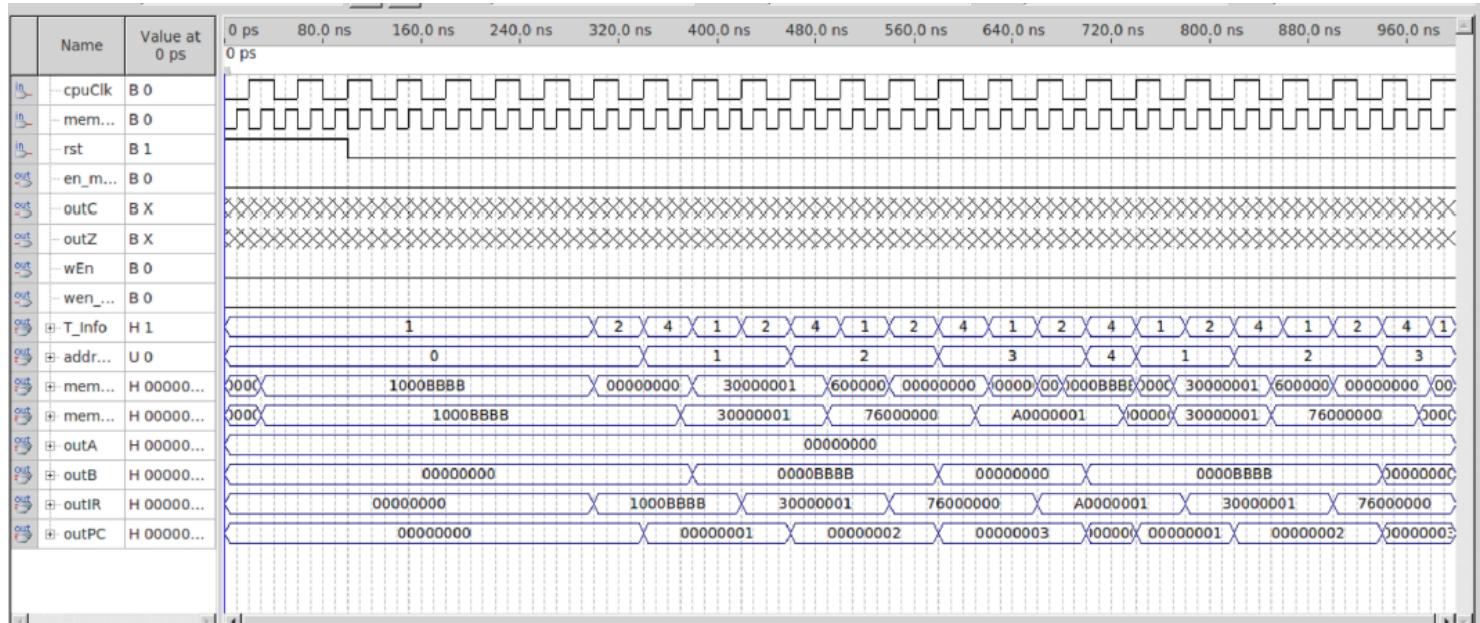
The objective of this lab was to apply knowledge and skills in a practical context to design and implement a complete CPU system. This CPU system included a reset circuit, a datapath, a controller and several other smaller components such as ‘add’ and ‘increment’ functions. The CPU system design is a collection of all of the previous labs which were all merged to create a functional CPU system, which is displayed using waveforms.

Simulations Results: LDAI, STA, CLRA, LDA



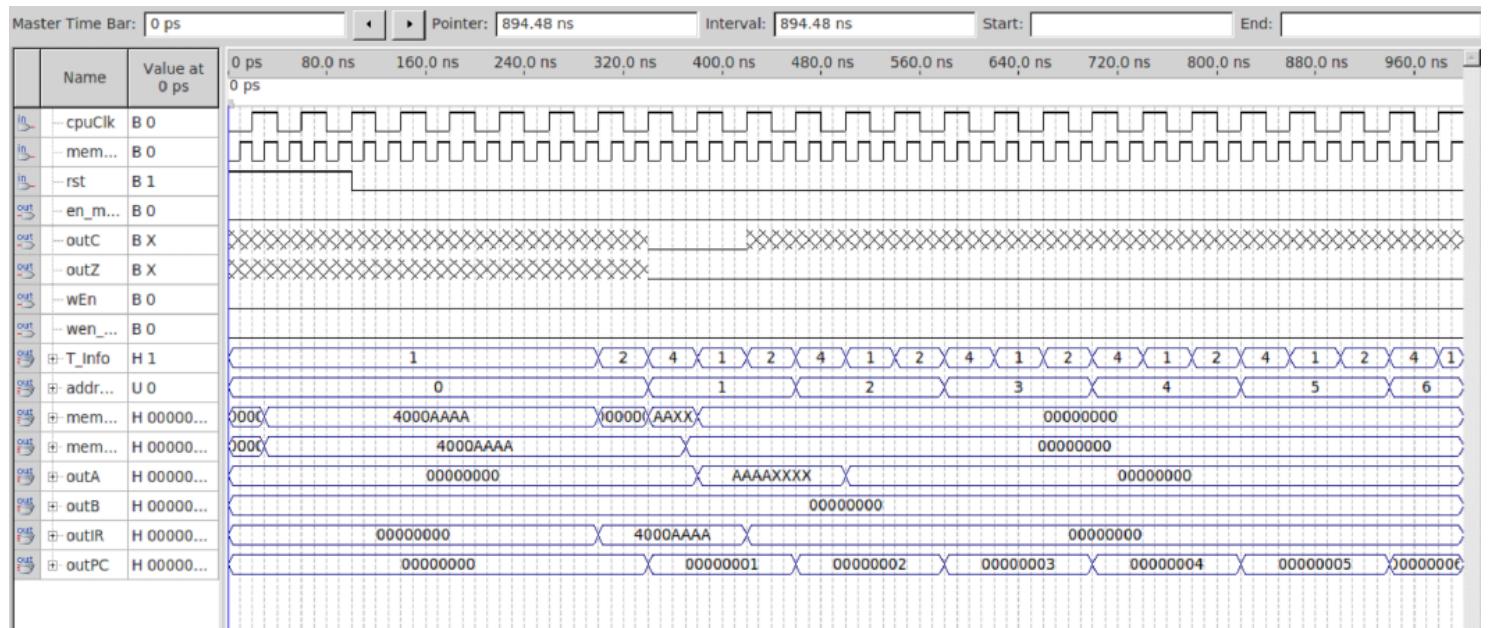
LDBI, STB, CLRb, LDB

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32	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	
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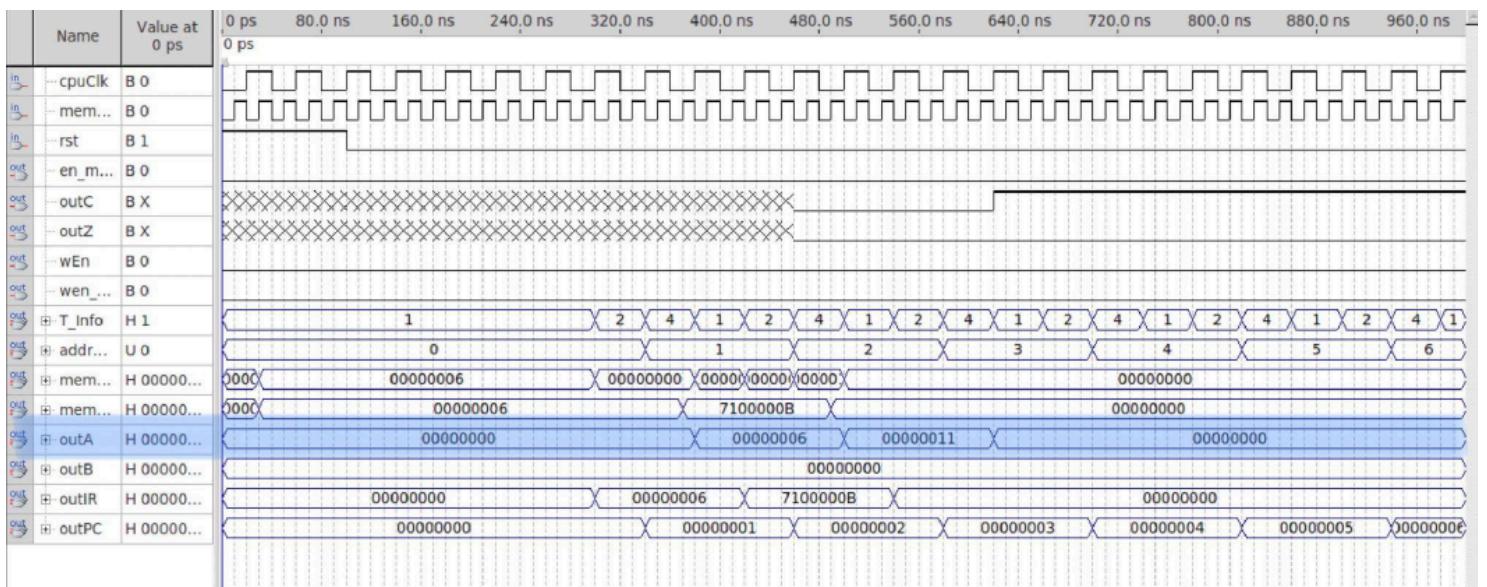
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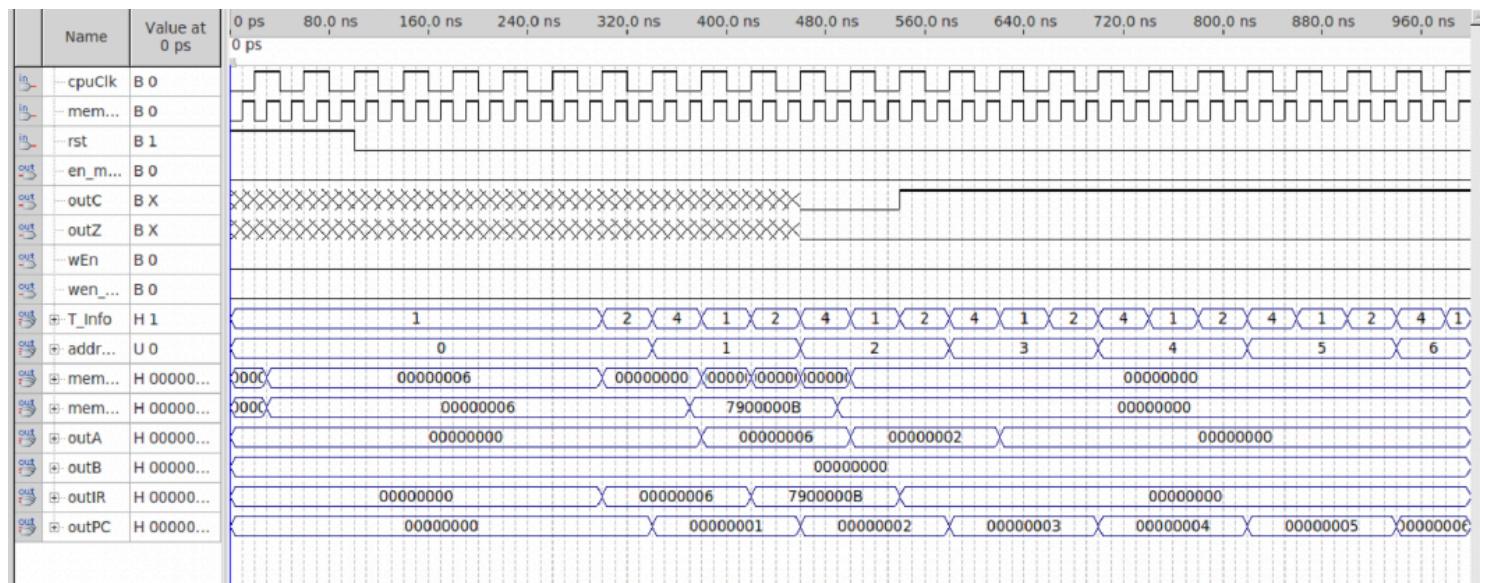
ADDI

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24	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	
32	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	
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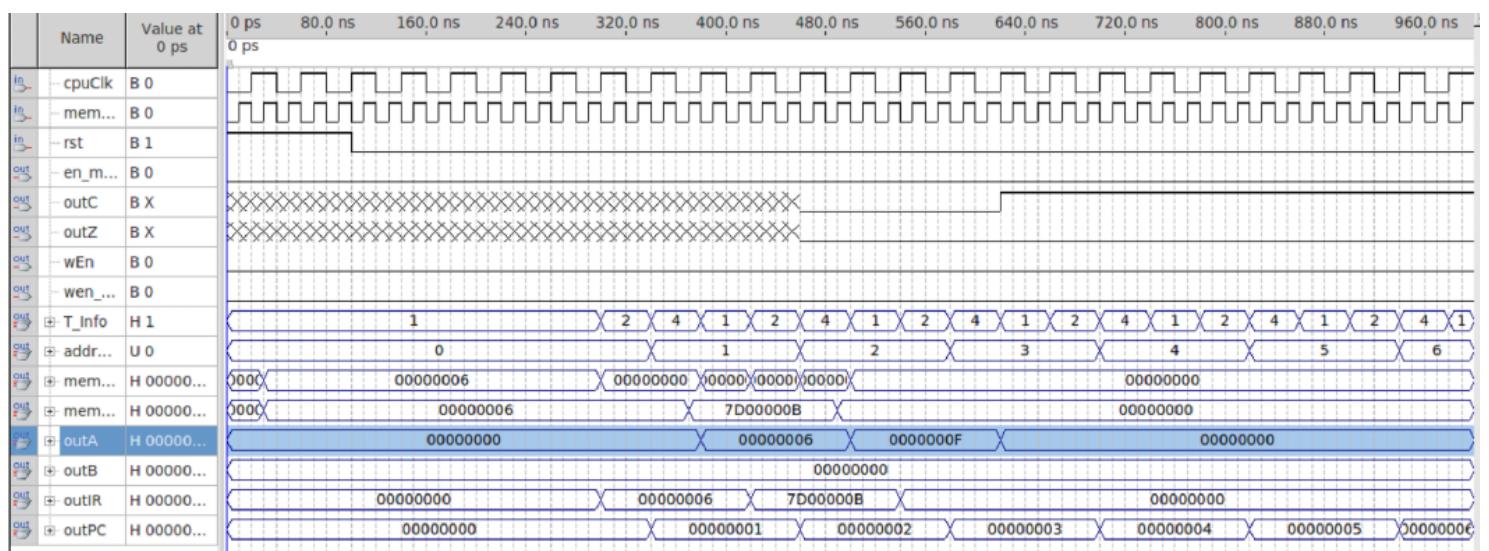
ANDI

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16	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	
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32	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	
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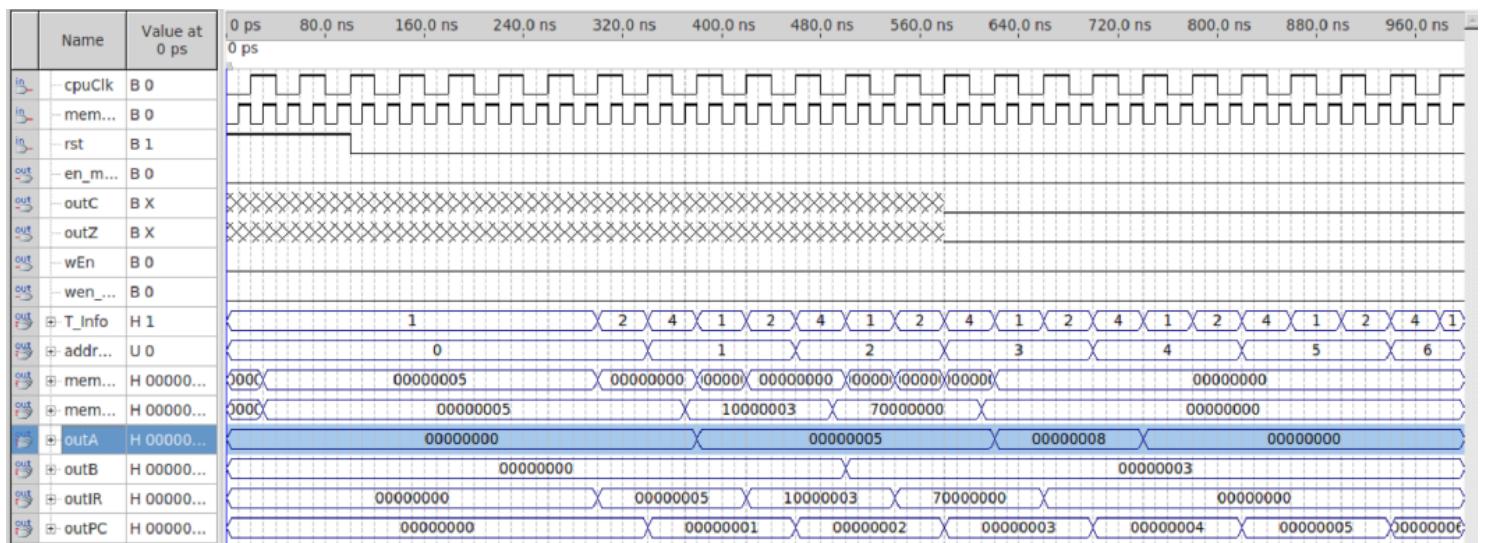
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16	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000
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32	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000
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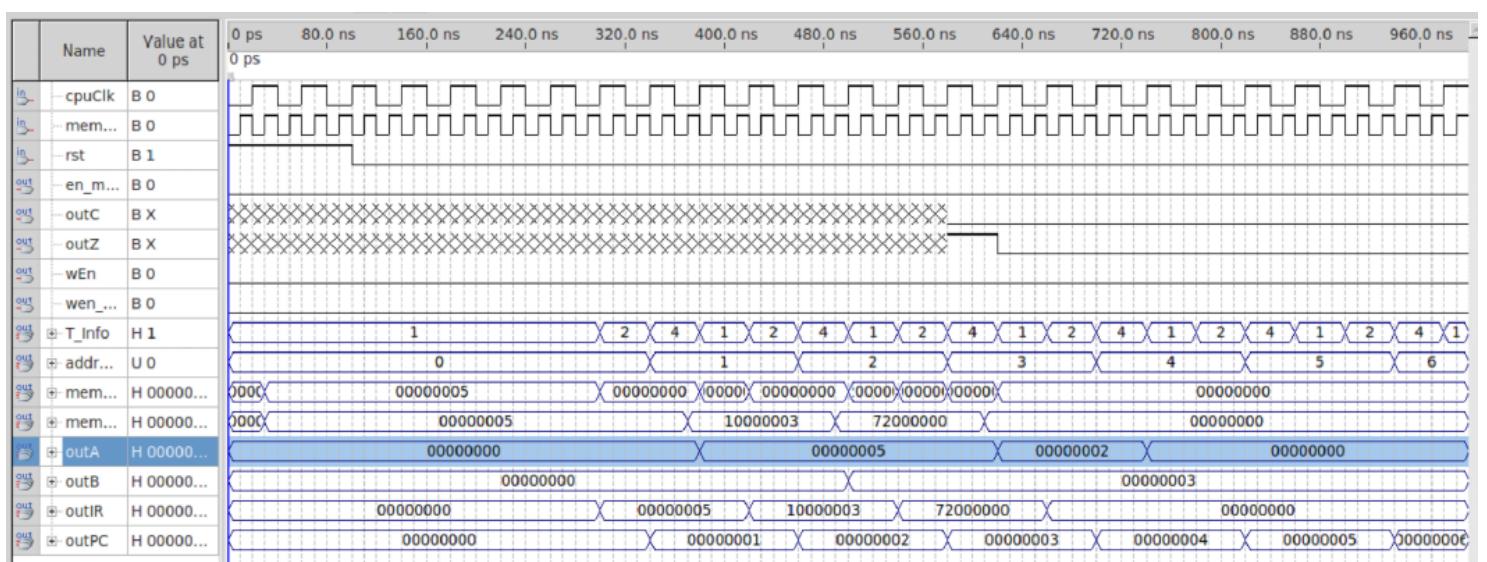
ADD

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32	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	
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56	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	



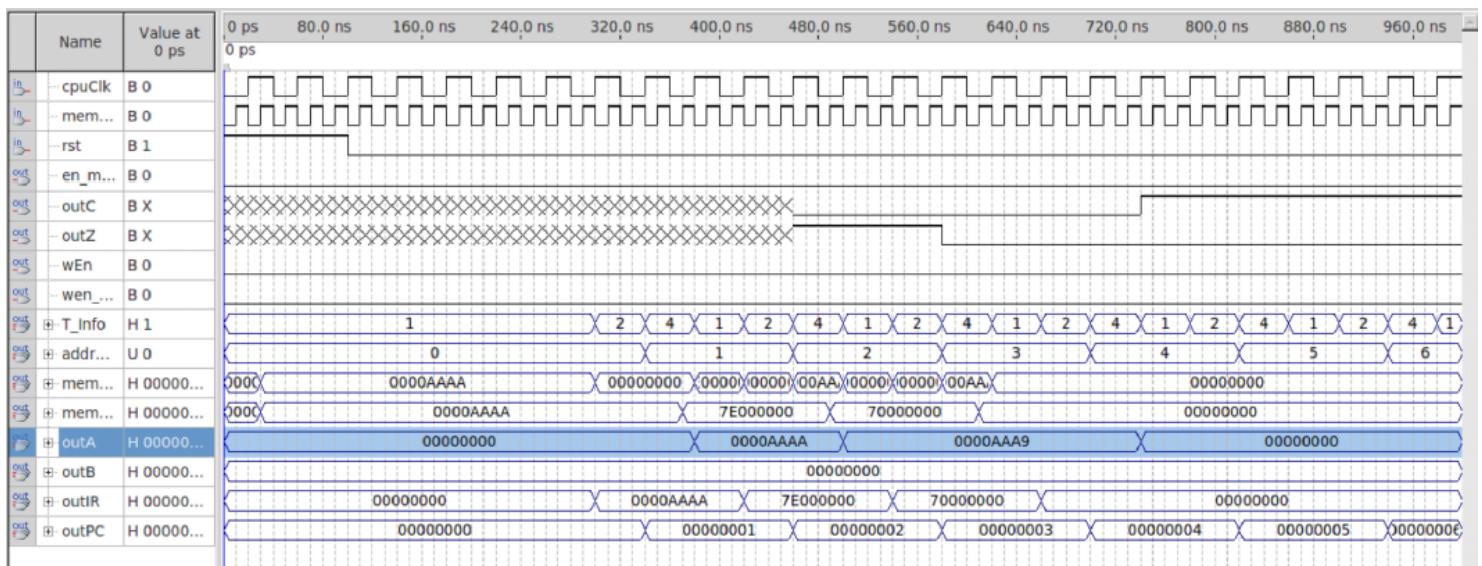
SUB

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8	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	
16	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	
24	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	
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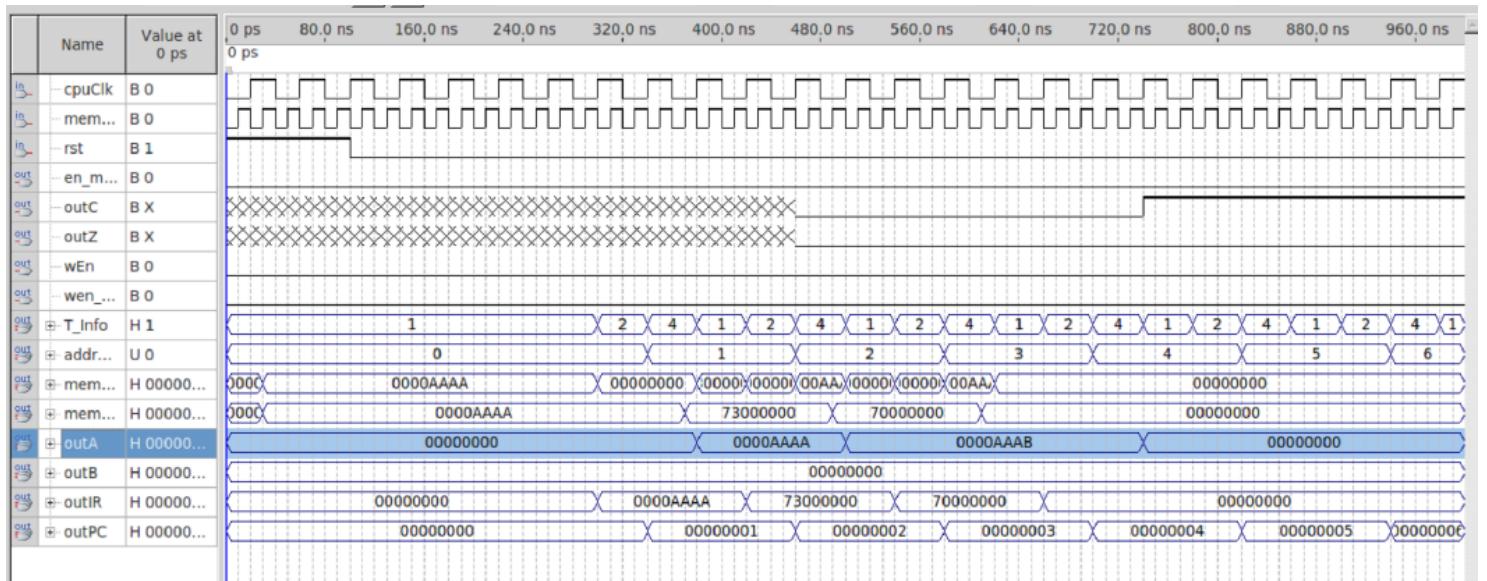
DECA

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16	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	
24	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	
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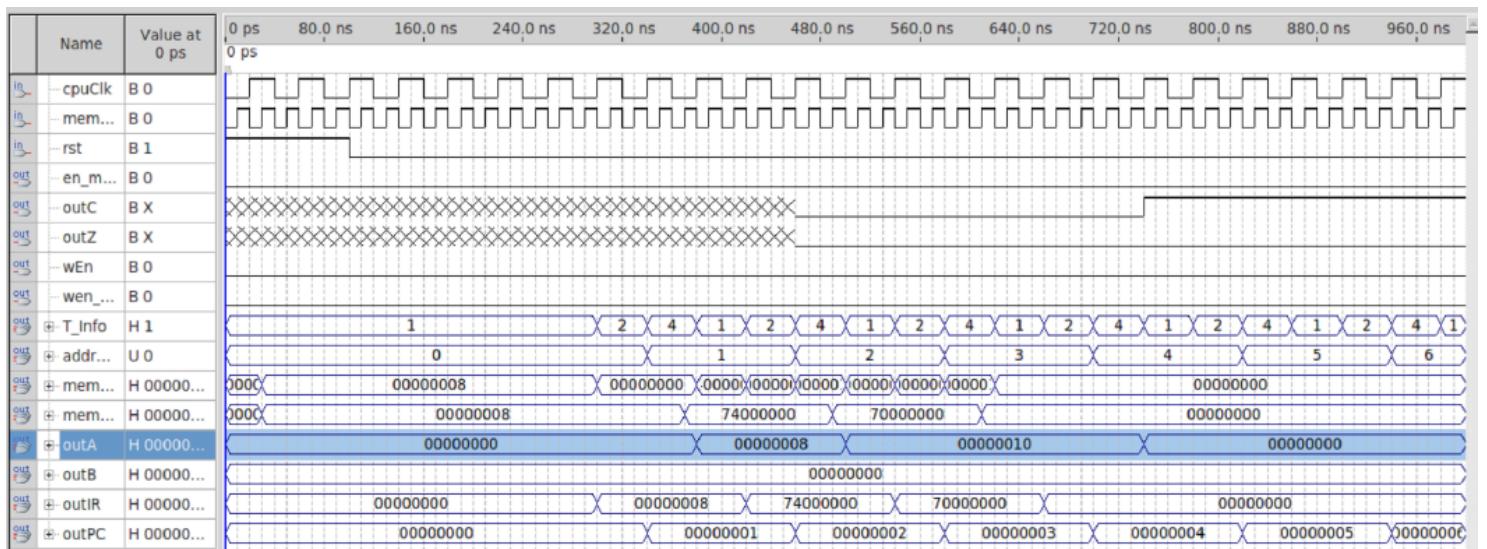
INCA

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16	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000
24	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000
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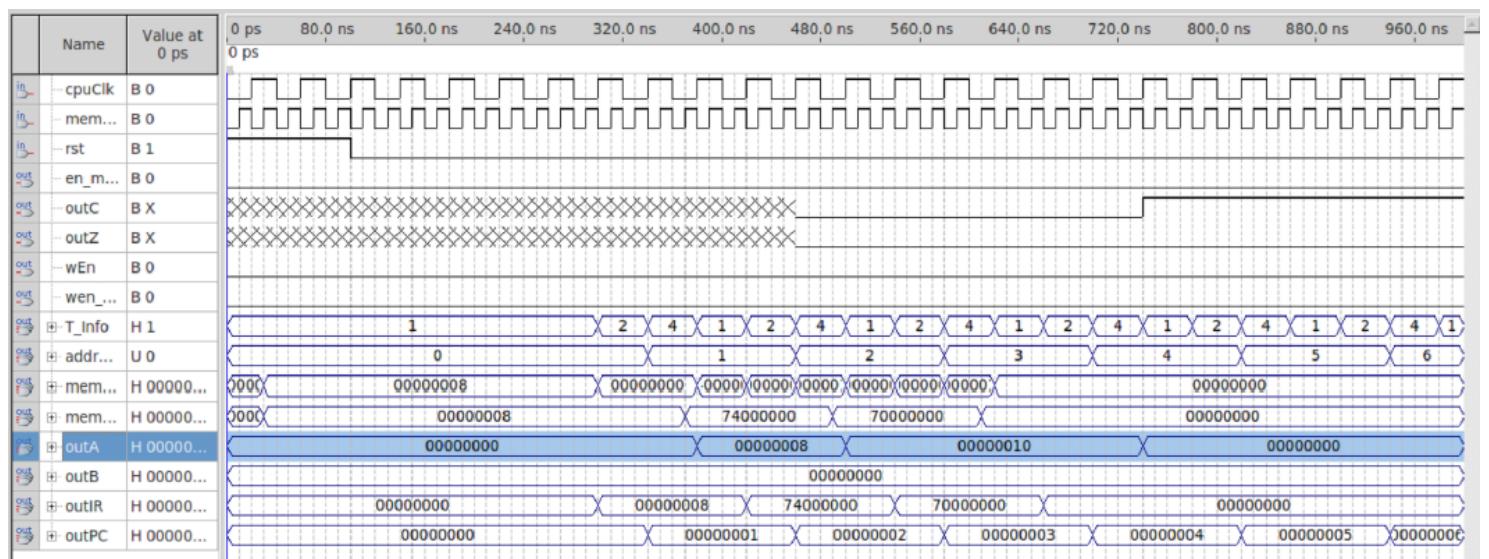
ROL

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ROR

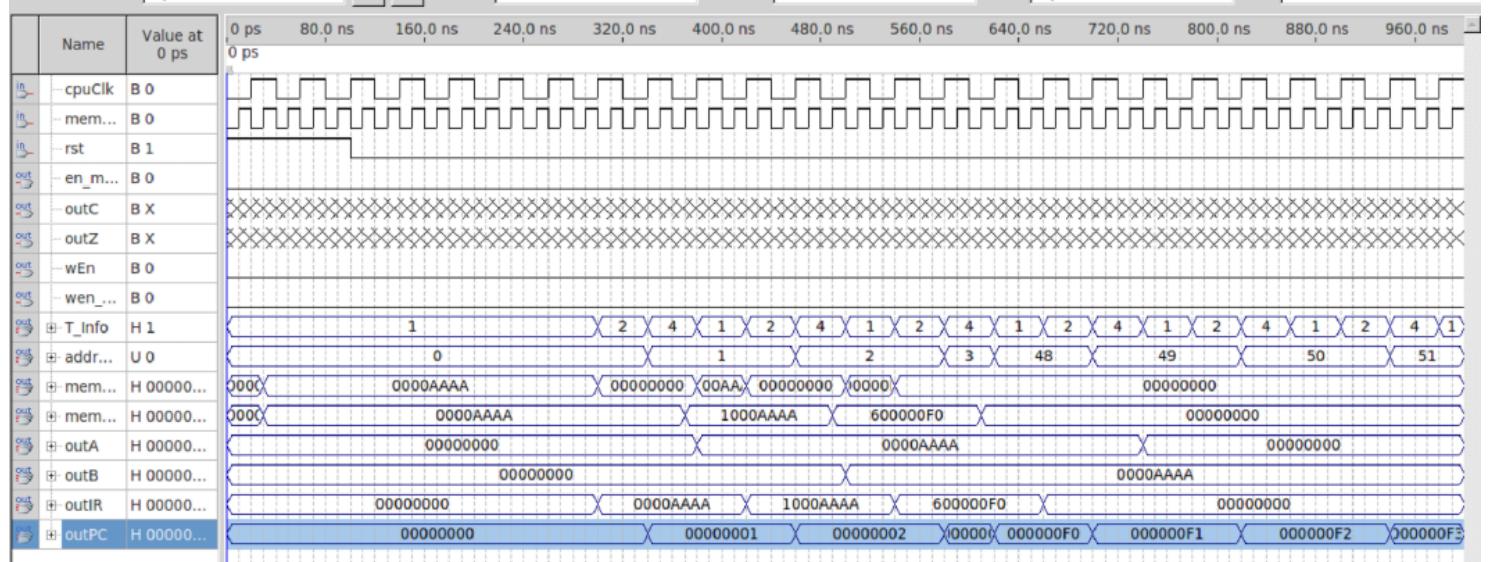
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BEQ

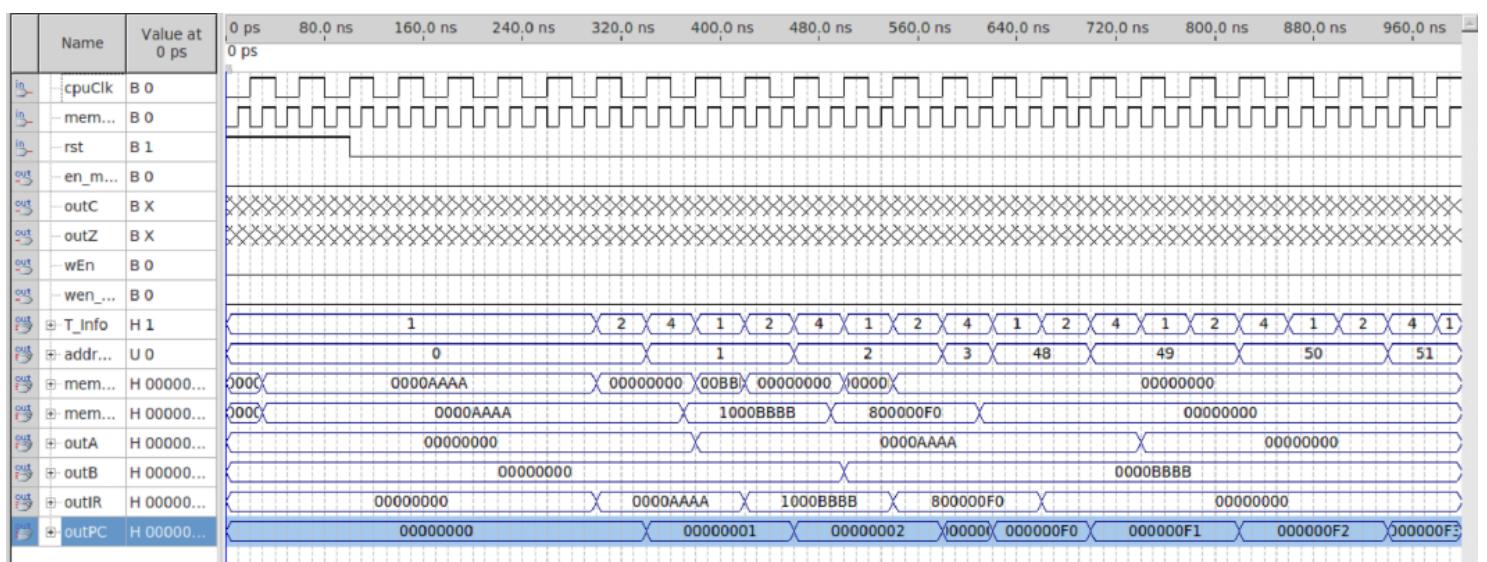
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40	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000
48	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000
56	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000

Master Time Bar: | 0 ps | ◀ ▶ Pointer: | 730.24 ns | Interval: | 730.24 ns | Start: | 0 ps | End: | 1.0 us |



BNE

Addr	+0	+1	+2	+3	+4	+5	+6	+7	ASCII	
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24	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	
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48	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	
56	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000	



Discussion:

In essence, the goal of this lab project was to merge various parts to form a functional CPU system. This entailed blending the data path and control components from prior labs alongside incorporating a reset circuit. The reset circuit played a vital role in ensuring the smooth operation of the CPU by clearing the program counter and stabilizing the surrounding data before commencing any operations.

Creating a functional CPU system provided a more profound insight into the intricate workings of a computer. Integrating different components necessitated meticulous planning and attention to detail while implementing the reset circuit demanded additional problem-solving skills. Overall, this project presented an opportunity to apply knowledge and skills in a practical context in designing and implementing a complete CPU system.