Quiz: Basic Processing Unit and Pipelining (CHAPTER 5)

Instructions: Select the most appropriate answer for each question.

What role does the Program Counter (PC) play in a processor's operation?

A) It stores the current executing instruction.

B) It keeps track of the address of the next instruction to be fetched.

C) It holds the results of the ALU operations.

D) It controls the input/output operations of the processor.

In pipelined architecture, what is the primary purpose of the instruction register (IR)?

A) To store data temporarily during computation.

B) To hold the instruction currently being executed.

C) To queue up multiple instructions for execution.

D) To send control signals to the ALU.

What is the benefit of having a multi-stage digital processing system, as discussed in Lecture 5?

A) It simplifies the processor's architecture.

B) It allows for multiple instructions to be executed at once.

C) It can decrease the clock cycle by using smaller, faster-operating subcircuits.

D) It increases the number of registers available in the system.

The 'fetch' phase of instruction processing involves which of the following actions?

A) The ALU performing arithmetic computations.

B) The program counter being updated to point to the next instruction.

C) Writing the results of computation back to the register file.

D) Storing data into the memory.

What is meant by the term 'pipelining' in computer architecture?

A) Increasing the power efficiency of the CPU by lowering its operating frequency.

B) Allowing each processor component to perform a different instruction simultaneously.

C) Reducing the physical size of the processor by integrating more components.

D) Connecting multiple processors to work on the same task.

Which stage in a basic pipelined processor would likely handle the decoding of an instruction and reading the registers?

A) Fetch

B) Decode

C) Execute

D) Write back

Answer Sheet:

B) It keeps track of the address of the next instruction to be fetched.

B) To hold the instruction currently being executed.

C) It can decrease the clock cycle by using smaller, faster-operating subcircuits.

B) The program counter being updated to point to the next instruction.

B) Allowing each processor component to perform a different instruction simultaneously.

B) Decode

Quiz: Pipelining Concepts in Computer Architecture (CHAPTER 6)

What is the fundamental concept of pipelining in computer processors?

A) Increasing the number of processors in a system.

B) Executing multiple instructions in one step.

C) Performing different stages of multiple instructions simultaneously.

D) Reducing the power consumption by minimizing the processing steps.

Which of the following best describes a 'data hazard' in pipelining?

A) A situation where the pipeline must be emptied before executing a new instruction.

B) A scenario where execution order must be changed due to data not being ready.

C) When two or more instructions interfere with each other due to shared data.

D) An error caused by insufficient data bandwidth in the pipeline.

What is the purpose of using interstage buffers in a pipelined processor?

A) To increase the instruction fetch rate.

B) To hold instruction-specific information as it flows through the pipeline stages.

C) To store final results of computation.

D) To enhance the speed of the ALU.

Why might a pipelined processor need to stall?

A) If the next instruction is a branch or jump.

B) When there is a data dependency between successive instructions.

C) Because the power supply to the processor is unstable.

D) To prevent overheating of the processor.

In pipelining, what is 'operand forwarding'?

A) Redirecting the output of one stage directly to a previous stage.

B) Using the result of a computation as an operand in a subsequent instruction without waiting for it to be written back to the register file.

C) Forwarding data from the main memory directly to the cache.

D) Sending instructions forward in the pipeline when there is a cache miss.

How does pipelining affect the instruction set architecture of a processor?

A) It requires a simpler, more limited set of instructions.

B) It demands complex instructions that combine multiple operations.

C) Pipelining necessitates considerations for instruction design that can support parallel execution of stages.

D) There is no impact on instruction set architecture from pipelining.

Answer Sheet:

C) Performing different stages of multiple instructions simultaneously.

C) When two or more instructions interfere with each other due to shared data.

B) To hold instruction-specific information as it flows through the pipeline stages.

B) When there is a data dependency between successive instructions.

B) Using the result of a computation as an operand in a subsequent instruction without waiting for it to be written back to the register file.

C) Pipelining necessitates considerations for instruction design that can support parallel execution of stages.

Quiz: Advanced Pipelining and Performance Optimization (CHAPTER 7)

What is the main purpose of branch prediction in a pipelined processor?

A) To reduce the power consumption during branch execution.

B) To minimize the performance loss caused by branch hazards.

C) To increase the number of pipeline stages.

D) To decrease the clock speed during branching.

What does it mean if a pipeline processor uses static branch prediction?

A) The processor dynamically decides the branch behavior based on past execution.

B) The prediction mechanism uses a simple, fixed strategy to guess branch behavior.

C) The branch decision changes in every execution based on runtime conditions.

D) It involves complex algorithms that require significant computational resources.

Why are pipeline stalls detrimental to processor performance?

A) They increase the processor's power consumption dramatically.

B) They signify that the processor is processing data at optimal speeds.

C) Stalls interrupt the steady flow of instruction execution, leading to wasted cycles.

D) They indicate that the processor is in a power-saving mode.

Which type of branch prediction is more adaptable to changing execution behaviors?

A) Static branch prediction.

B) Dynamic branch prediction.

C) Linear branch prediction.

D) Indirect branch prediction.

What role does a Branch Target Buffer (BTB) play in a pipelined processor?

A) It stores the outcomes of recent branch instructions to optimize decision-making.

B) It acts as a temporary storage for data needed by branch instructions.

C) It buffers data directly from the memory to speed up execution.

D) It stores the physical addresses of the next instruction to execute.

How does out-of-order execution benefit a pipelined processor's performance?

A) By allowing instructions to execute as soon as their operands are ready, regardless of their original order.

B) By strictly maintaining the sequence of instruction execution to prevent data hazards.

C) By reducing the number of instructions that can be executed in parallel.

D) By simplifying the control logic required to manage instruction dependencies.

Answer Sheet:

B) To minimize the performance loss caused by branch hazards.

B) The prediction mechanism uses a simple, fixed strategy to guess branch behavior.

C) Stalls interrupt the steady flow of instruction execution, leading to wasted cycles.

B) Dynamic branch prediction.

A) It stores the outcomes of recent branch instructions to optimize decision-making.

A) By allowing instructions to execute as soon as their operands are ready, regardless of their original order.

Quiz: Advanced Pipelining Techniques in Computer Architecture (CHAPTER 8)

What is the main challenge addressed by the introduction of superscalar architectures?

A) Decreasing the physical size of the processor.

B) Reducing the energy consumption of the CPU.

C) Increasing the number of instructions processed simultaneously.

D) Simplifying the processor design.

What is the purpose of reservation stations in a superscalar processor?

A) To store the results of arithmetic operations.

B) To temporarily hold instructions until their operands are ready for execution.

C) To keep track of the program counter for multiple threads.

D) To reduce the complexity of the instruction set.

How does out-of-order execution impact the performance of a pipelined processor?

A) It increases the chance of pipeline stalls due to data hazards.

B) It allows more efficient use of CPU resources by executing available instructions.

C) It simplifies the processor's control logic.

D) It decreases the throughput by increasing the complexity of dependency checks.

What is the role of a reorder buffer in superscalar processors?

A) To reorder the instructions to their original sequence for correct program execution.

B) To enhance the speed of the arithmetic logic unit (ALU).

C) To bypass the cache memory for faster data access.

D) To store intermediate values of computations.

In the context of pipelining, what is a 'branch target buffer' used for?

A) Storing the outcomes of branch instructions to facilitate quicker branch decisions.

B) Temporarily disabling branches that are predicted not to be taken.

C) Redirecting branch instructions to alternative pipeline paths.

D) Holding data required for executing branch instructions.

What benefit does dynamic branch prediction offer over static branch prediction?

A) It always assumes branches will not be taken, which simplifies the prediction logic.

B) It utilizes historical information to make more accurate branch predictions.

C) It reduces the overall cost of the processor.

D) It eliminates the need for branch predictions in the pipeline.

Answer Sheet:

C) Increasing the number of instructions processed simultaneously.

B) To temporarily hold instructions until their operands are ready for execution.

B) It allows more efficient use of CPU resources by executing available instructions.

A) To reorder the instructions to their original sequence for correct program execution.

A) Storing the outcomes of branch instructions to facilitate quicker branch decisions.

B) It utilizes historical information to make more accurate branch predictions.