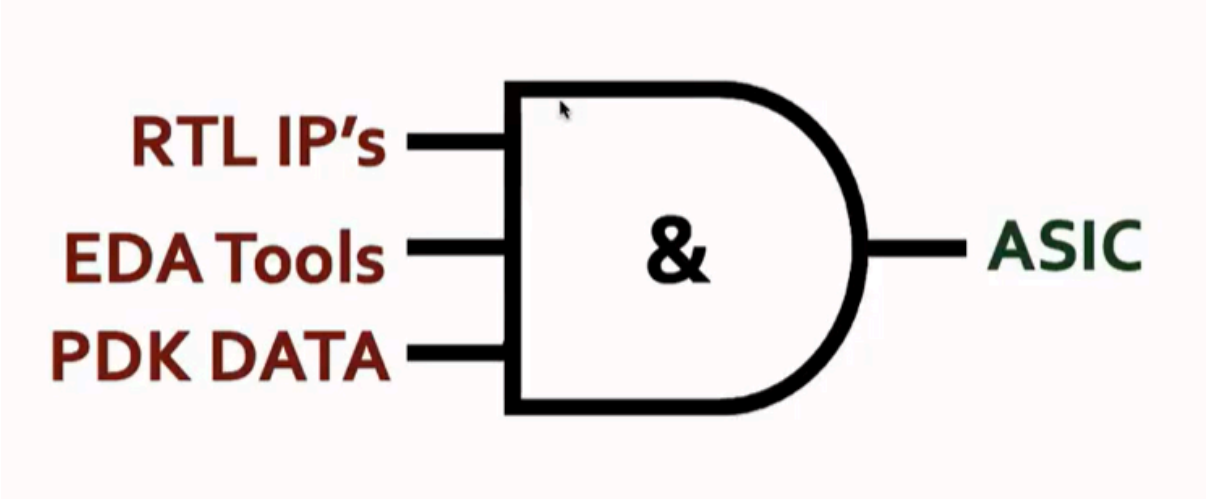
SKY130_D1_SK2 - SoC design and OpenLANE

SKY_L1 - Introduction to all components of open-source digital asic design

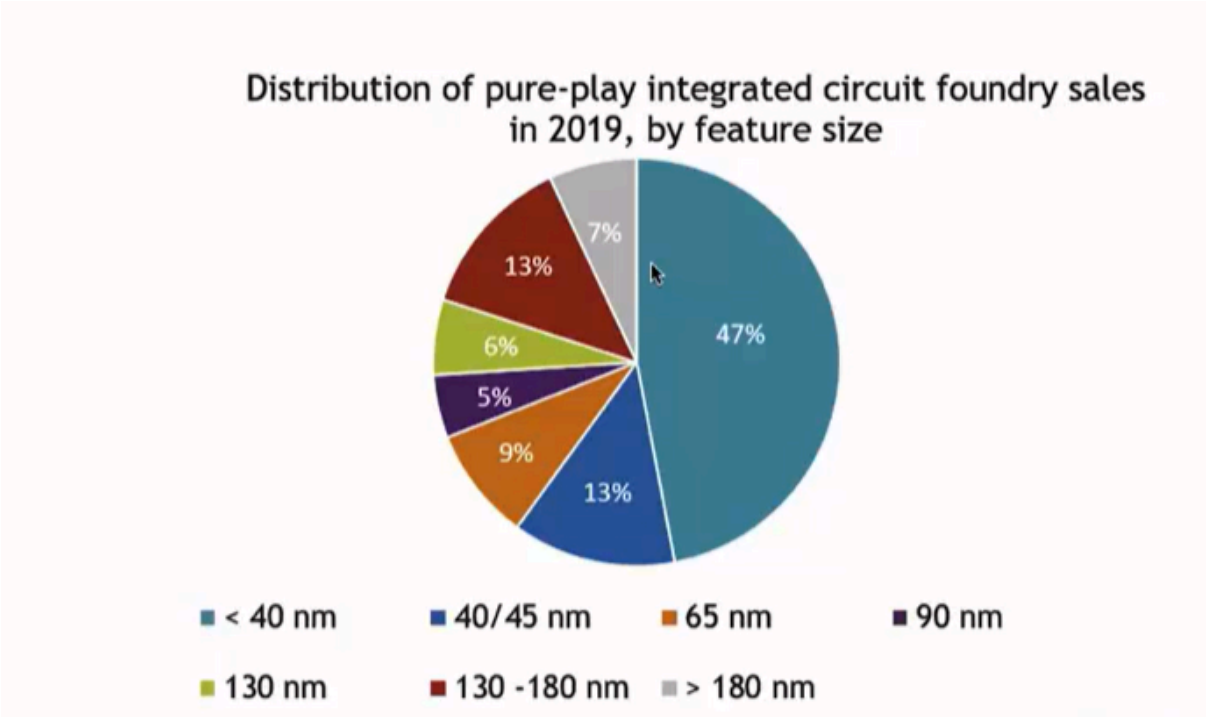
Designing Digital Application Specific Integrated circuits(AISC)



[REQUIREMENTS FOR ASIC]

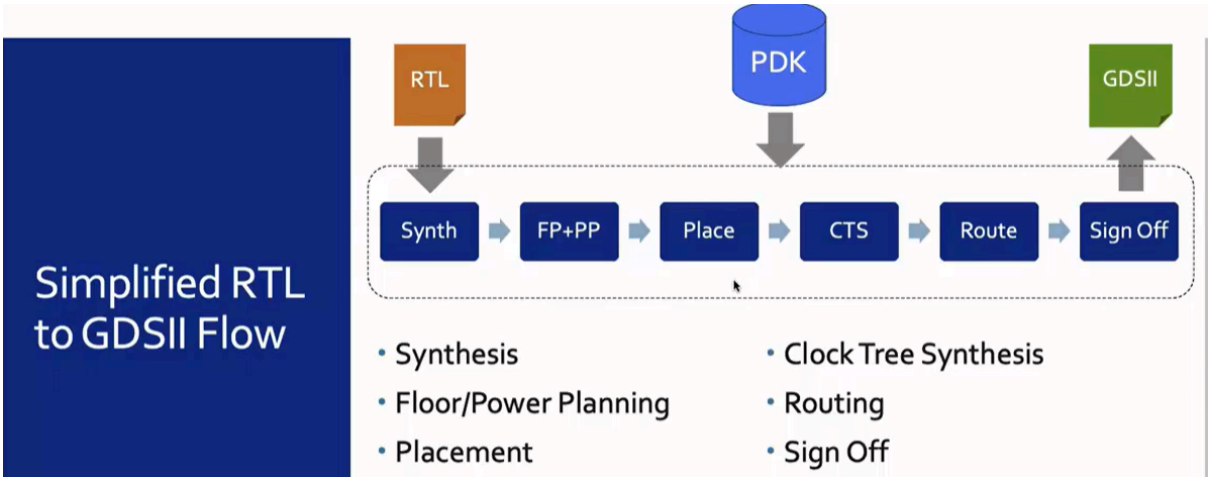
PDK: Process Design Kit. These are the collection of files used to model for the fabrication process for the EDA tools used in IC design. It contains :

- Process Design rules- LVS, DRC, PEX
- Device Models
- Digital Standard cell Libraries



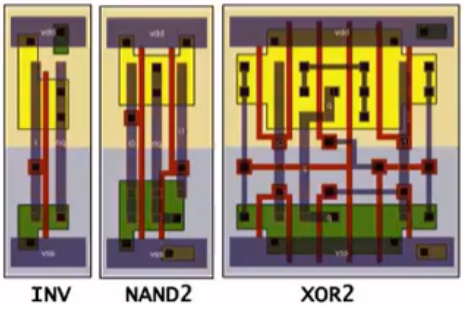
- ASIC Flow Objective: RTL to GDSII
  - Also, called Automated PnR and/or Physical Implementation

SKY_L2 - Simplified RTL2GDS flow



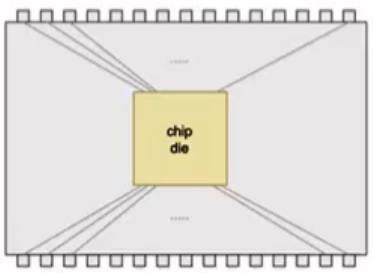
The first major step in the ASIC flow is the **synthesis** where RTL is converted into circuit components from standard cell library(SCL). Standard calls have a regular layout.

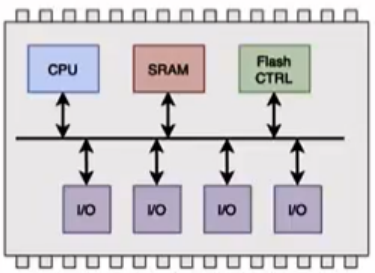
- Each has different views/models
  - Electrical, HDL, SPICE,
  - Layout (Abstract and Detailed)
  - ...

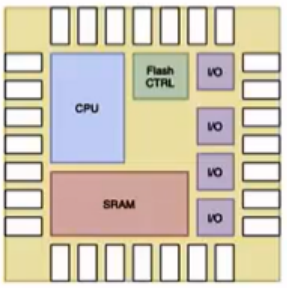


FLOOR AND POWER PLANNING

i)CHIP-FLOORPLANNING- chip die is partitioned between different components.

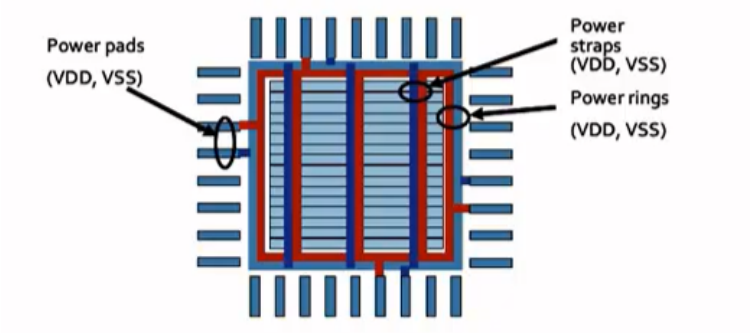






ii)MACRO PLANNING- define macro dimensions and pic locations. In this step, the rows are not undefined

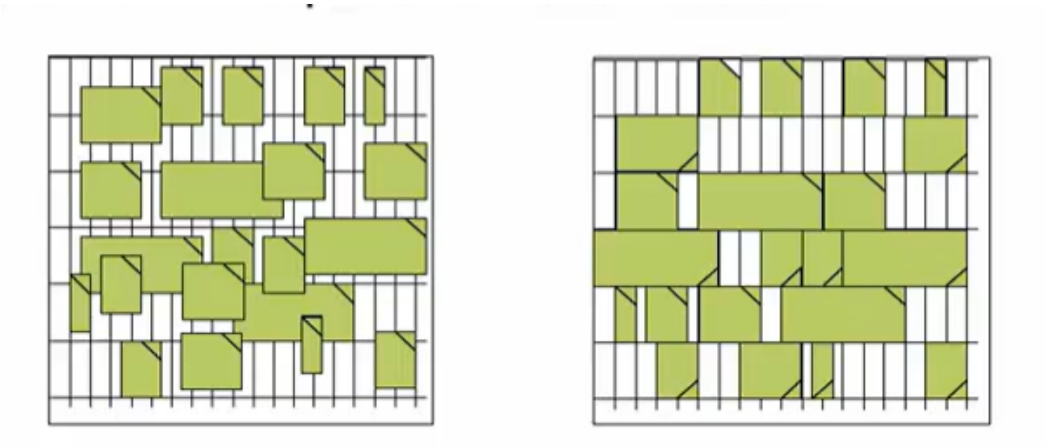
iii) POWER PLANNING- the power network is constructed. The chip is powered by multiple VDD and GND pins. Parallel strips are used to reduce resistance and to address electro migration problems. Electromigration occurs when the current density in the wires exceeds the specified limits for a given process. It uses upper metal layers which are thicker.



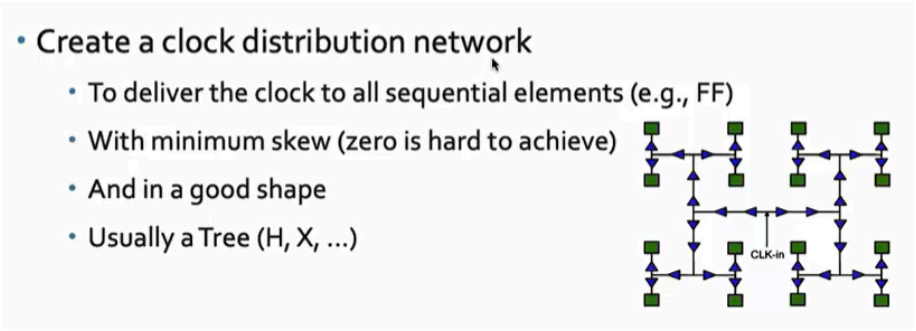
POWER PLANNING

PLACEMENT

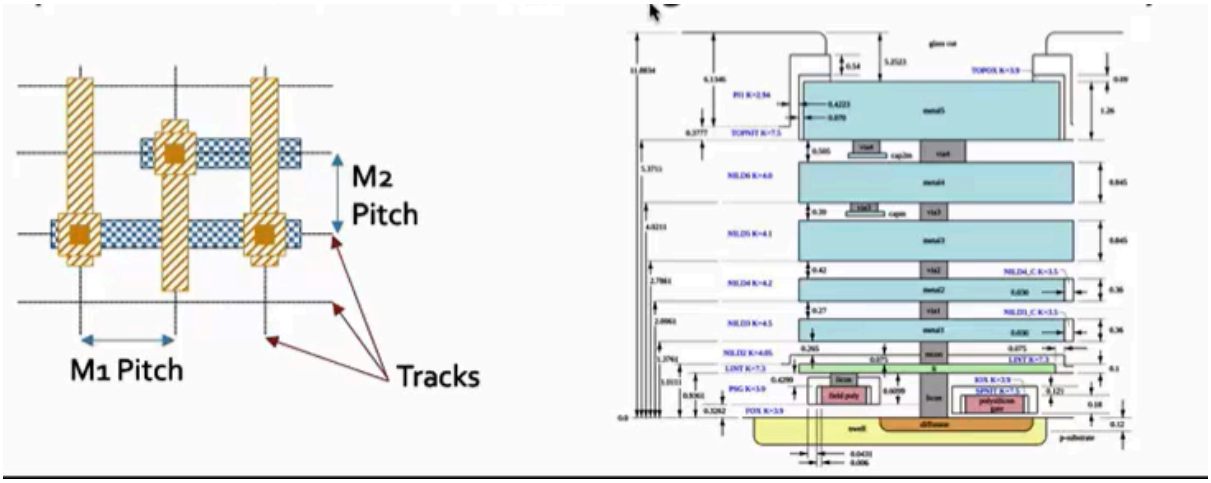
Typically done in 2 steps: Global and Detailed



CTS



ROUTING: Implement the interconnect using available metal layers. For each metal layer, the pdk defines the thickness, the pitch and defines the tracks the minimum width. The SKYWATER PDK defines 6 routing layers



SKY_L3 - Introduction to OpenLANE and Strive chipsets