Tribhuvan University

Faculty of Humanities & Social Sciences

OFFICE OF THE DEAN

2021

Bachelor in Computer Applications
Course Title: Microprocessor and Computer Architecture
Code No: CACS 155
Semester: II

Full Marks: 60
Pass Marks: 24
Time: 3 hours
Batch: 2021

Candidates are required to answer the questions in their own words as far as possible.

Group B

Attempt any SIX questions. **[6×5 = 30]**

2. Define addressing mode? Suppose content of register A and B is 37H and 57H respectively. Find the content of flag register after ADD B is performed. [2+3]
3. What is the requirement of common bus System? Explain with figure
4. Explain Symbolic Microinstruction and microinstruction format.
5. What is stack? Give the organization of register stack with all necessary elements.
6. What is pipeline conflict? Explain data dependency and handling of branch instruction in detail.
7. Explain the basic working principle of the Control Unit with timing diagram.
8. Explain the following instructions
   a) LHLD 5050H
   b) CPI 34H
   c) JNZ 6080H

Group C

Attempt any TWO questions. **[2×10 = 20]**

9. Draw the timing diagram for MOV B. For ten bytes of data starting from 7050H, write a program to sort the reading in ascending order [4+6]
10. Explain the steps of Address Sequencing in detail. Draw and explain selection of address for control memory. [5+5]
11. Discuss four-segment instruction pipeline with suitable diagram.