Tribhuvan University

Faculty of Humanities & Social Sciences

OFFICE OF THE DEAN

2021

Bachelor in Computer Applications
Course Title: Microprocessor and Computer Architecture
Code No: CACS 155
Semester: II
Centre:

Full Marks: 60
Pass Marks: 24
Time: 3 hours
Batch: 2021

Symbol No:

Reg. No.:

Candidates are required to answer the questions in their own words as far as possible.

Group A

Attempt all the questions. [10×1 = 10]

1. Circle (O) the correct answer.

i) How is -01H stored in "A" register?

a) -0000 0001 b) 1111 1111 c) 1000 0001 d) 1111 1110

ii) How many iterations will this loop have.....

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MVI C, 00H
Back: .....
DCR C
JNZ Back
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a) 255 iterations b) 256 iterations c) 257 iterations d) 1 iteration

iii) MVI A, 25H
CPI 25 H
Show effect on CF and ZF

a) CF=1, ZF=0 b) CF=0, ZF=0 c) CF=0, ZF=1 d) CF=X, ZF=0

iv) In a program using subroutine call instruction, it is necessary

a) initialize program counter b) Clear the accumulator

c) Reset the microprocessor d) Clear the instruction register

v) ___ architecture is also known as systolic arrays for pipelined execution of specific algorithms.

a) MISD (Multiple Instruction streams over Single Data stream)

b) SISD (Single Instruction stream over Single Data stream)

c) SIMD (Single Instruction stream over Multiple Data streams)

d) MIMD (Multiple Instruction streams over Multiple Data streams)

vi) Microinstructions are stored in control memory groups, with each group specifying.

a) Routine b) Subroutine c) Vector d) Address

vii) The micro operation that specifies binary operations for strings of bits stored in registers are_____.

a) logic micro operation. b) shift micro operation.

c) arithmetic micro operation. d) register transfer micro operation.

viii) A special register that holds the address of location to or from which data are to be transferred is known as

a) Memory data register b) Memory address register

c) Index register d) Program counter

ix) Which one of the following is not pipelining hazard?

a) Resource Conflict b) Data Dependency

c) Branch Conflict d) Interrupt Hazard

x) In RISC architecture, memory access is limited to instructions:

a) MOV and JMP b) STA and LDA

c) PUSH and POP d) CALL and RET