Tribhuvan University

Faculty of Humanities & Social Sciences

OFFICE OF THE DEAN

2019

Bachelor in Computer Applications
Course Title: Microprocessor and Computer Architecture
Code No: CACS 155
Semester: II

Full Marks: 60
Pass Marks: 24
Time: 3 hours

Candidates are required to answer the questions in their own words as far as possible.

Group B

Attempt any SIX questions. **[6×5 = 30]**

2. Define CPU. Differentiate between Microprocessor and Microcontroller with example. [1 + 4]
3. Define instruction cycle. Explain the opcode fetch machine cycle for MOV A, B with timing diagram. (Opcode: MOV A, B = 78h) [1 + 4]
4. Write an ALP using 8085 to check number stored in memory location 8080h is either even or odd. [5]
5. What is cache memory? Explain the elements of cache design. [1 + 4]
6. Explain the organization of Microprogrammed Control Unit. [5]
7. What is pipeline? Explain the four segment instruction pipeline. [1 + 4]
8. Write short notes on (any two): [2 x 2.5 = 5]
   a) Accumulator b) 8085 Interrupts c) Structure of Hard Disk

Group C

Attempt any TWO questions. **[2×10 = 20]**

9. Define instruction set. Classify the instructions available in 8085 with example. [2 + 9]
10. Define the addressing mode. Explain the various instruction addressing modes with example. [2 + 8]
11. Define micro-program? Describe symbolic micro-program for instruction FETCH routine. Explain the organization of micro-program sequencer for control memory with suitable diagram. [1 + 4 + 5]