Progetto TTL

IEEE Student Branch 1019, University of Brescia

Rev.	Date	Revision Description
0	10/11	Creazione progetto, Prima progettazione del generatore di clock e clk multiplexer
1	24/11	Aggiunta contatore per divisore frequenza. modifica input pushbutton in CLK_GEN. Creazione circuito HLT, Aggiunta bit a CLK_SELECT. Aggiunta registri

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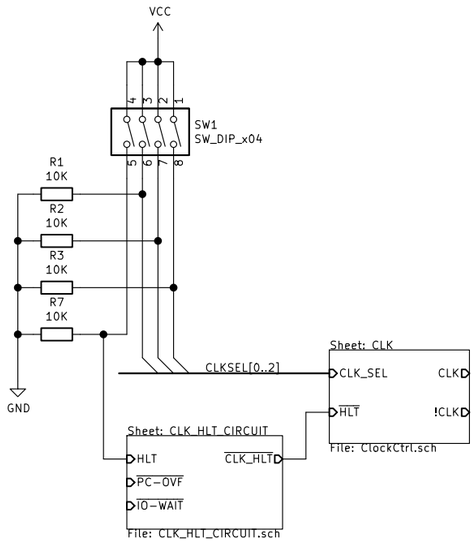

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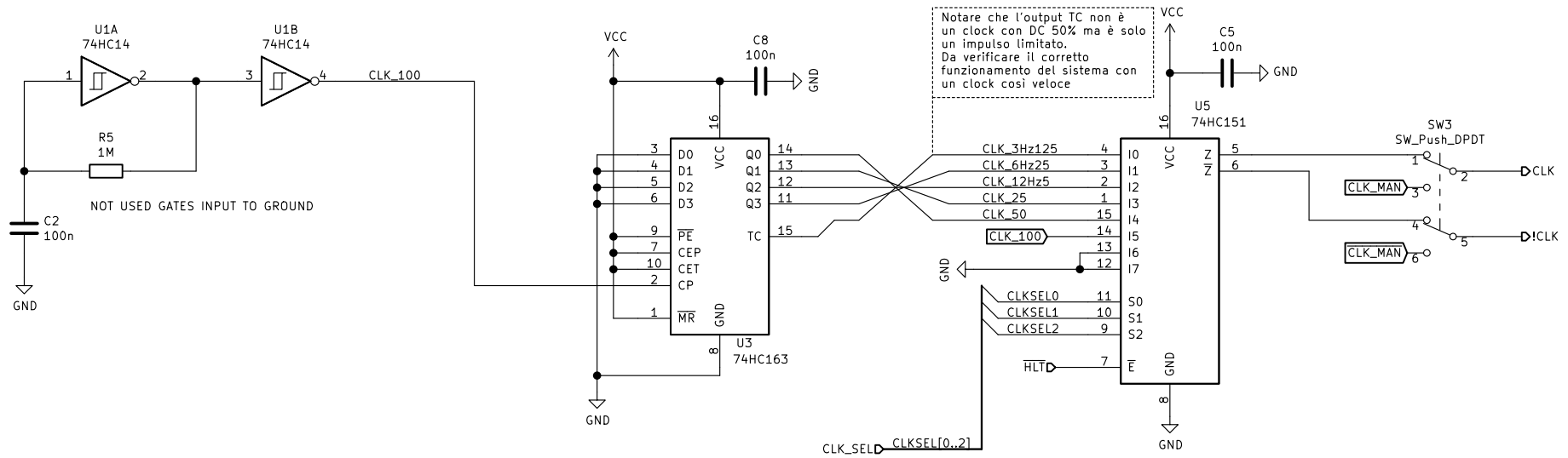

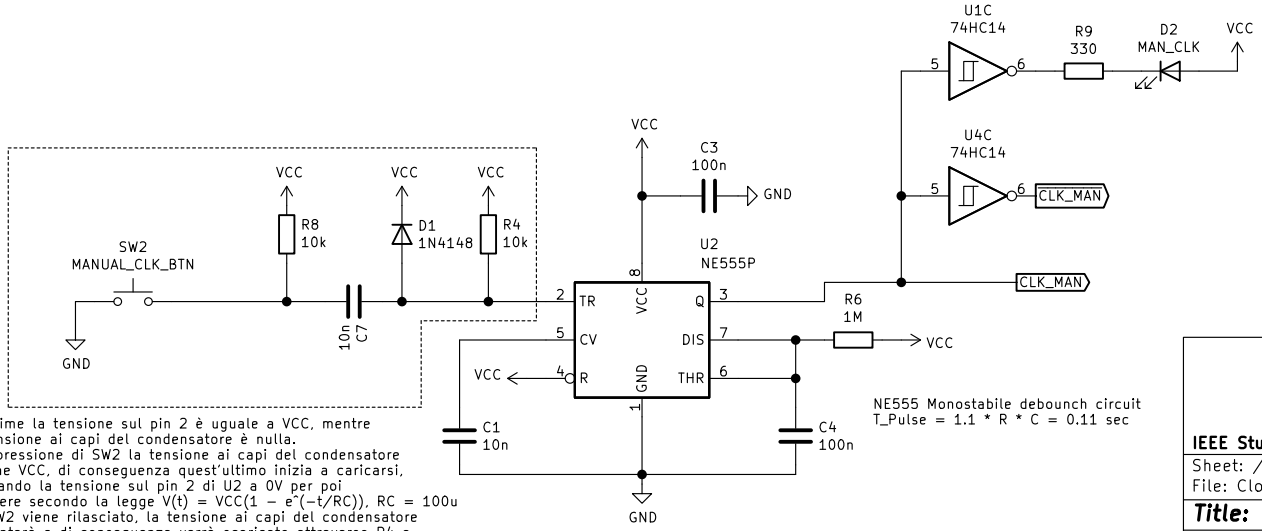

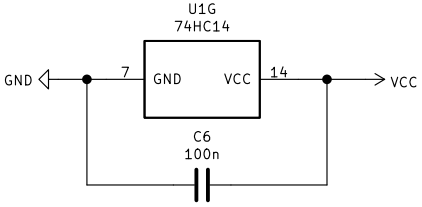

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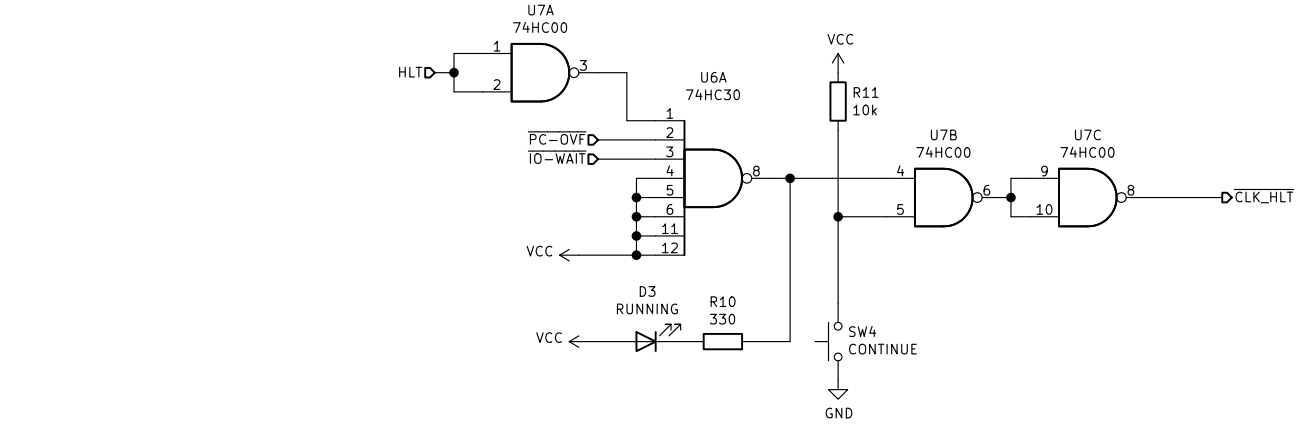

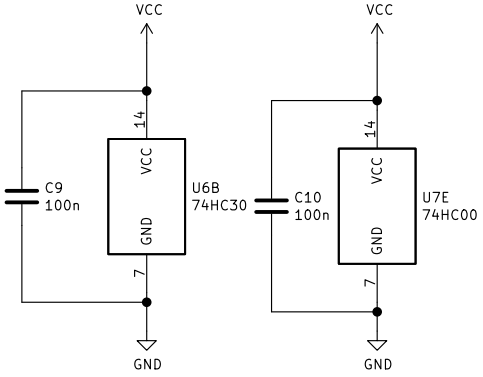

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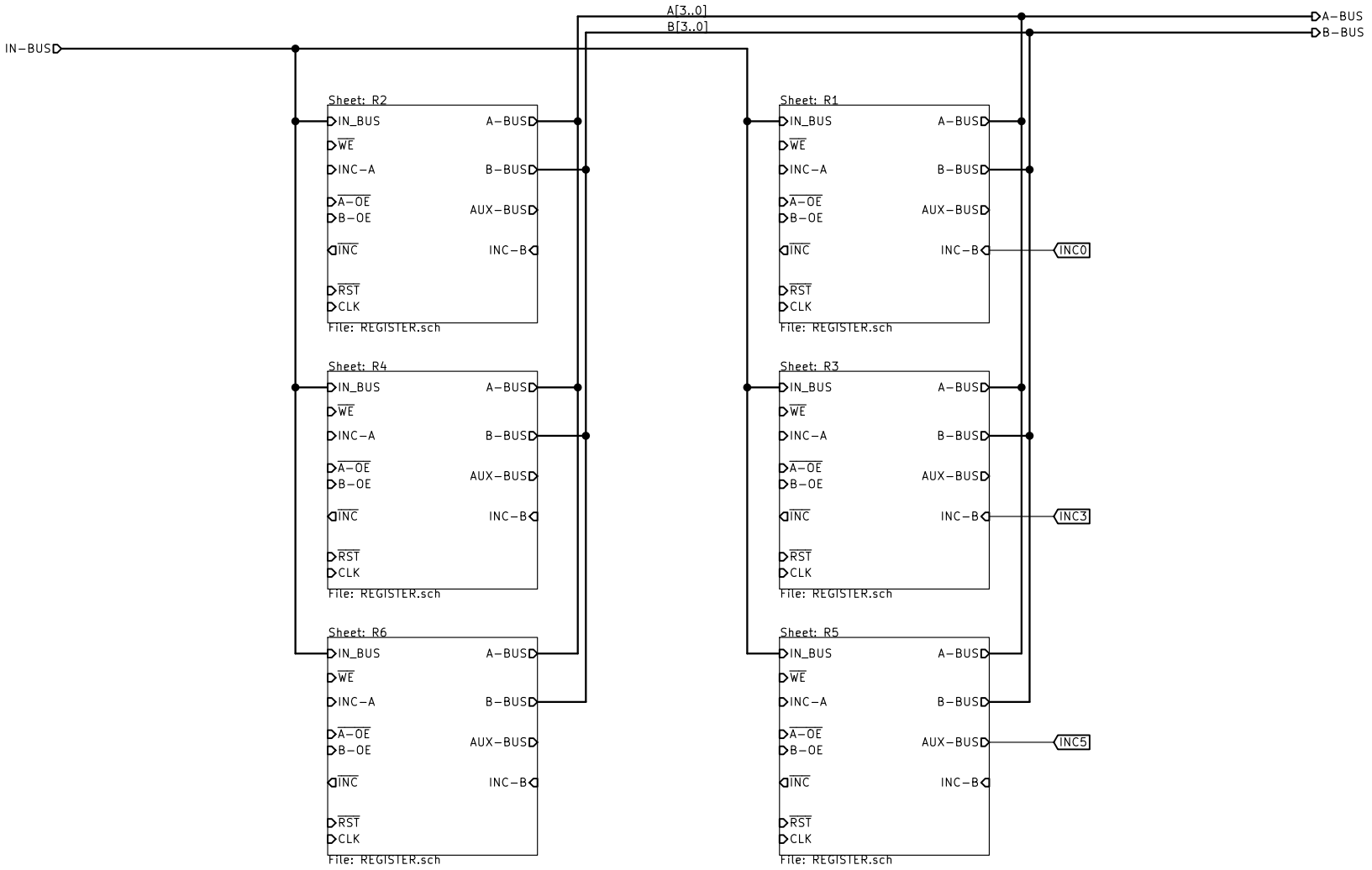

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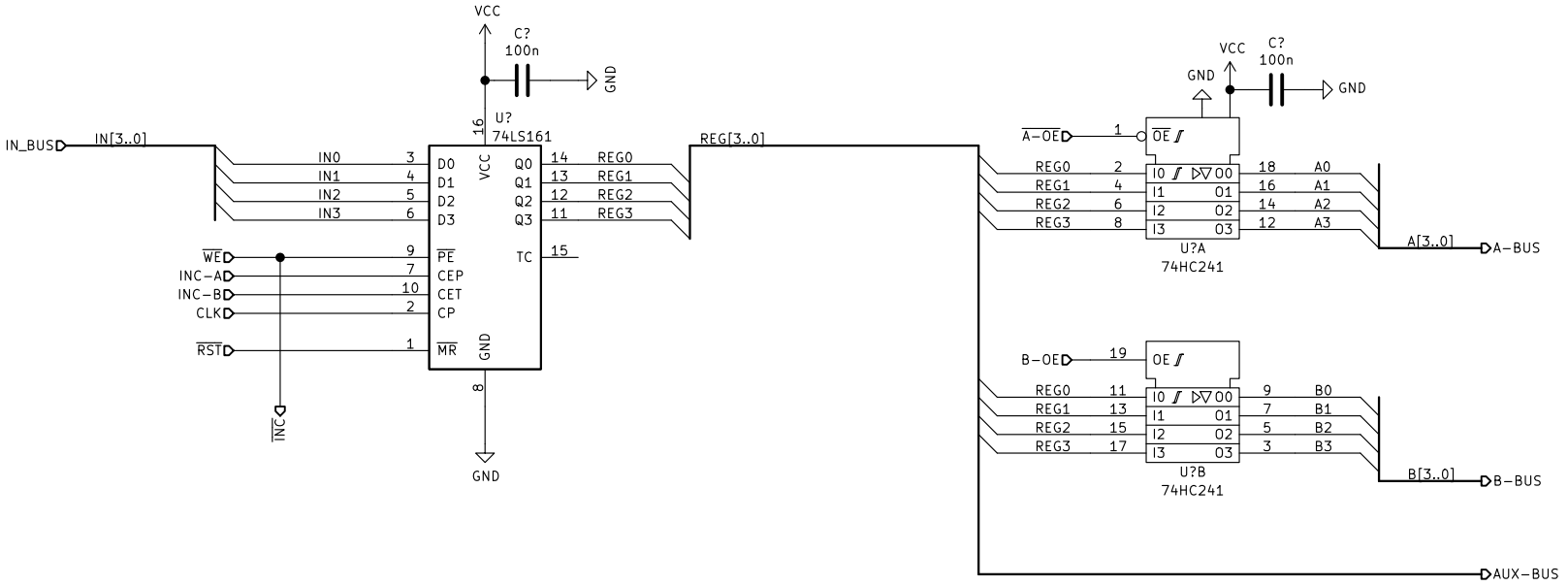

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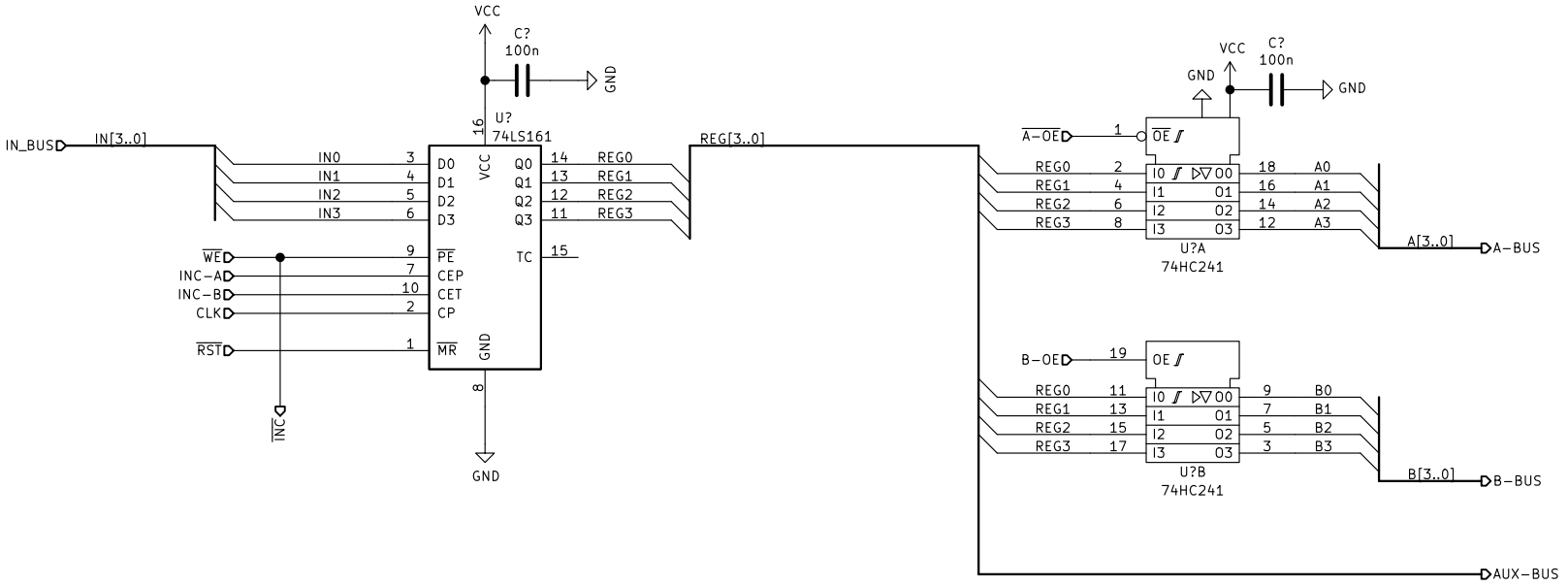

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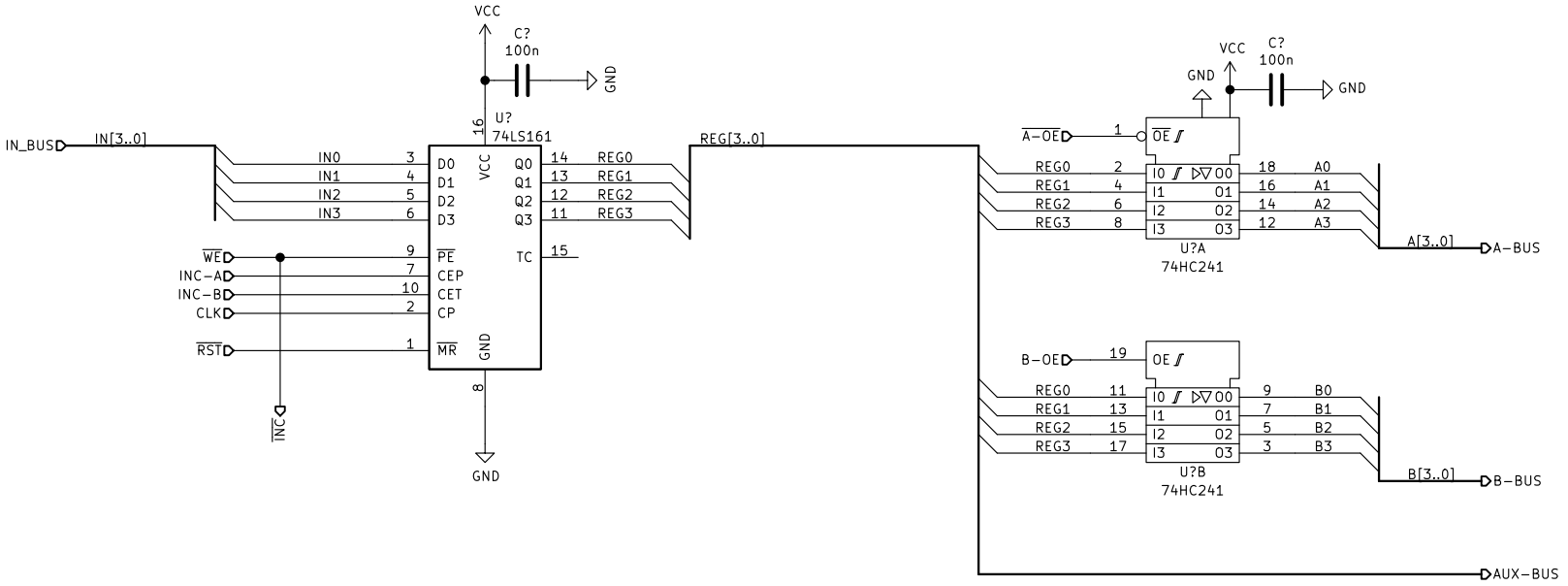

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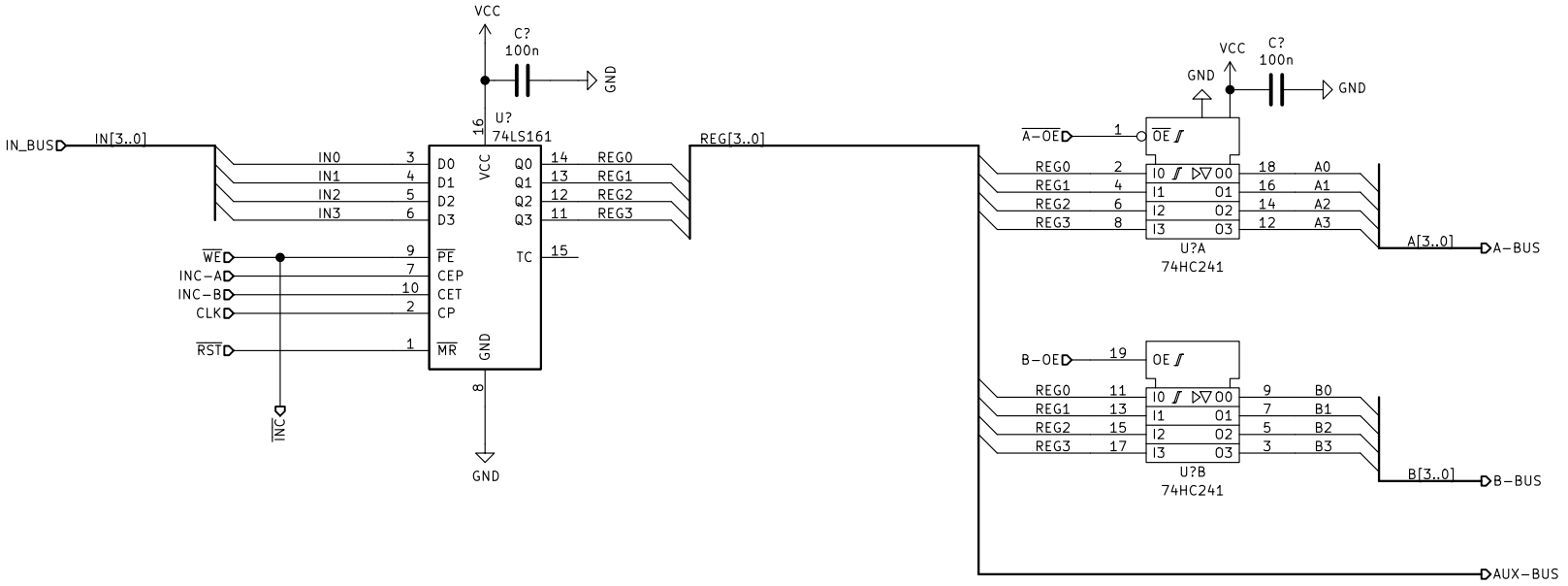

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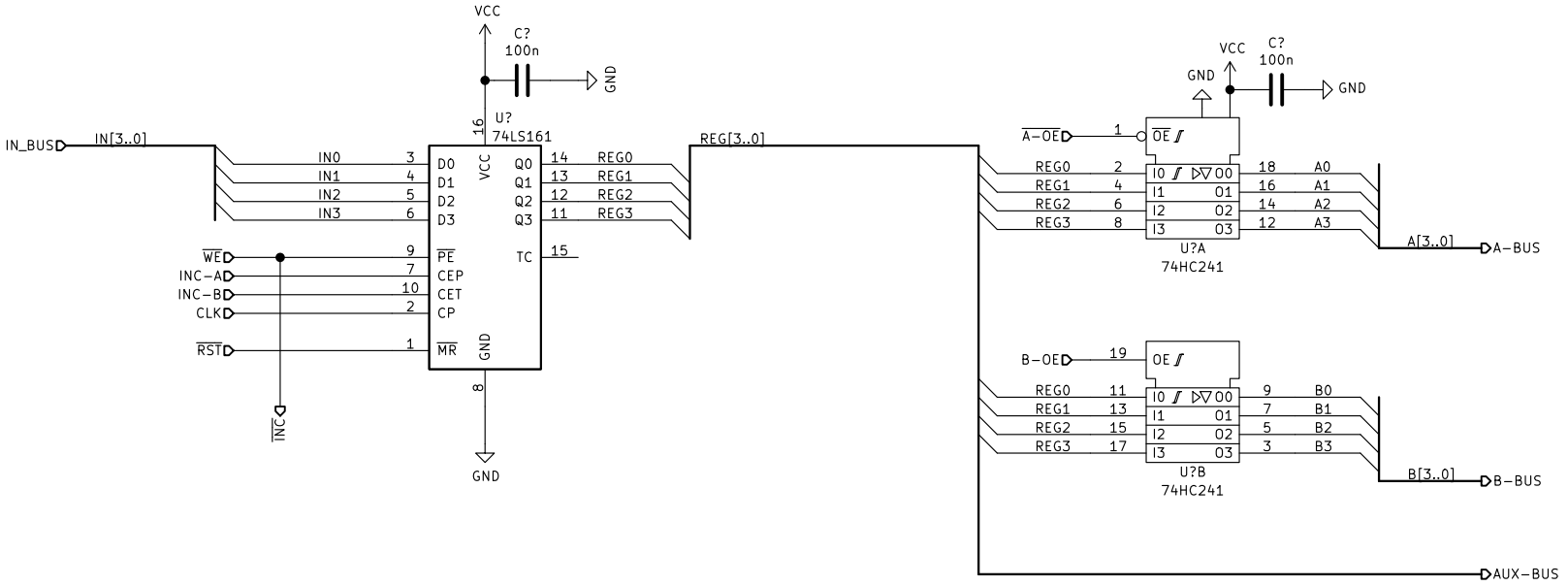

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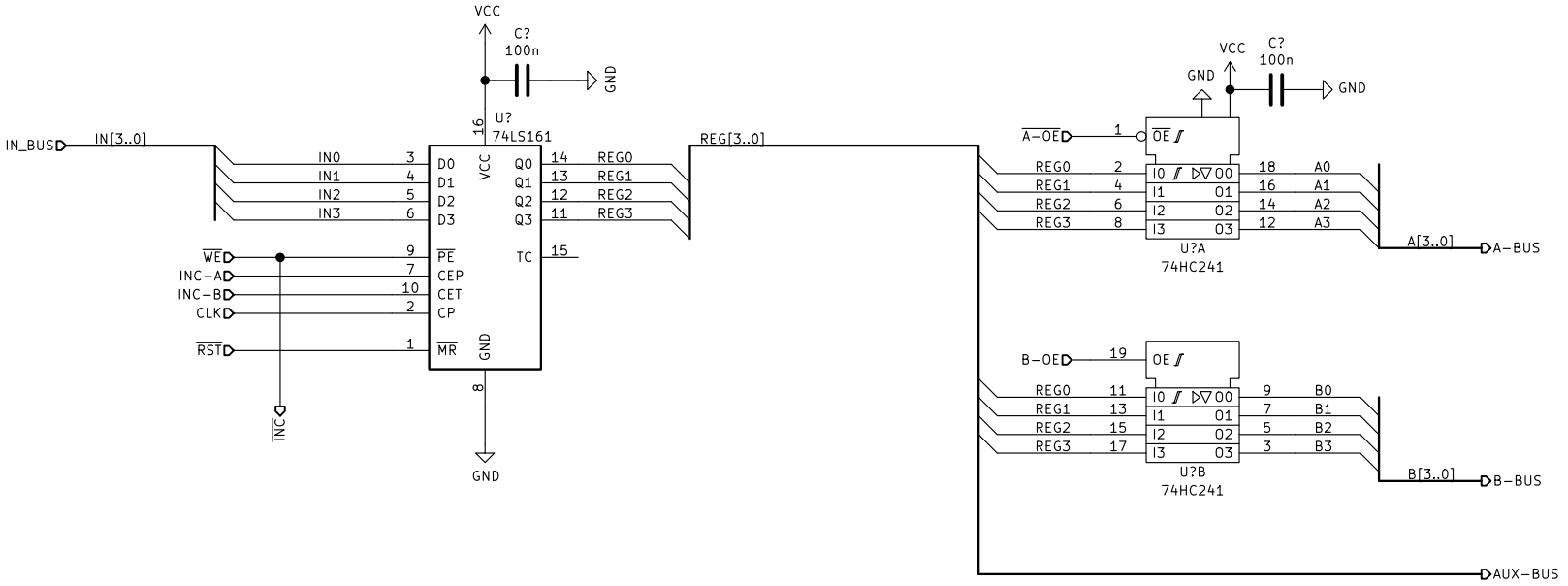

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