# Progetto TTL

## IEEE Student Branch 1019, University of Brescia

| Rev. | Date | Revision Description |
|---|---|---|
| 0 | 10/11 | Creazione progetto, Prima progettazione del generatore di clock e clk multiplexer |
| 1 | 24/11 | Aggiunta contatore per divisore frequenza. modifica input pushbutton in CLK_GEN. Creazione circuito HLT, Aggiunta bit a CLK_SELECT. Aggiunta registri |
| 2 | 29/11 | Fix convenzione dei nomi, register selection and I/O logic |
| 3 | 15/12 | Alu e interconnessione con i registri. Logo nel cartiglio e fix minori |

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Sheet: /
File: TeToLogic.sch

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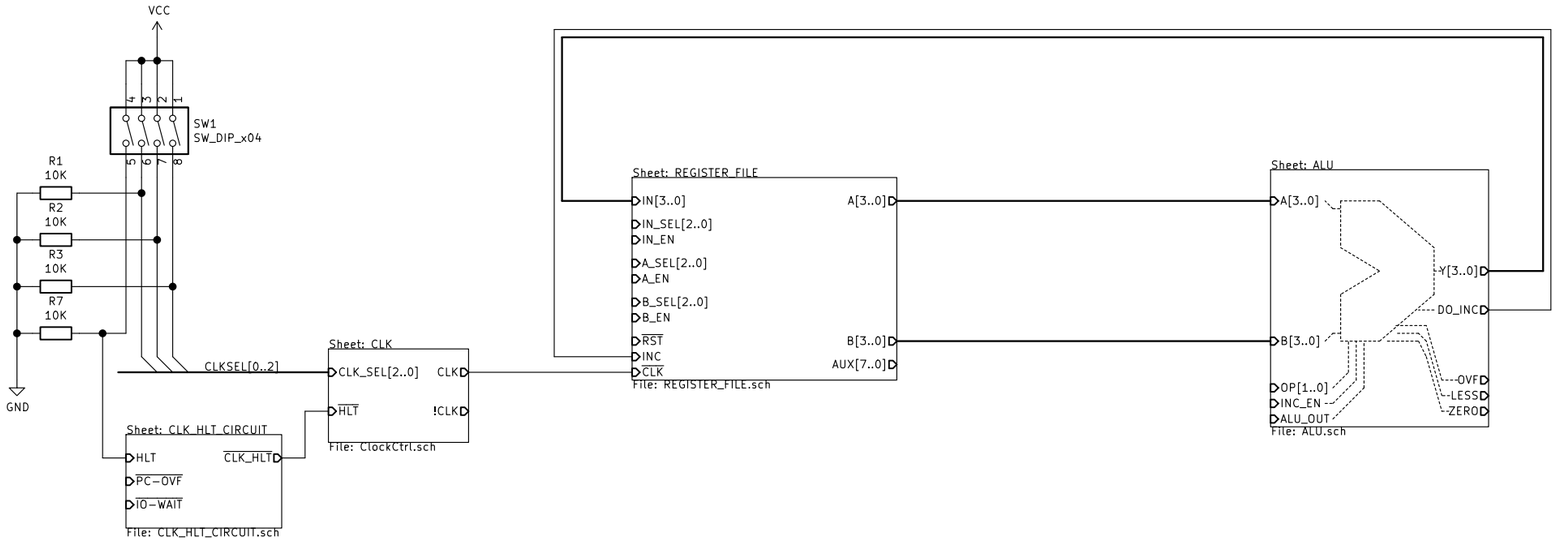
| Size: A3 | Date: 2021-11-10 | **Rev:** |
| KiCad E.D.A. eeschema 5.1.10 | | Id: 1/13 |




# General Structure

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Sheet: /Hierarchy/
File: BlockDiagram.sch

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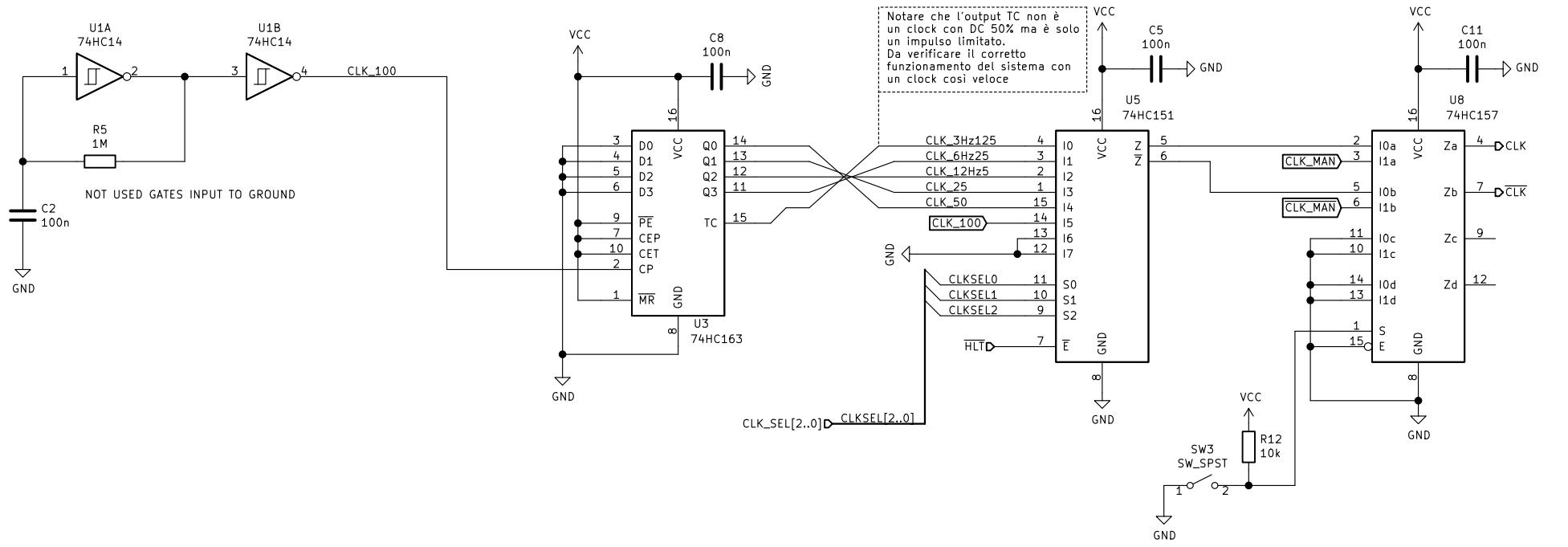


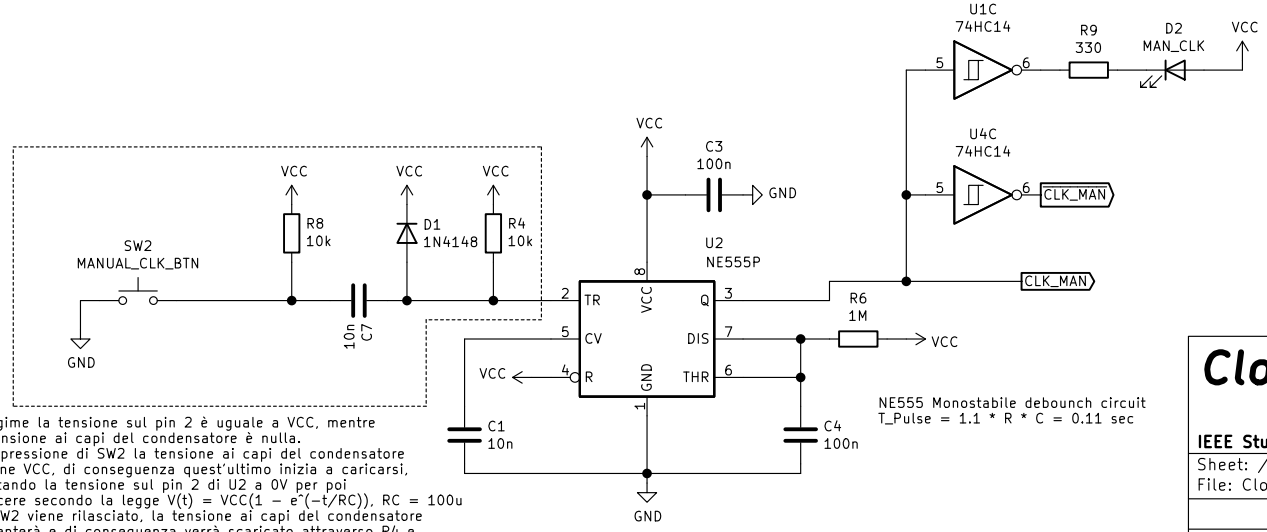


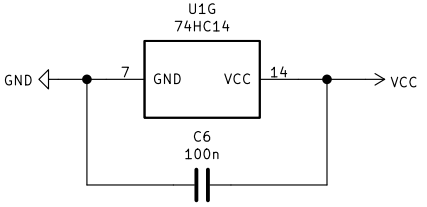


# Clock Generator

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Sheet: /Hierarchy/CLK/
File: ClockCtrl.sch

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| Size: A4 | Date: 2021-11-10 | **Rev: 2** |
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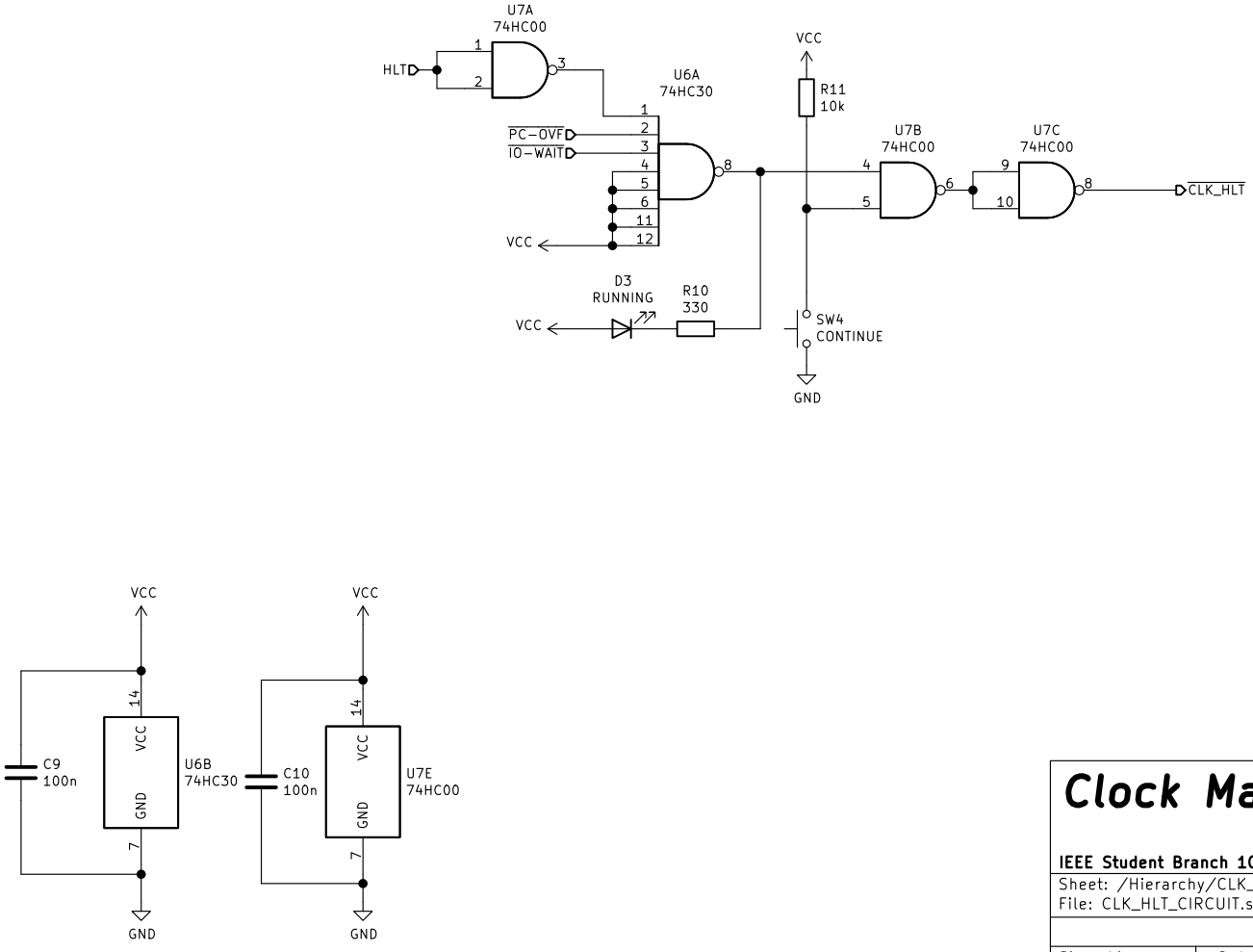


# Clock Management

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Sheet: /Hierarchy/CLK_HLT_CIRCUIT/
File: CLK_HLT_CIRCUIT.sch

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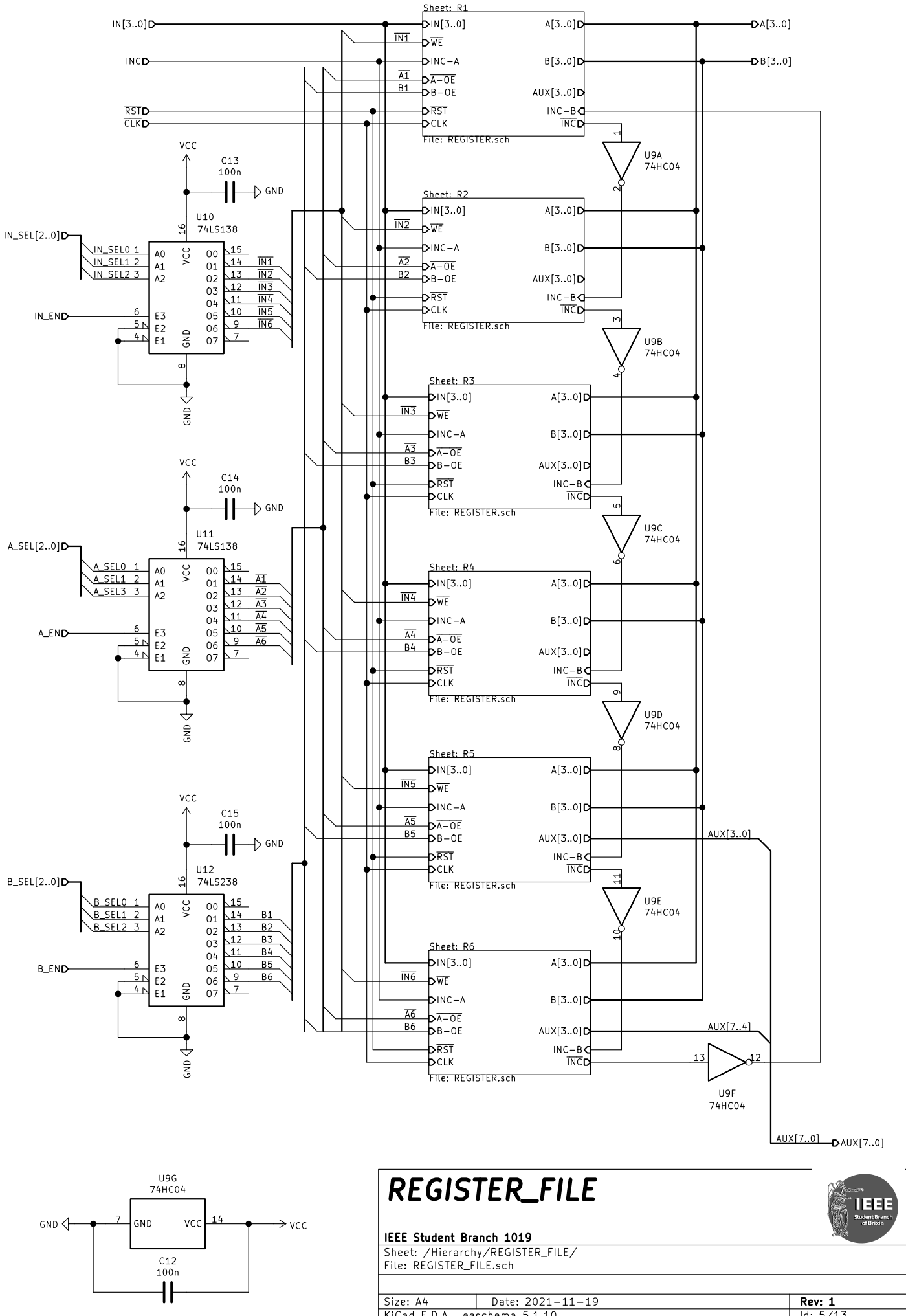
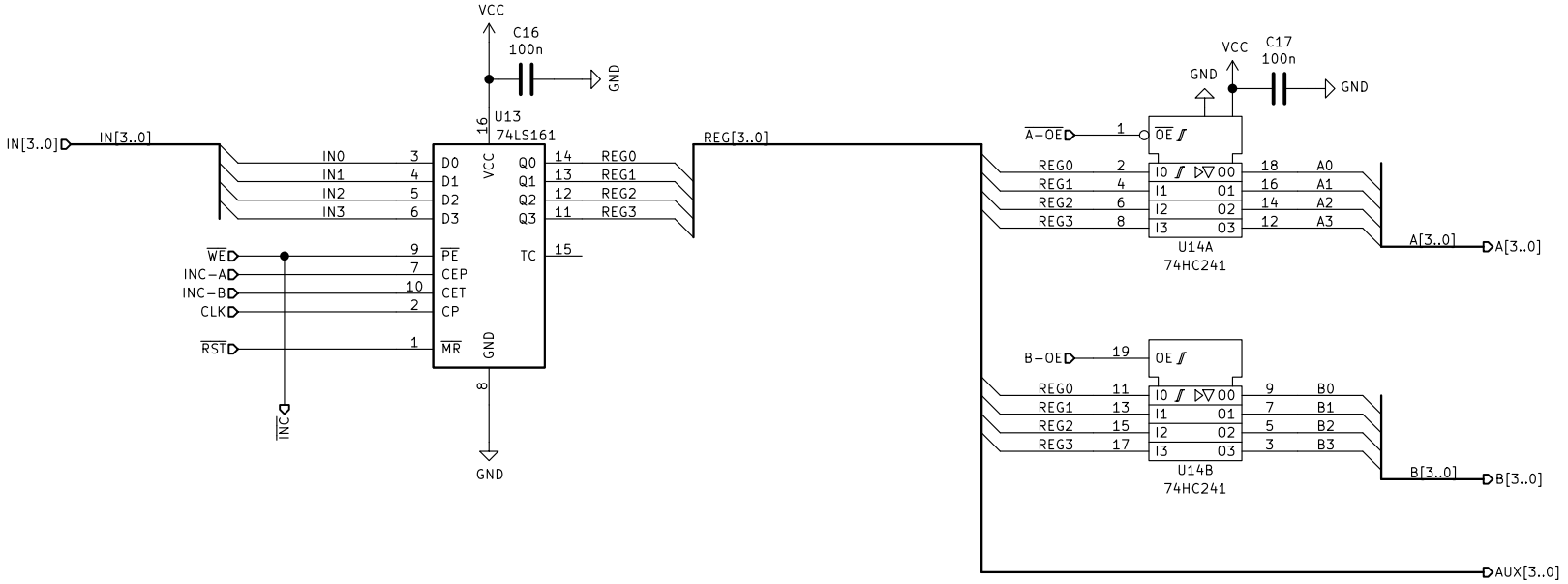
| KiCad E.D.A. eeschema 5.1.10 | | Id: 4/13 |


Sheet: R1
IN[3..0]
WE
INC-A
A-OE
B1
B-OE
RST
CLK
A[3..0]
B[3..0]
AUX[3..0]
INC-B
INC
File: REGISTER.sch
Sheet: R2
IN2
A2
B2
Sheet: R3
IN3
A3
B3
Sheet: R4
IN4
A4
B4
Sheet: R5
IN5
A5
B5
Sheet: R6
IN6
A6
B6
U9A
74HC04
U9B
74HC04
U9C
74HC04
U9D
74HC04
U9E
74HC04
U9F
74HC04
U9G
74HC04
U10
74LS138
U11
74LS138
U12
74LS238
C13
100n
C14
100n
C15
100n
C12
100n
VCC
GND
IN[3..0]
INC
RST
CLK
IN_SEL[2..0]
IN_SEL0
IN_SEL1
IN_SEL2
IN_EN
A_SEL[2..0]
A_SEL0
A_SEL1
A_SEL3
A_EN
B_SEL[2..0]
B_SEL0
B_SEL1
B_SEL2
B_EN
AUX[3..0]
AUX[7..4]
AUX[7..0]
REGISTER_FILE
IEEE Student Branch 1019
Sheet: /Hierarchy/REGISTER_FILE/
File: REGISTER_FILE.sch
Size: A4
Date: 2021-11-19
Rev: 1
KiCad E.D.A. eeschema 5.1.10
Id: 5/13




# REGISTER

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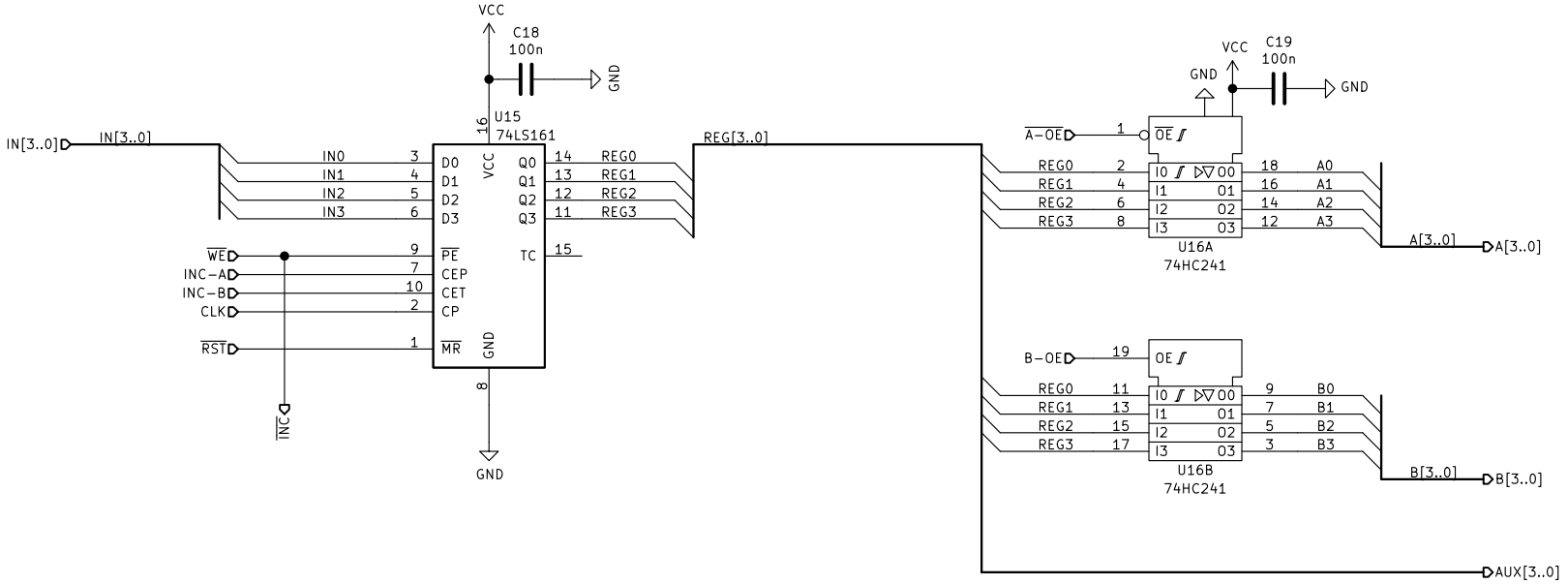


# REGISTER

**IEEE Student Branch 1019**

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File: REGISTER.sch

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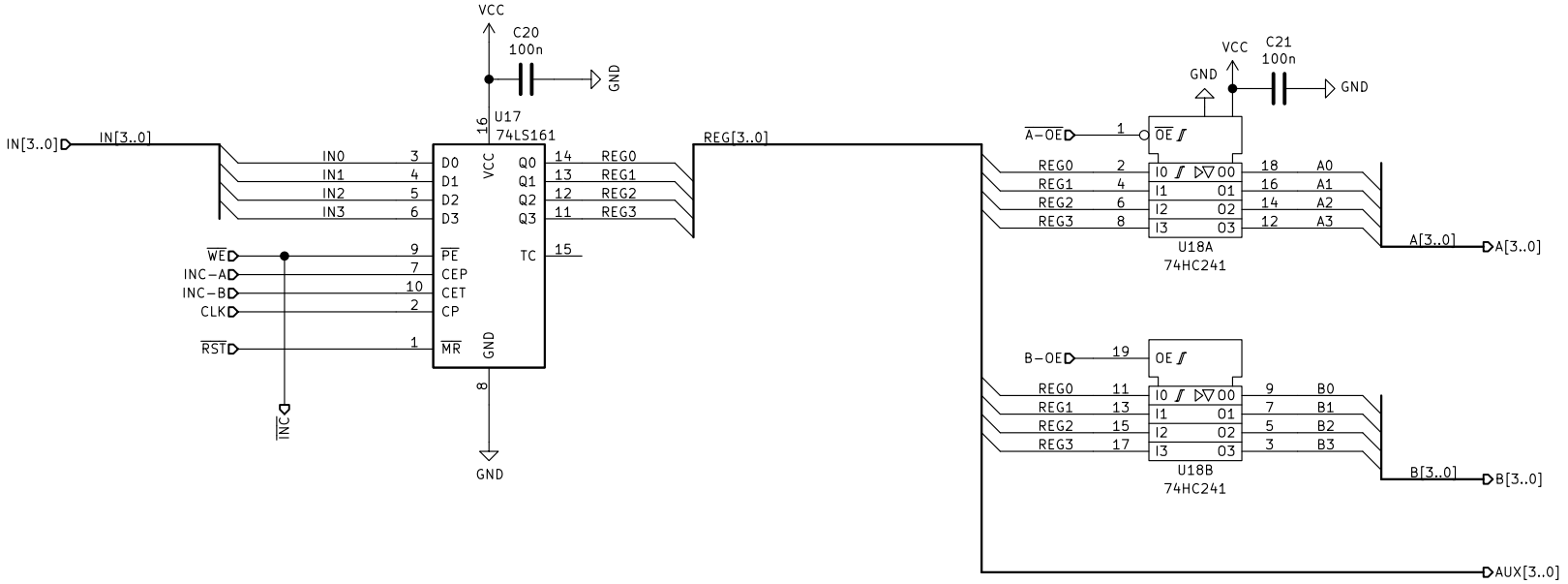
| KiCad E.D.A. eeschema 5.1.10 | | Id: 7/13 |




# REGISTER

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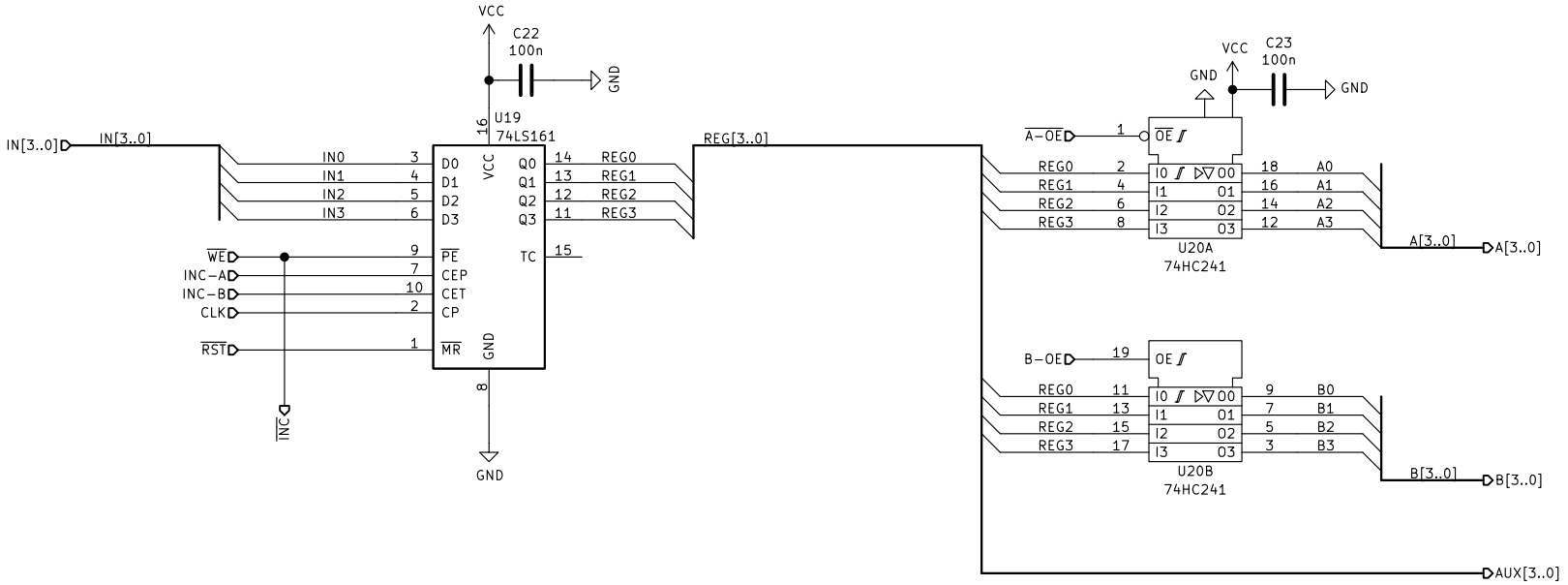


# REGISTER

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File: REGISTER.sch

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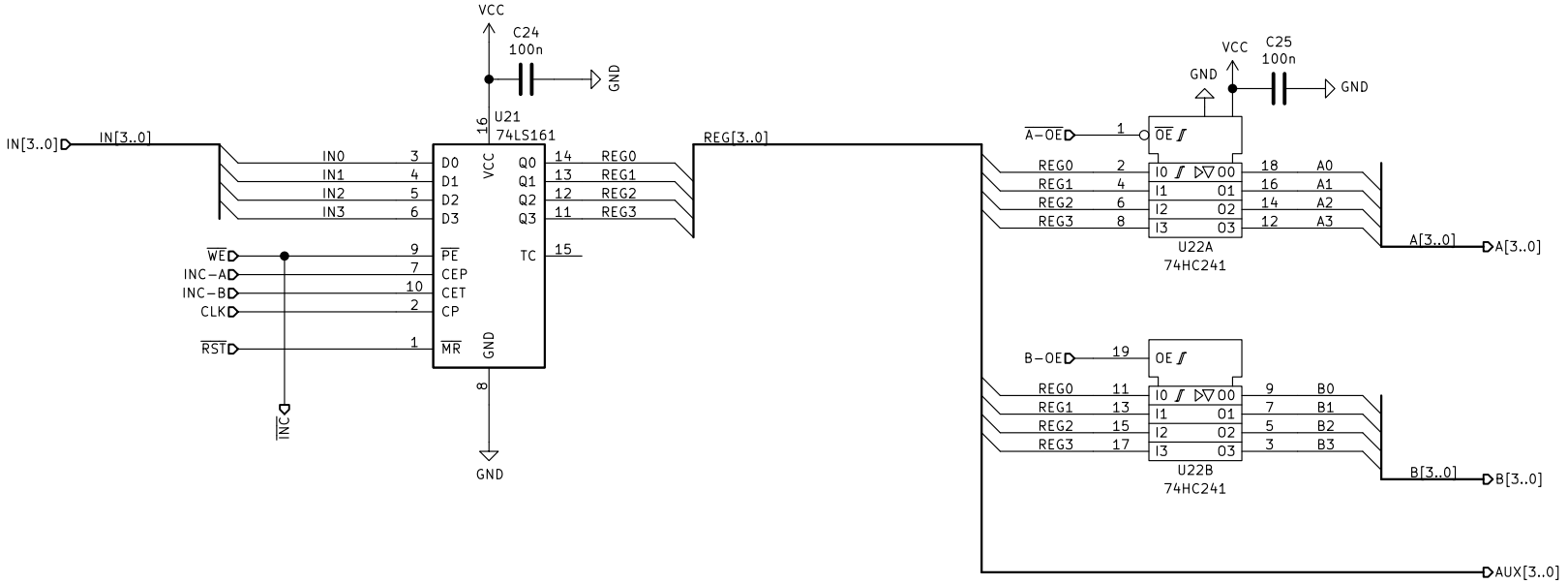


# REGISTER

**IEEE Student Branch 1019**

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File: REGISTER.sch

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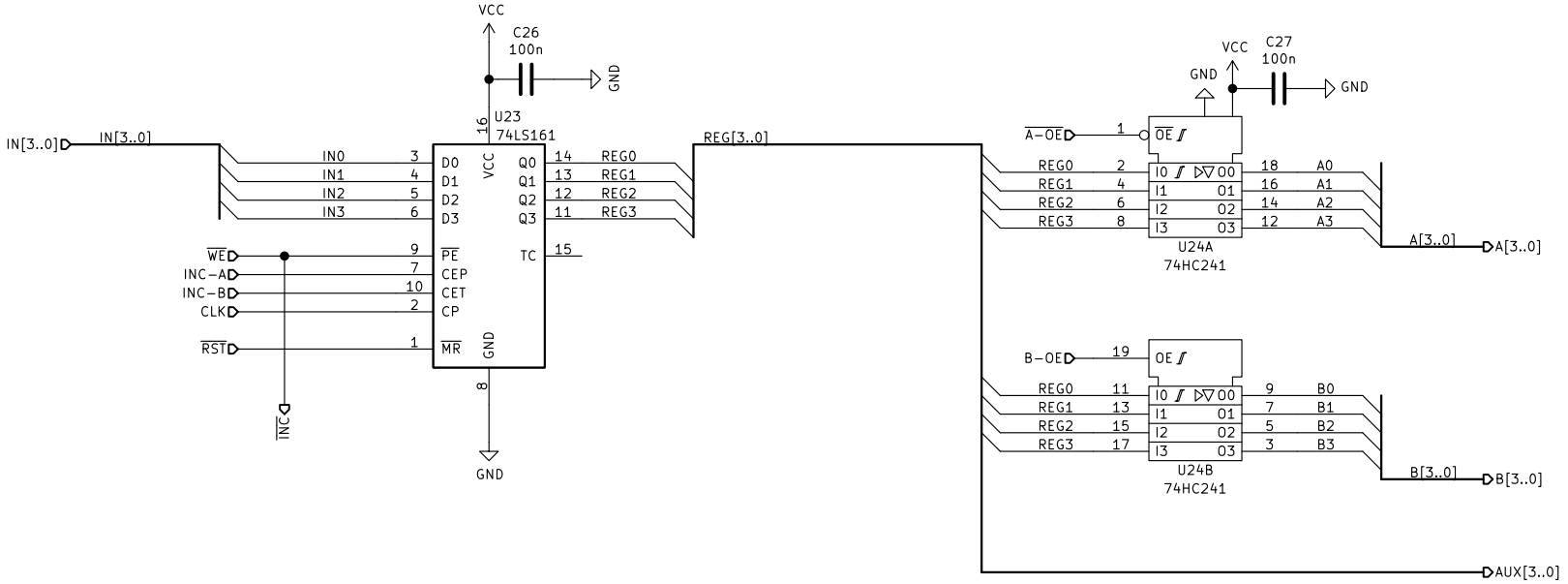
| Size: A4 | Date: 2021-11-19 | **Rev:** |
| KiCad E.D.A. eeschema 5.1.10 | | Id: 10/13 |




# REGISTER

**IEEE Student Branch 1019**

Sheet: /Hierarchy/REGISTER_FILE/R6/
File: REGISTER.sch

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| Size: A4 | Date: 2021-11-19 | **Rev:** |
| KiCad E.D.A. eeschema 5.1.10 | | Id: 11/13 |

# ALU

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Sheet: /Hierarchy/ALU/
File: ALU.sch

| | | |
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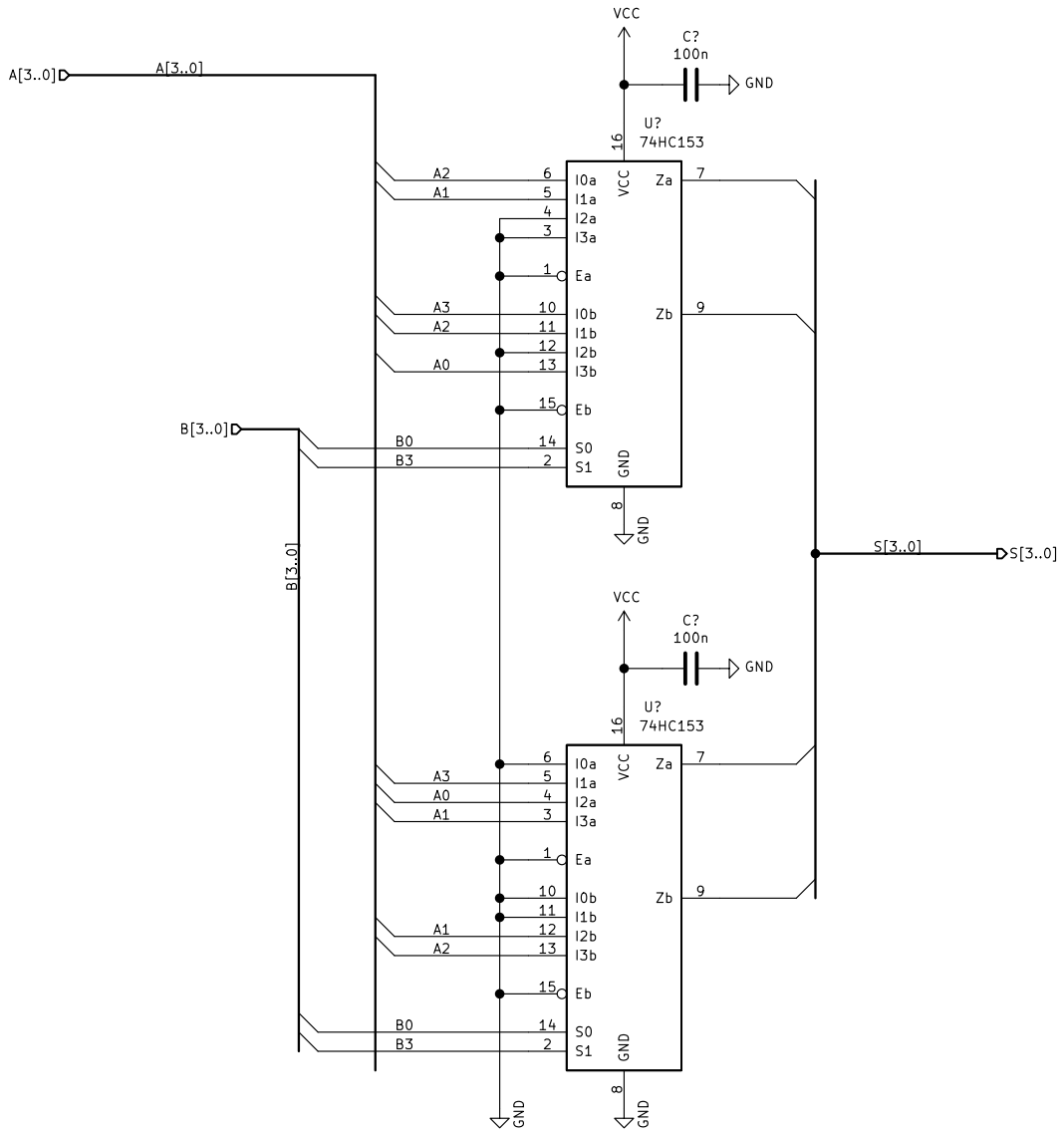
| Size: A3 | Date: 2021-12-20 | **Rev: 0** |
| KiCad E.D.A. eeschema 5.1.10 | | Id: 12/13 |




Questo circuito effettua lo shift logico del valore di A di una o due posizioni
in funzione del valore di B.
Le limitazioni del circuito sono:
- Non è possibile effettuare uno shift aritmetico
- Non è possibile effettuare shift di zero posizioni

Per motivi di complessità utiliziamo il seguente circuito invece che uno shifter completo.

La tabella di verità del circuito è la seguente.
Considerando l'input A come [A3 A2 A1 A0]

| B | S = A <> B | |
|---|---|---|
| B3 B2 B1 B0 | S3 S2 S1 S0 | |
| 0 0 0 1 | 0 A3 A2 A1 | S = A >> 1 |
| 0 0 1 0 | 0 0 A3 A2 | S = A >> 2 |
| 1 0 0 1 | A2 A1 A0 0 | S = A << 1 |
| 1 0 1 0 | A1 A0 0 0 | S = A << 2 |

Come è possibile notare gli effettivi bit di B utilizzati per lo shift sono B3 per la direzione e B0 per l'ammontare.
Questo comporta che eventuali combinazioni non legali
diano i seguenti risultati.

| B | S = A <> B | |
|---|---|---|
| B3 B2 B1 B0 | S3 S2 S1 S0 | |
| 0 0 0 0 | 0 0 A3 A2 | S = A >> 2 |
| 0 0 1 1 | 0 A3 A2 A1 | S = A >> 1 |
| 0 1 0 0 | 0 0 A3 A2 | S = A >> 2 |
| 0 1 0 1 | 0 A3 A2 A1 | S = A >> 1 |
| 0 1 1 0 | 0 0 A3 A2 | S = A >> 2 |
| 0 1 1 1 | 0 A3 A2 A1 | S = A >> 1 |
| 1 0 0 0 | A1 A0 0 0 | S = A << 2 |
| 1 0 1 1 | A2 A1 A0 0 | S = A << 1 |
| 1 1 0 0 | A1 A0 0 0 | S = A << 2 |
| 1 1 0 1 | A2 A1 A0 0 | S = A << 1 |
| 1 1 1 0 | A1 A0 0 0 | S = A << 2 |
| 1 1 1 1 | A2 A1 A0 0 | S = A << 1 |

# 4-BIT SHIFTER

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Sheet: /Hierarchy/ALU/SHIFTER/
File: 4BIT-SHIFTER.sch

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| Size: A4 | Date: 2021-12-20 | **Rev: 0** |
| KiCad E.D.A. eeschema 5.1.10 | | Id: 13/13 |