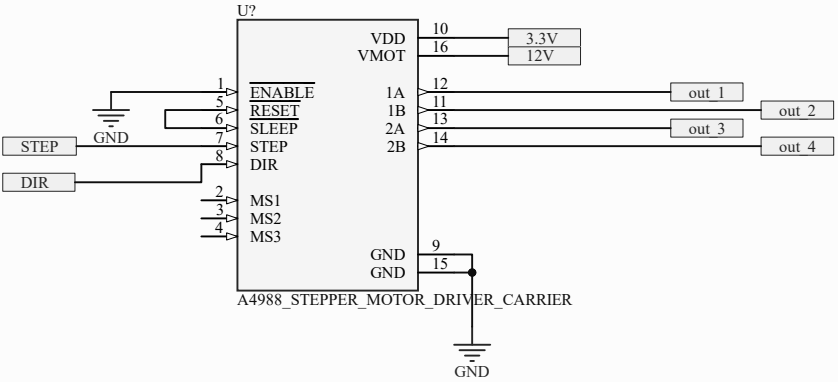
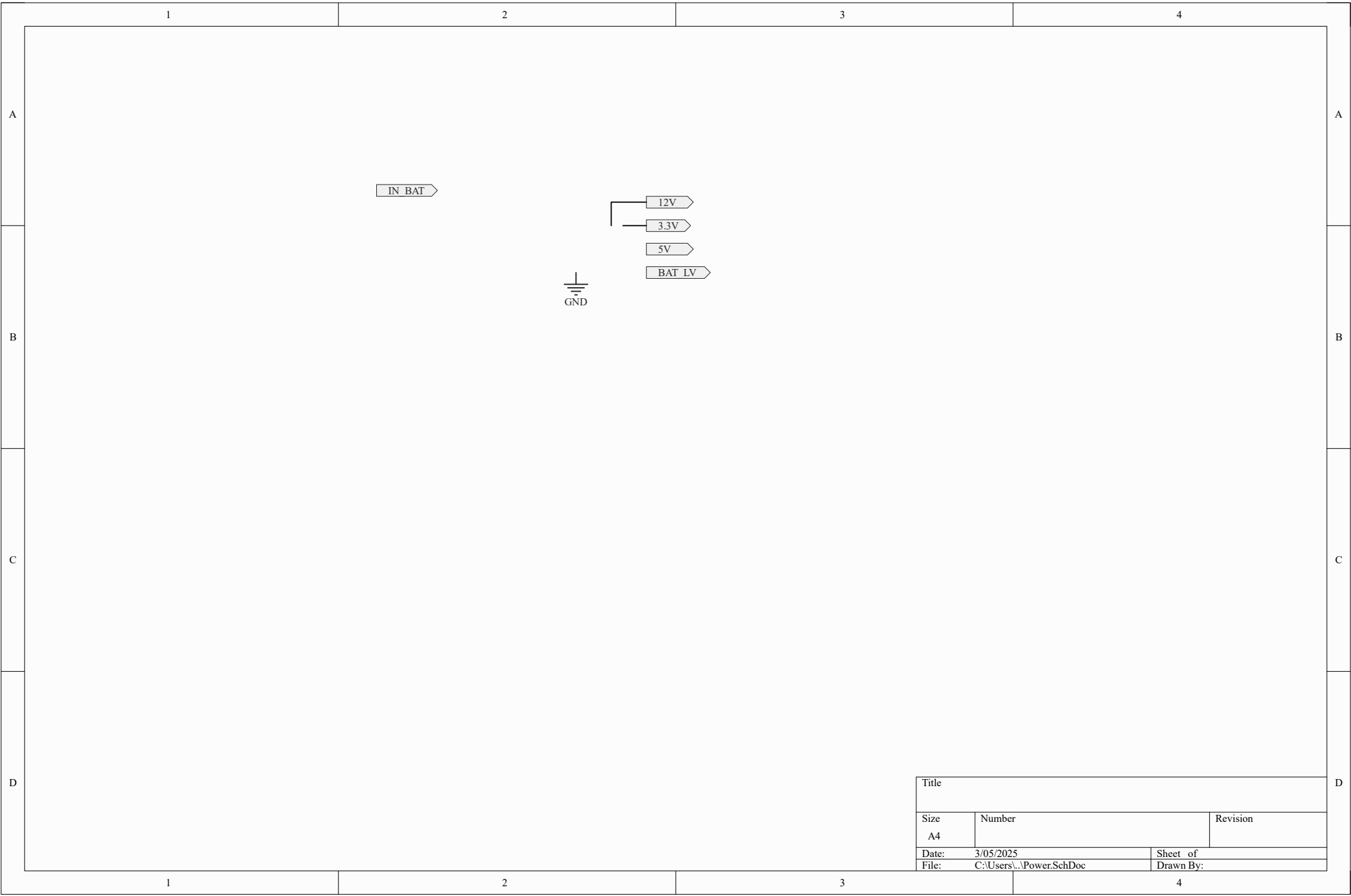


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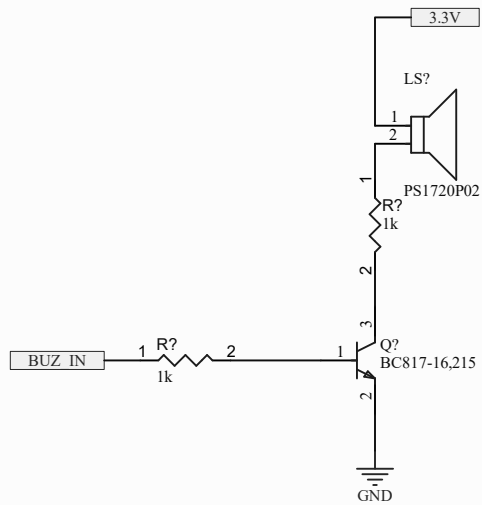


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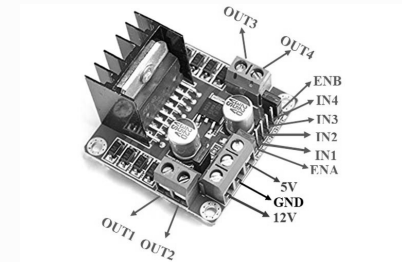
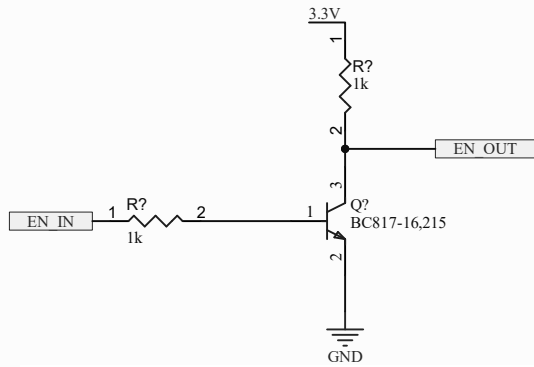
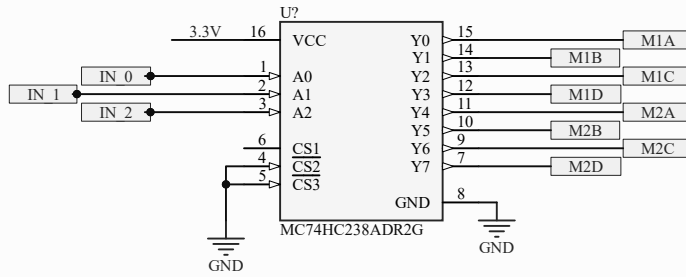




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3.3V

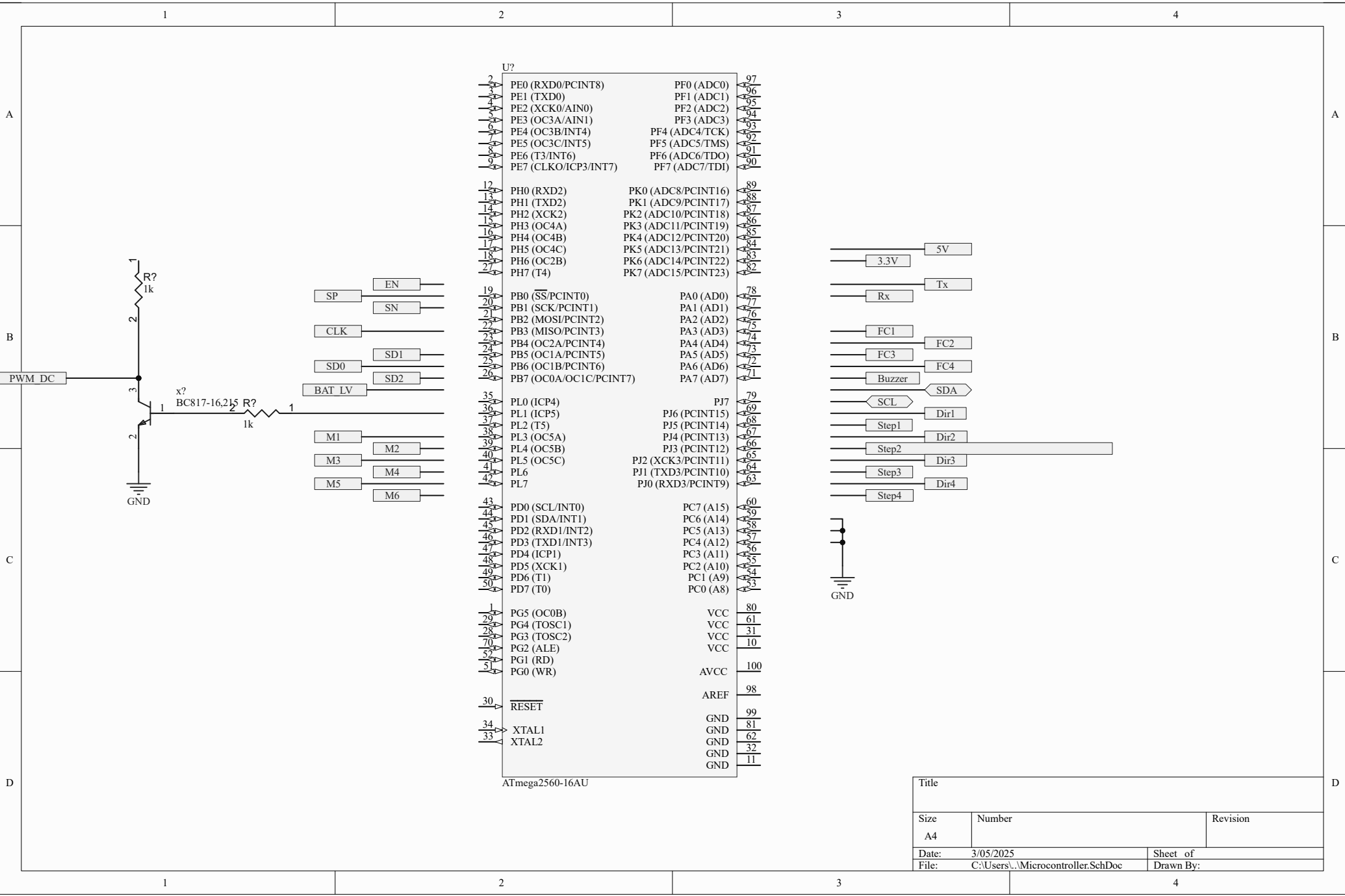
EN	IN1	IN2	ACTION	ACTION	EN	IN1	IN2	IN3	IN4
0	X	X	SOFT BRAKE	SAME+	1	1	0	1	0
1	0	0	HARD BRAKE	SAME-	1	0	1	0	1
1	1	1	HARD BRAKE	OPPOSITE+	1	1	0	0	1
1	0	1	DIR+	OPPOSITE-	1	0	1	1	0
1	1	0	DIR-	BRAKE	1	A	A	B	B
				OFF	0	X	X	X	X



TRUTH TABLE

Inputs						Outputs							
CS3	CS2	CS1	A0	A1	A2	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
H	X	X	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	X	L	L	L	L	L	L	L	L
X	X	L	X	X	X	L	L	L	L	L	L	L	L
L	L	H	L	L	L	H	L	L	L	L	L	L	L
L	L	H	H	L	L	L	H	L	L	L	L	L	L
L	L	H	L	H	L	L	L	H	L	L	L	L	L
L	L	H	H	H	L	L	L	L	H	L	L	L	L
L	L	H	L	L	H	L	L	L	L	H	L	L	L
L	L	H	H	L	H	L	L	L	L	L	H	L	L
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L	L	H	H	H	H	L	L	L	L	L	L	L	H

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## 5.3 DC Characteristics (3.3 V, 25 °C)

Table 7: DC Characteristics (3.3 V, 25 °C)

Symbol	Parameter		Min	Typ	Max	Unit
$C_{IN}$	Pin capacitance		-	2	-	pF
$V_{IH}$	High-level input voltage		$0.75 \times VDD^1$	-	$VDD^1 + 0.3$	V
$V_{IL}$	Low-level input voltage		-0.3	-	$0.25 \times VDD^1$	V
$I_{IH}$	High-level input current		-	-	50	nA
$I_{IL}$	Low-level input current		-	-	50	nA
$V_{OH}$	High-level output voltage		$0.8 \times VDD^1$	-	-	V
$V_{OL}$	Low-level output voltage		-	-	$0.1 \times VDD^1$	V
$I_{OH}$	High-level source current ( $VDD^1 = 3.3\text{ V}$ , $V_{OH} \geq 2.64\text{ V}$ , output drive strength set to the maximum)	VDD3P3_CPU power domain <sup>1, 2</sup>	-	40	-	mA
		VDD3P3_RTC power domain <sup>1, 2</sup>	-	40	-	mA
		VDD_SDIO power domain <sup>1, 3</sup>	-	20	-	mA

## 5 Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$I_{OL}$	Low-level sink current ( $VDD^1 = 3.3\text{ V}$ , $V_{OL} = 0.495\text{ V}$ , output drive strength set to the maximum)	-	28	-	mA
$R_{PU}$	Resistance of internal pull-up resistor	-	45	-	k $\Omega$
$R_{PD}$	Resistance of internal pull-down resistor	-	45	-	k $\Omega$
$V_{IL\_nRST}$	Low-level input voltage of CHIP_PU to shut down the chip	-	-	0.6	V

## Notes:

- Please see Appendix IO\_MUX of [ESP32 Datasheet](#) for IO's power domain. VDD is the I/O voltage for a particular power domain of pins.
- For VDD3P3\_CPU and VDD3P3\_RTC power domain, per-pin current sourced in the same domain is gradually reduced from around 40 mA to around 29 mA,  $V_{OH} \geq 2.64\text{ V}$ , as the number of current-source pins increases.
- Pins occupied by flash and/or PSRAM in the VDD\_SDIO power domain were excluded from the test.

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Table 7: DC Characteristics (3.3 V, 25 °C)

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		VDD3P3_RTC power domain <sup>1, 2</sup>	-	40	-	mA
		VDD_SDIO power domain <sup>1, 3</sup>	-	20	-	mA

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		VDD3P3_RTC power domain <sup>1, 2</sup>	-	40	-	mA
		VDD_SDIO power domain <sup>1, 3</sup>	-	20	-	mA

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A

A

B

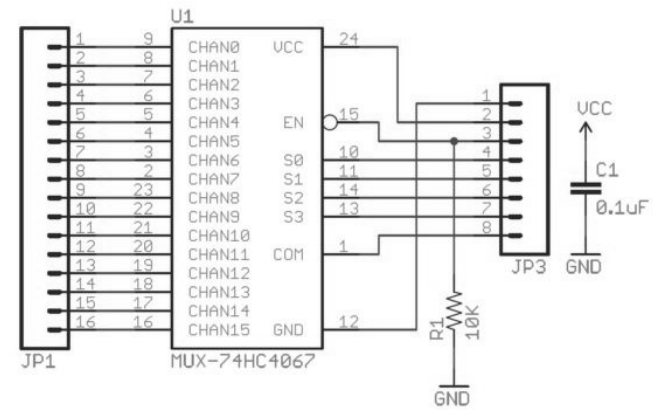
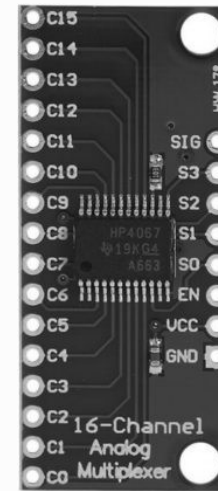
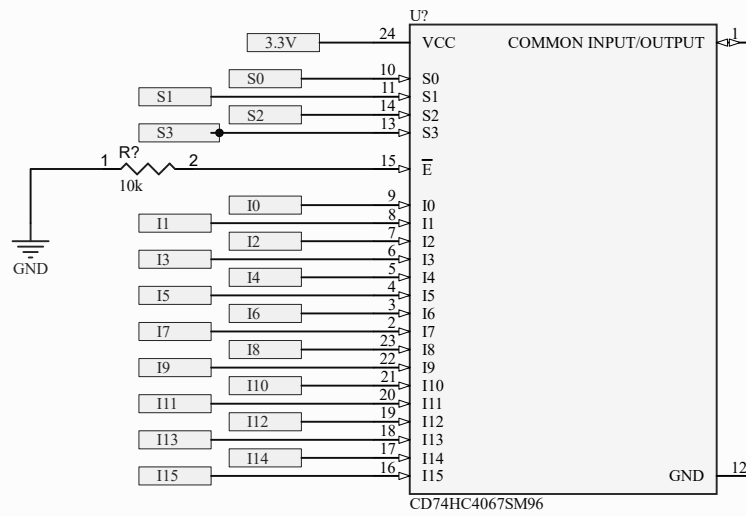
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