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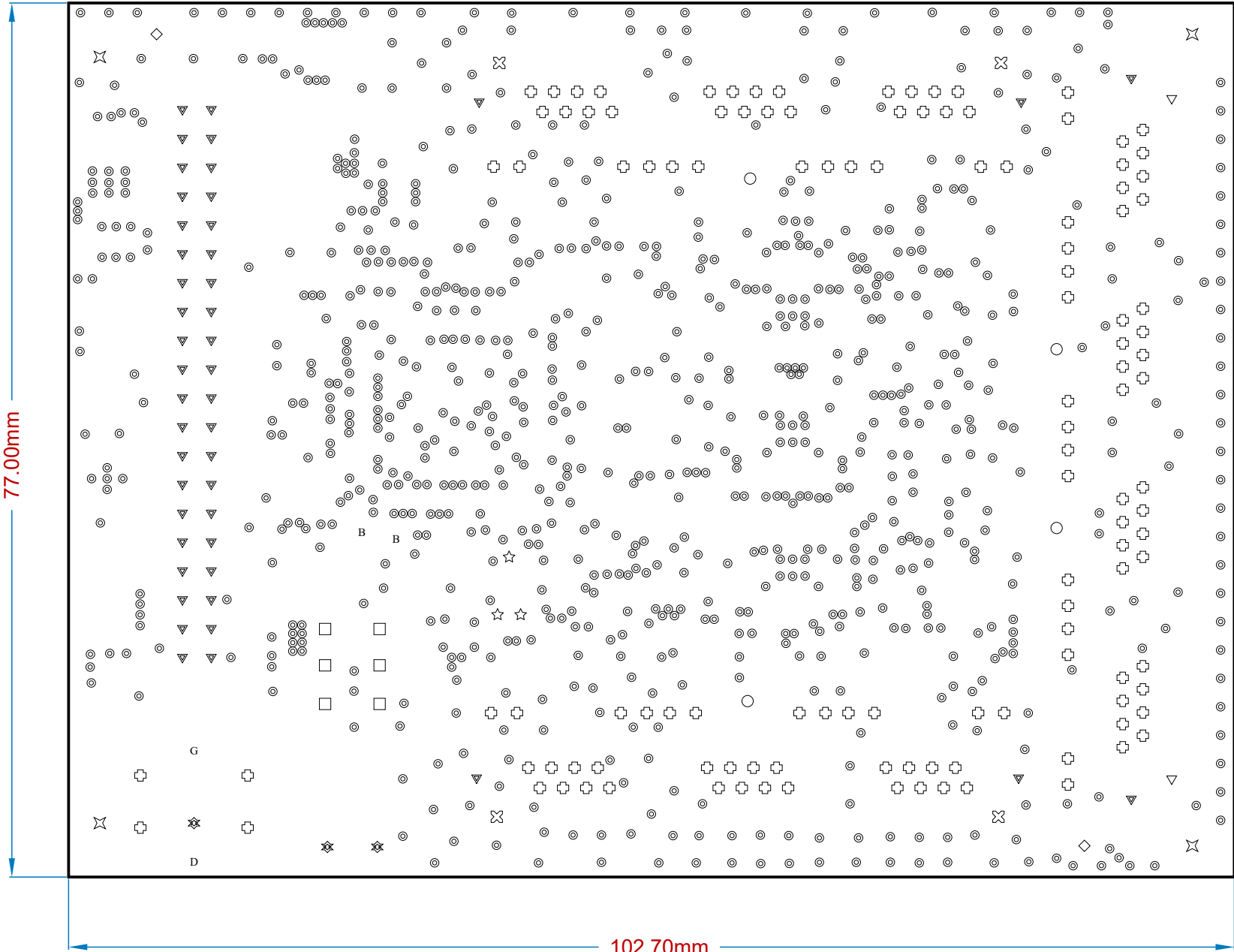
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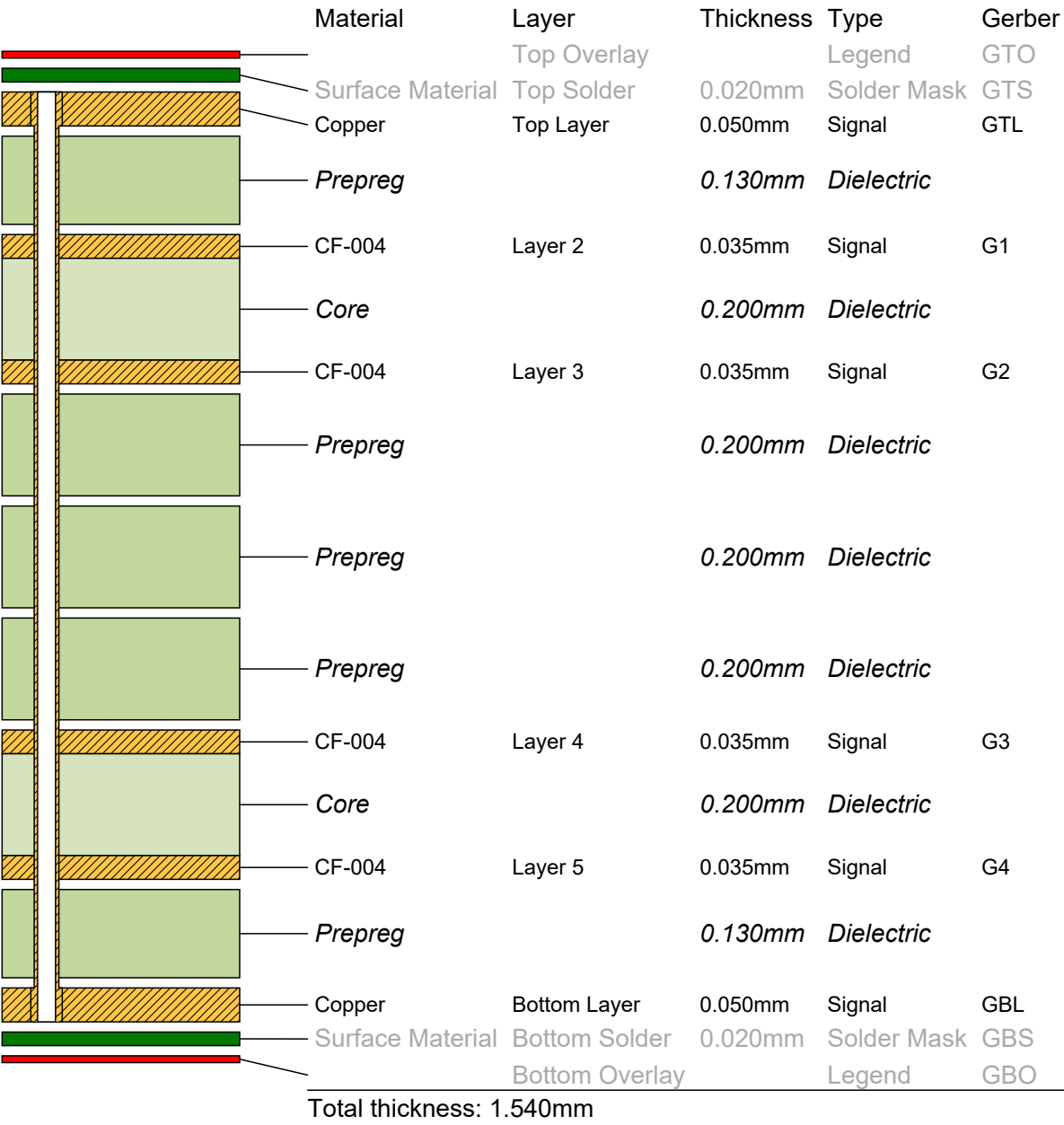
8



Drill Table

Symbol	Count	Hole Size	Plated	Hole Tolerance
⊙	851	0.30mm	Plated	
✱	3	0.70mm	Plated	
⊕	124	0.90mm	Plated	
☆	3	1.00mm	Non-Plated	
▼	46	1.10mm	Plated	
Ⓑ	2	1.20mm	Plated	
Ⓖ	1	1.50mm	Plated	
○	4	1.60mm	Plated	
Ⓓ	1	1.70mm	Non-Plated	
□	6	1.70mm	Plated	
◇	2	2.00mm	Non-Plated	
⊠	4	2.80mm	Plated	
⊞	4	3.20mm	Non-Plated	
▽	2	3.25mm	Non-Plated	
1053 Total				

Stack-up Legend



PCB Fabrication Notes

- All materials shall be RoHS compliant and final product shall be accepted to use in RoHS assembly
- Board shall be fabricated according to IPC-6012E Class 2 standard
- Number of layers - 6
- Board size - 102.7mm x 77mm. Tolerance - +/- 0.1mm
- Board thickness - 1.54mm +/-10% (see stack-up data)
- Material - FR-4 High Tg, cooper thickness is 35um (1oz) + plating (see stack-up data)
- Stack-up data is shown for reference and may be changed with notification
- Solder Mask shall be applied on two sides, PURPLE, liquid. Solder mask mis-registration +/-0.05mm. No overlap permitted on SMD lands. Solder Mask is in accordance with IPC-SM-840 D, Class H
- Silkscreen - white, both sides
- Type of finish - ENIG
- Electrical test shall be performed on both sides
- Min. plated hole size - 0.3mm
- Min. annular ring - 0.15mm
- Min. trace width/clearance - 0.125mm
- Non-functional pads (NFP) shall be removed
- This data also exists in CAD gerber format. In case of any discrepancies gerber data prevails.

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN MILLIMETERS SURFACE FINISH: TOLERANCES:		FINISH:			DEBURR AND BREAK SHARP EDGES	DO NOT SCALE DRAWING		REVISION 3.3		
		NAME	SIGNATURE	DATE			TITLE:  RRRC V2 Carrier Board Fabrication Drawing			
DRAW	A.Chirkun		17.04.23							
CHKD	A.Kovalenko		17.04.23							
APPV'D										
MFG										
QA					MATERIAL:		DWG NO.		A2	
					WEIGHT:	SCALE 2:1		SHEET 1 OF 1		