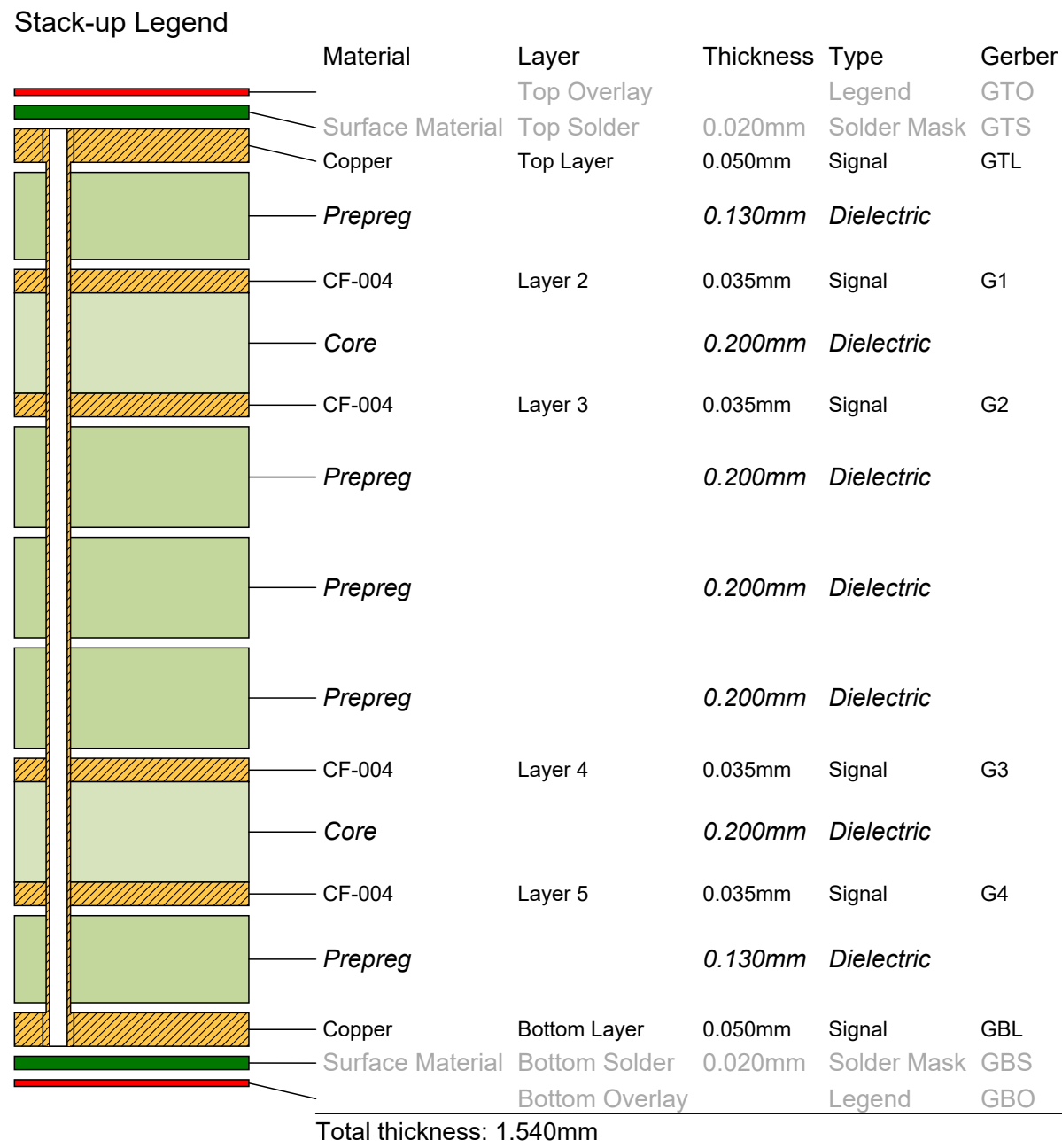


Drill Table				
Symbol	Count	Hole Size	Plated	Hole Tolerance
⊙	978	0.30mm	Plated	
✳	3	0.70mm	Plated	
⊕	124	0.90mm	Plated	
☆	3	1.00mm	Non-Plated	
▽	46	1.10mm	Plated	
B	2	1.20mm	Plated	
G	1	1.50mm	Plated	
○	4	1.60mm	Plated	
D	1	1.70mm	Non-Plated	
□	6	1.70mm	Plated	
◇	2	2.00mm	Non-Plated	
✳	4	2.80mm	Plated	
✳	4	3.20mm	Non-Plated	
▽	2	3.25mm	Non-Plated	
1180 Total				



PCB Fabrication Notes

1. All materials shall be RoHS compliant and final product shall be accepted to use in RoHS assembly
2. Board shall be fabricated according to IPC-6012E Class 2 standard
3. Number of layers - 6
4. Board size - 102.7mm x 77mm. Tolerance - +/- 0.1mm
5. Board thickness - 1.54mm +/-10% (see stack-up data)
6. Material - FR-4 High Tg, copper thickness is 35um (1oz) + plating (see stack-up data)
7. Stack-up data is shown for reference and may be changed with notification
8. Solder Mask shall be applied on two sides, PURPLE, liquid. Solder mask mis-registration +/-0.05mm. No overlap permitted on SMD lands. Solder Mask is in accordance with IPC-SM-840 D, Class H
9. Silkscreen - white, both sides
10. Type of finish - ENIG
11. Electrical test shall be performed on both sides
12. Min. plated hole size - 0.3mm
13. Min. annular ring - 0.15mm
14. Min. trace width/clearance - 0.125mm
15. Non-functional pads (NFP) shall be removed
16. This data also exists in CAD gerber format. In case of any discrepancies gerber data prevails.

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN MILLIMETERS SURFACE FINISH: TOLERANCES:		FINISH:		DEBURR AND BREAK SHARP EDGES		DO NOT SCALE DRAWING		REVISION 2.2	
						TITLE: RRRC V3 Carrier Board Fabrication Drawing			
DRAW	NAME Y.Aishanik	SIGNATURE	DATE 12.06.24						
CHK'D	A.Kovalenko		12.06.24						
APP'VD									
MFG									
QA				MATERIAL:		DWG NO.		A2	
				WEIGHT:		SCALE 2:1		SHEET 1 OF 1	