Lab 2 and 3: Design of Counter on FPGA

(Please refer "**Lab 1**" document for a review of all the steps in the design flow)

1. Create a Vivado Project and write Verilog code (**Counter_N.v**) for 4-bit Counter The 4-bit counter has **Clk** (clock), **Reset** as inputs and 4-bit **Count** as output. Reset is active high. Hence if **Reset**=0 then Count gets incremented on **positive edge of Clk**. If Reset=1 then the Count is reset to 0. Please use same port names as mentioned.

2. Write the test bench **Test_Counter_N.v** and simulate your design to check the functionality. (Please go through the comments)

3. Plan your I/O mapping (using **I/O planning** option) such that **Clk** and **Reset** are connected to push button switches and **Count** is connected to LEDs. Connect the clock to **T18** (Push button) of the ZedBoard. Connect the Reset pin to **R18** (Push button). Connect output **i.e. Count** to **U21, U22, T21, T22** (LEDs)**,** where U21 is MSB and T22 is LSB. Save the mapping information as **Count.xdc**.
   Push button are generally not used as **Clk** (clock) in complex designs. Hence if you go ahead with synthesis and implementation. It will give a routing error saying "Poor placement for routing…..". To avoid (override) this add the following statement to **.xdc** file.

   set_property CLOCK_DEDICATED_ROUTE FALSE [get_nets <ClkSignalName>_IBUF]

   if the Clock signal is defined as "**Clk**", the you have to add the following statement to **Count.xdc** file

   set_property CLOCK_DEDICATED_ROUTE FALSE [get_nets Clk_IBUF]

4. Synthesize (**Run Synthesis**) and Implement the design (**Run Implementation)**.

5. **Generate Bitstream**
   (Note: Since the Push button is used as clock, the output Count may skip some values due to switch debouncing)

6. Edit (you can edit the **.xdc** file by double clicking on the file name) the **Count.xdc** file such that **Clk** is connected to internal Clock instead of push button switch. In the ZedBoard, internal clock pin is **Y9**. Since the **Clk** is now connected to clock source, you can comment/remove the statement (i.e. **set_property CLOCK_DEDICATED_ROUTE FALSE [get_nets Clk_IBUF]**) we had adder earlier. Save the **Count.xdc** file (**Ctrl-S**).

   The internal clock is of frequency 100MHz. Hence if we directly use this clock then counting will not visible to the naked eye. Hence the internal clock should be divided (such that clock frequency reduces to 1 Hz) before it is used for counting. Modify Verilog code (**Counter_N.v**) to include clock division.

   Repeat Steps 4 to 6 i.e.

7. Synthesize (**Run Synthesis**) and Implement the design (**Run Implementation)**.

8. **Generate Bitstream**