Minilab 1a

Github Link: https://github.com/SUBRAMANYA-IV/ECE554SP26_Minilab1

Repo was created by cloning my parenters repo (so there could be shared contributions) via the linux command line, then forking this repo once all the work was done to have my own private version of said repo.
The folder was cloned onto the local using the “git clone” command, and any time changes were made, the git add->commit-> push cycle was used to sync the changes with the remote repo, such that everyone had the newest version of RTL.

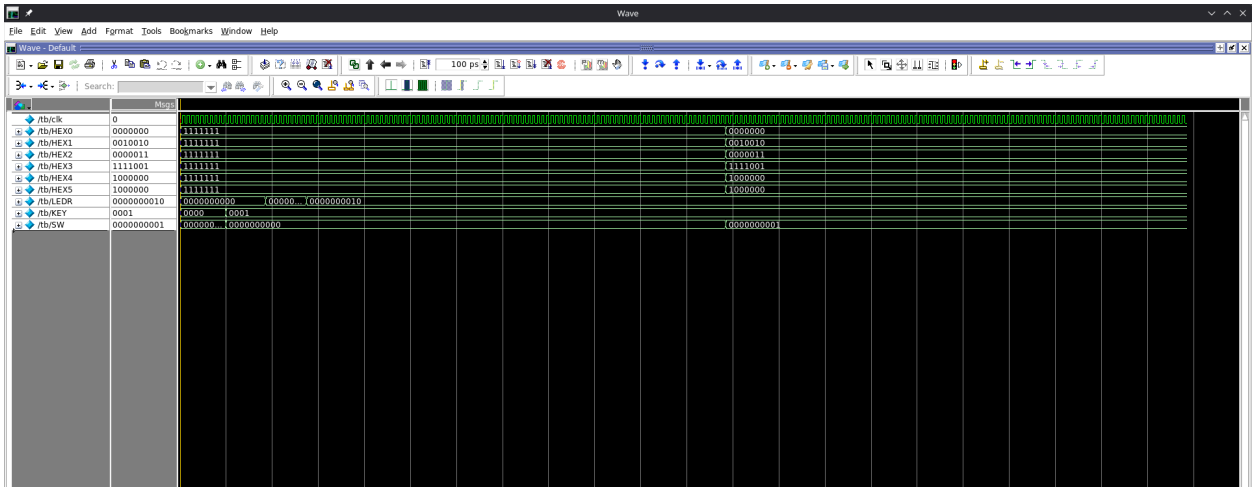
Transcript with IP:

```
# do run.do
 # ** Warning: (vlib-34) Library already exists at "work".
 # Model Technology ModelSim - Intel FPGA Edition vlog 10.5b Compiler
2016.10 Oct  5 2016
 # Start time: 16:14:03 on Feb 05,2026
 # vlog -reportprogress 300 -work work addsb_bb.v addsb.v fifo.sv
mac.sv mult_mod_bb.v mult_mod.v tb.sv fifo2_bb.v fi
 fo2.v Minilab0.v
 # -- Compiling module addsb
 # ** Warning: addsb.v(40): (vlog-2275) 'addsb' already exists and
will be overwritten.
 # -- Compiling module addsb
 # -- Compiling module FIFO
 # -- Compiling module MAC
 # -- Compiling module mult_mod
 # ** Warning: mult_mod.v(40): (vlog-2275) 'mult_mod' already exists
and will be overwritten.
 # -- Compiling module mult_mod
 # -- Compiling module tb
 # -- Compiling module fifo2
 # ** Warning: fifo2.v(40): (vlog-2275) 'fifo2' already exists and
will be overwritten.
 # -- Compiling module fifo2
 # -- Compiling module Minilab0
 #
 # Top level modules:
 #       addsb
 #       mult_mod
 #       tb
 #       fifo2
 # End time: 16:14:03 on Feb 05,2026, Elapsed time: 0:00:00
 # Errors: 0, Warnings: 3
 # vsim -L
/home/michael2/Documents/intelFPGA/18.1/modelsim_ase/altera/verilog/a
ltera_mf -L /home/michael2/Documents/
```

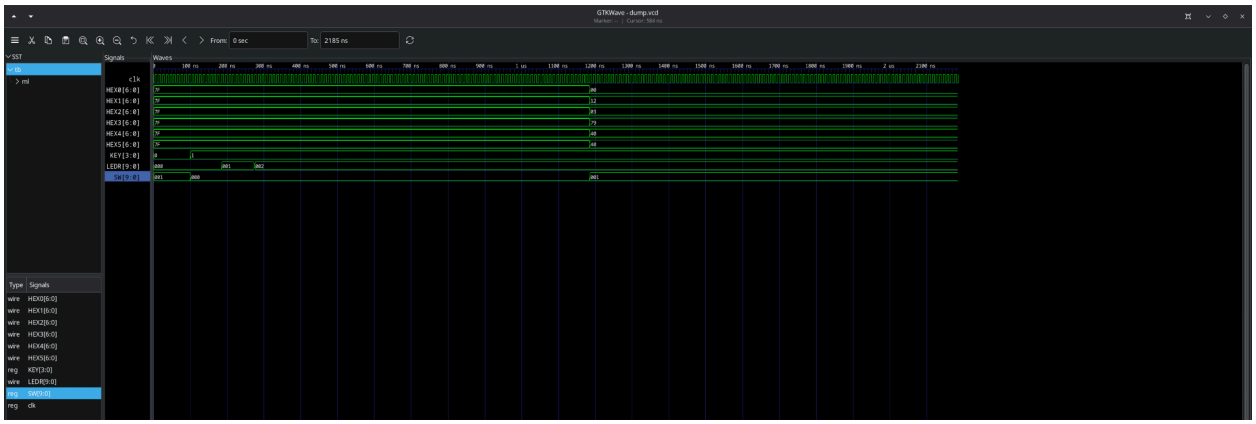
```
 intelFPGA/18.1/modelsim_ase/altera/verilog/220model work.tb
-voptargs="+acc"
 # Start time: 16:14:03 on Feb 05,2026
 # Loading sv_std.std
 # Loading work.tb
 # Loading work.Minilab0
 # Loading work.MAC
 # Loading work.FIFO
 # ** Warning: (vsim-3116) Problem reading symbols from
linux-gate.so.1 : can not open ELF file.
 # ** Warning: (vsim-3116) Problem reading symbols from
/lib/libpthread.so.0 : module was loaded at an absolute addre
 ss.
 # ** Warning: (vsim-3116) Problem reading symbols from
/lib/librt.so.1 : module was loaded at an absolute address.
 # ** Warning: (vsim-3116) Problem reading symbols from
/lib/libdl.so.2 : module was loaded at an absolute address.
 # ** Warning: (vsim-3116) Problem reading symbols from
/lib/libm.so.6 : module was loaded at an absolute address.
 # ** Warning: (vsim-3116) Problem reading symbols from
/lib/libc.so.6 : module was loaded at an absolute address.
 # ** Warning: (vsim-3116) Problem reading symbols from
/lib/ld-linux.so.2 : module was loaded at an absolute address
 .
 # Yahoo! All tests passed!
 # ** Note: $finish    : tb.sv(66)
 #    Time: 2185 ns  Iteration: 0  Instance: /tb
 # 1
 # Break in Module tb at tb.sv line 66
 add wave -position insertpoint  \
 sim:/tb/clk \
 sim:/tb/HEX0 \
 sim:/tb/HEX1 \
 sim:/tb/HEX2 \
 sim:/tb/HEX3 \
 sim:/tb/HEX4 \
 sim:/tb/HEX5 \
 sim:/tb/LEDR \
 sim:/tb/KEY \
 sim:/tb/SW
 restart -f
 # Closing VCD file "dump.vcd"
 run -all
 # ** Warning: (vsim-3116) Problem reading symbols from
linux-gate.so.1 : can not open ELF file.
 # ** Warning: (vsim-3116) Problem reading symbols from
/lib/libpthread.so.0 : module was loaded at an absolute addre
 ss.
 # ** Warning: (vsim-3116) Problem reading symbols from
/lib/librt.so.1 : module was loaded at an absolute address.
 # ** Warning: (vsim-3116) Problem reading symbols from
/lib/libdl.so.2 : module was loaded at an absolute address.
```

```
 # ** Warning: (vsim-3116) Problem reading symbols from
/lib/libm.so.6 : module was loaded at an absolute address.
 # ** Warning: (vsim-3116) Problem reading symbols from
/lib/libc.so.6 : module was loaded at an absolute address.
 # ** Warning: (vsim-3116) Problem reading symbols from
/lib/ld-linux.so.2 : module was loaded at an absolute address
 .
 # Yahoo! All tests passed!
 # ** Note: $finish    : tb.sv(66)
 #    Time: 2185 ns  Iteration: 0  Instance: /tb
 # 1
 # Break in Module tb at tb.sv line 66
```

- The waveform demonstrates the waves using the IP



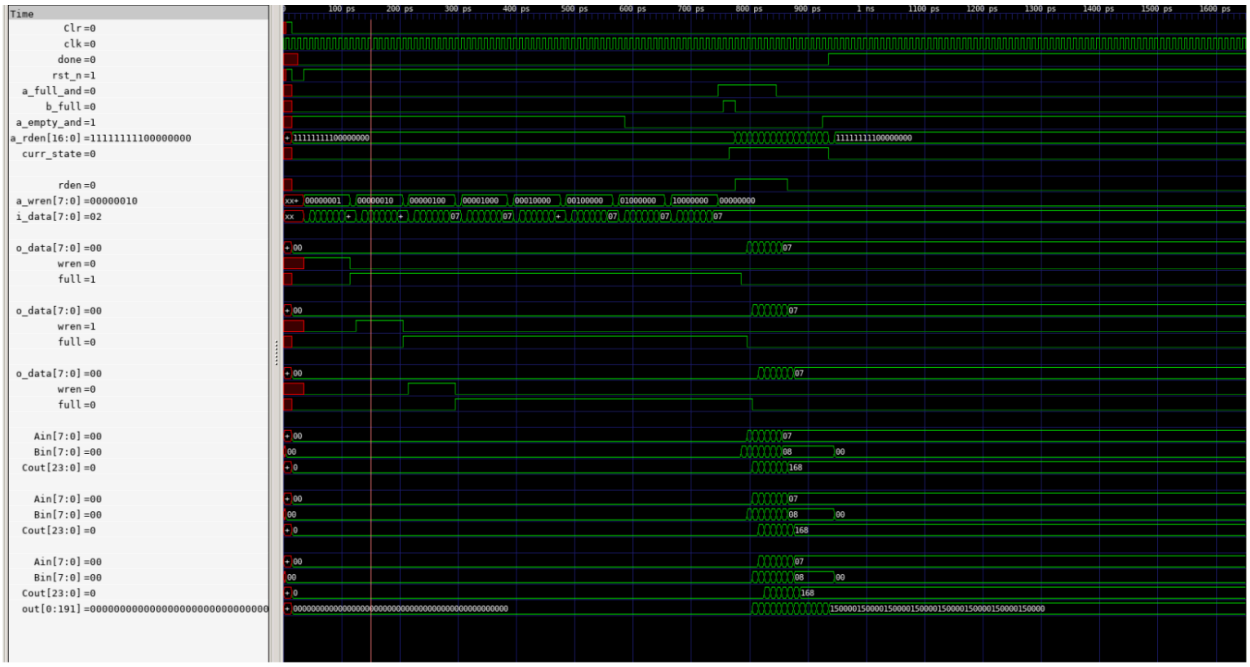
- The waveform below is without the IP



Using the IP had significantly lower resource utilization

Minilab 1b

The github page was created by first cloning the remote repository created by my partner, modifying it, going through the git add->commit->push/pull cycle, and then creating a fork for my own, unique version of the project.
Quartus files were added by running quartus synthesis in the directory, and then pushing/pulling the files to sync them.



The design was tested by first writing a simple testbench specifically for the mat_vec_mult module, and then integrating it with the avalon data interface, reading data from the ROM (read from the mif file), and then sequentially filling up FIFOS for the a matrix, and then determining if the output is correct.