# Fabrication and I-V Curve Characterization of Silicon Homojunction Diode Using Si Nanomembrane Grafted onto an Amorphous Aluminum Oxide Dielectric Interface

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ORANGE HIGHLIGHTED SECTIONS ARE PLACES THAT I COULD USE SOME SUGGESTIONS

**FABRICATION/PROCESS STEPS STILL NEEDED FOR THE PAPER:**

1. Refabricate Si/Si devices for: **(waiting for new n-/n+ Si substrates since Donghyeok said that the old substrate structures aren't right)**
    a. More data to support a baseline for our grafting process with higher statistical significance
    b. Device breakdown testing
    c. Optimizing fabrication processes
    d. CV measurements (should help show if there are any residual charges or interface traps?)
        i. need to look more into theory basis of CV testing on diodes
        ii. What experiment parameters should be used (voltage, scan speed, etc…) and what measurement variables should be focused on?
    **e.** Should new devices test out both Al2O3 as well as HfO2 interface material to compare the two?
        **i.** Talked with PMa and decided on testing out multiple HfO2 pieces at the same time to optimize the HfO2 annealing temp/time by seeing which conditions result in the best devices

2. TEM/SEM image of diode cross section to show interface layer between the host substrate and NM.

3. Use Silvaco software to try modeling different types of Si diode junctions (IE with diffused depletion zone ect...)

**CONTENT THAT NEEDS TO BE EXPANDED UPON:**

**4. Need to emphasize that our device is:**

**a. characterized by ideal diode equation**

**b. a model system for showing that the NM grafting works and produces devices with performances as good as, or better, than traditionally fabricated products. This is why we are making a homojunction for a better direct comparison of process baselines**

**c. being used to establish a baseline for future, more complex, device grafting work**

**d.** Should plots of the ideality factor vs voltage be included or just have the minimized ideality factor value stated? If just the minimum value, should that choice be explained in the paper?

5. Ideality Factor Experimental Calculations:

a. Looks like there are a few different ways that papers calculate the ideality factors so may want to try out a few different methods to see how well they agree with each other (the method we use definitely seems to be the most commonly employed though)

b. What voltage range are the device ideality factors normally recorded in (since the IF and recombination mechanisms will depend on the applied voltage)

6. Should we include values for the current density by estimating it using the approximate area of the smaller contact, 40x40um, as the diode size?

7. Should we mention that all of the results here are without any post metallization anneal? Might cause the current density magnitude to be lower than other devices?

8. Need to research a lot more about silicon diode performance/parameters using traditional fabrication techniques (wafer bonding, diffused junction, etc…) and how those values compare to our grafted devices

    a. Ideality factor is one parameter that we may want to focus specifically on because most traditional devices tend to assume that this factor will be about 2 at low voltages due to recombination traps in the device junction, but ours should be able to approach much closer to 1 due to having a high-quality abrupt junction

    b. Jiarui sent over paper about bonded wafers (Ref 13)

    c. Might want to also look up the approximate size of these junctions to try and compare? Or maybe just try to figure out the increase in junction size that is needed for the different techniques?

9. A lot of papers include the built-in potentials. Most of the ones I've seen are on photodetector papers, but this is one of the main parameters that is reported

**Abstract:**

**(Need to change the abstract so that it shows that the paper is focused much more on the successes of the grafting process, without any detriments, in order to lay the foundations for future work. Right now it sounds like the purpose of the paper and work was just to make a good diode)**

In this work, we present the fabrication process and electrical results of an Si/Si diode created by grafting a p+ silicon nanomembrane onto an n-type silicon host substrate coated with a 0.5nm thick amorphous layer of $Al_2O_3$. Both a high on/off current ratio above 2E4 at 1V

bias as well as a diode ideality factor of 1.05 were obtained demonstrating the excellent interface junction quality and rectifying behavior of the fabricated device. The excellent electrical performances of the individual diodes, as well as our demonstration of scaling the grafting process up to 2-in full wafers while maintaining high yield and uniformity, lay the foundation for future experimentation and development of lattice mismatched heterostructure devices.

**Introduction:**

The most common fabrication methods used to form PN junctions rely on either epitaxial growth or a diffusion-controlled process. While these methods have successfully formed the basis of most semiconductor devices developed in the last century, they each come with inherent problems. The most common problems that arise during fabrication are due to the difficulties involved with creating an abrupt junction interface. Most techniques require a graded junction volume to reduce interface defects and strain or due to the behavior of diffusion mechanisms. These problems decrease both speed and efficiency and place a limit on how small the devices can be.

To facilitate the next generation of semiconductor devices that contain smaller heterostructure interfaces not restricted to materials with similar lattice constants, new fabrication techniques are needed. One of the most exciting methods developed in the last couple of decades utilizes the grafting of nanomembranes onto bulk substrates of a different material.

Unlike devices grown using epitaxy, grafted structures contain an abrupt transition at the interface of the two regions. Having an abrupt junction not only allows for smaller devices, but also reduces interface traps and charge carrier recombination which helps produce diodes that more closely follow the Shockley ideal diode model.

NM grafting circumvents many challenges that epitaxy and wafer bonding/fusion run into, especially when involving materials with different lattice parameters. By circumventing the problems that arise from differences in lattice constants, semiconductor grafting allows us to create devices that combine the favorable mechanical and electrical properties from distinct materials.

To mitigate any detriments caused by defects or mechanical strain that might arise from mismatched lattices at the device junction interface, a thin 0.5nm thick layer of $Al_2O_3$ is coated

onto the surface of the host substrate using Atomic Layer Deposition (ALD) **[2?].** The amorphous dielectric layer serves multiple purposes by passivating dangling bonds on the surface of both materials, reducing defects and interface traps, effectively bonding to both material surfaces regardless of lattice constant, and allowing charge carriers to transverse the junction without increasing the device's internal resistance.

This paper aims to demonstrate that device junctions fabricated from grafted nanomembranes perform as well as, or better, than traditional devices. Before using our grafting technique to create heterojunctions, or homojunctions of more exotic materials, we first fabricated a silicon based homojunction diode to verify that there is no decline in electrical performance, or junction interface quality, when compared to conventional devices. Silicon based devices have been extensively studied for decades, and have had numerous fabrication methods thoroughly tested, which makes them the perfect model to establish a baseline against.

Silicon-on-insulator (SOI) substrates are often the first material candidates considered for many grafting purposes due to their wide commercial availability, ability of the surface silicon layer to be highly doped with ion implantation, and ease of separating the NM from the buried oxide (BOX) layer.

**Experiment:**

The process flow for the fabrication of our Si/Si diode is depicted in **Fig. 2.** Fabrication began with a phosphorus doped host substrate made of a 500nm thick lower doped 1E16 $cm^{-3}$ n- layer on top of an 800nm thick highly doped 1E18 $cm^{-3}$ n+ layer **(Fig. 1a)**. The surface of the n-/n+ substrate is first cleaned using a 1:1 mixture of 49%HF and DI water for 10 minutes (to remove native oxide on sample surface), acetone, isopropyl alcohol (IPA), and a DI water rinse. A Savannah S200 Atomic Layer Deposition (ALD) tool by Ultratech/Cambridge Nanotech using precursors of 97.05% TMA and high-purity $H_2O$ was then used to deposit a 0.5nm thick layer of $Al_2O_3$ over 5 cycles at a temperature of 200$^{\circ}C$.

In parallel to the nSi host substrate processing, an SOI p-type donor substrate was acquired that consisted of a 180nm Si crystalline layer grown over a 400nm-thick $SiO_2$ layer on a bulk Si substrate **(Fig. 1b).** The 180 nm-thick Si layer was boron-doped at 1.64E19 $cm^{-3}$ and is referred to as a nanomembrane (NM) layer **[1].**

The NM transfer of the pSi layer to the $Al_2O_3$/nSi substrate starts with detaching the top pSi layer from the SOI wafer. This is achieved by first using a contact lithography tool to pattern a grid of small holes onto the NM surface **(Fig. 3)**. A Reactive Ion Etching (RIE) tool (Samco RIE-10NR) is then used to etch through the exposed silicon surface and reveal the SOI box layer using a 60s long process at 2Pa, flowing 67sccms of $SF_6$ and 5sccms of $O_2$, and an RF generator power of 100w. Once exposed, the SOI box layer was removed using a wet etch process wherein the sample is immersed in a 1:1 mixture of 49% HF with isopropyl alcohol (IPA) for 1 hour, followed by a rinse in DI water. During this stage, the oxide was completely etched away to release the NM and ensure an atomic-level surface smoothness for high-quality adhesion between the NM and host substrate/interface dielectric layer. The detached NM was then picked up off the donor substrate surface using a polydimethylsiloxane (PDMS) polymer stamp **(Fig. 4)** and printed, by hand, onto the host substrate. The pSi-NM/$Al_2O_3$/nSi structure was then thermally annealed using a Rapid Temperature Anneal (RTA) process at 350°C for 5 min to ensure a higher bonding strength between the pSi NM and nSi substrate.

The anode ohmic contacts were then created by using contact lithography to define the contact pattern **(Fig. 5)**, followed by the deposition of a Ni/Au/Cu (10/5/100nm bottom to top) metal stack, using electron beam evaporation and then an acetone facilitated photoresist lift-off. To create the cathode ohmic contacts, the same RIE process that was used to etch through the original pSi layer was run for 60s while using the anode metal stack as a pattern mask. After verifying that the $n^+$ layer had been reached, by measuring the surface resistance, electron beam evaporation was used to deposit a Ti/Au/Cu (10/5/100nm) metal stack, followed by a photoresist lift-off **(Fig. 5)**.

The current-voltage (*I*-*V*) characteristics of the diodes were then obtained using a Keithley 4200 semiconductor characterization system.

**(Will also need to rewrite parts of the experiment section if more devices are fabricated since the process flow will be slightly changed for optimization and the starting substrates might be different based on Donghyeok's characterization)**

## Results and Discussion:

The *I*-*V* characteristics of the grafted diodes are shown in **Fig. 6a** along with a plot of the $I_{on}/I_{off}$ ratios in **Fig. 6b**. The ratio of the absolute values of measured current flow under applied

forward bias +V compared to the current measured under reverse bias -V clearly demonstrates rectifying behavior with an $I_{on}/I_{off}$ ratio above 2E4 at 1V **(Fig. 6b).** Using the measured I-V curves, the ideality factors were calculated using the Shockley ideal diode equation

$$I = I_S\left(e^{\frac{V_D}{nV_T}} - 1\right) = I_S\left(e^{\frac{V_D}{\frac{nkT}{q}}} - 1\right) = I_S\left(\exp\left(\frac{eV}{nkT}\right) - 1\right)$$

$$n \approx \left(\frac{1}{V_T}\right)\left(\frac{V_D + dV}{l(I + dI)}\right) \approx \left(\frac{1}{V_T}\right)\left(\frac{\Delta V_D}{\ln(\Delta I)}\right)$$

where $V_t$ is the thermal voltage ($V_t = kT/q \approx 25.85mV$ at room temperature), n (or $\eta$) is the diode ideality factor, $V_d$ is the applied voltage across the device, and I/Is are respectively the output forward and reverse currents at voltage "V".

The ideality factor of this device can be calculated by taking the diode's I-V curve data in the low forward voltage region (0.1-0.5V) and calculating the instantaneous slope of the applied voltage over the natural log of the measured current (with a scale factor of one over the thermal voltage):

$$n \approx \left(\frac{1}{V_T}\right)\left(\frac{V_D + dV}{l(I + dI)}\right) \approx \left(\frac{1}{V_T}\right)\left(\frac{\Delta V_D}{\ln(\Delta I)}\right)$$

Using this method, the ideality factor of our grafted diode was calculated to be 1.05 (at a forward bias of 0.1V), which shows that the diode junction formed using this grafting method maintains excellent recombination and interface defect quality characteristics.

- **(Jiarui's wafer bonding junction paper Fig.4 says that their devices had ideality factors of 2.5 before annealing and 2.3 after. Their simulated IF is apparently 1.8 assuming a mid-gap energy GR site concentration of 5E11 cm^-2)**

**<u>CV Measurement Data Analysis</u>**

**CV measurements of a PN junction can be used to calculate:**

- **Depletion layer width "w"**
- 

**Useful equations:**

$$C_j = \frac{\varepsilon_0 \varepsilon_r A}{w}$$

**For abrupt p+n junction:**

$$w = \sqrt{\frac{2\varepsilon_0 \varepsilon_r (V_{bi} - V)}{e N_d}}$$

$$\frac{1}{C_j^2} \, vs \, V \; is \, a \, straight \, line \, with \, slope \wedge intercept \, giving \, doping \, concentration \wedge V_{bi}$$

**Useful links/references about CV measurements:**

- **https://lampx.tugraz.at/~hadley/psd/problems/capacitance/Q.php**
- **https://arxiv.org/ftp/arxiv/papers/1011/1011.3463.pdf**

Verification of the grafted junction interface was acquired using transition electron microscopy (TEM) **(Fig.XX). (still need to get these images, will probably use the new batch of devices that I'm fabricating. Either need to get trained on the NIAC SEM and use that, or send out a sample to one of our partner groups for TEM analysis)**.

The diodes tested in this study were fabricated using NMs that were 4x4mm (containing contact patterns for 33 separate devices on each NM), but the grafting technique can be applied to larger sample sizes. We have achieved 2-in full wafer Si NM transfer with very high yield (>99%) and uniformity **(Fig. 7).** The purpose of this demonstration is to show that while individual diodes were able to achieve epitaxy-like interface quality using the grafting approach, the grafting process is also scalable.

**Conclusion:**

**(Need to rewrite after adding to the main paper and finishing the Abstract)**

Fabrication results of an Si/Si diode created by grafting a p+ silicon nanomembrane onto an n-type silicon host substrate that had been coated with a 0.5nm thick amorphous layer of $Al_2O_3$ are reported and electrical testing results were calculated by measuring I-V curves using a Keithley 4200 probe. Both a high on/off current ratio above 2E4, at 1V bias, as well as a diode ideality factor of 1.05 (at 0.1V) were obtained demonstrating the excellent interface junction quality and rectifying behavior of the fabricated device. This paper presents excellent electrical performances of individual diodes made via nanomembrane grafting and demonstration of successful NM grafting up to 2-in full wafers while maintaining high yield and uniformity.

**Figures:**

**(attached in separate PowerPoint for now)**

**Acknowledgements:**

- AFRL and Atollo Engineering
    - Air Force Contract Funding Number: FA864921P0622
- UW Madison WCAM?
- Whatever tool/group ends up performing TEM measurement
- Shouldn't need to acknowledge the AFM equipment in this paper since that was only really used during the Ge/Si fabrication
- PMa? (or not if he's listed under the authors up top? or just in the author contributions section if that is included?)
- Acknowledgments/Contributions typically include:
    - Authors, non-authors (colleagues, collaborators, supervisors, etc.) and, funding sources

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**Author Contributions?:**

**(Is this necessary with so few authors or should other members of the group be added as well because they've done similar work before even if none of their data was actually used and they didn't directly contribute to the fabrication and testing of these diodes?)**

**(Part of Ma Group ARXIV Paper author contribution section for reference: "All performed the research. Z.M. conceived the idea, and designed and managed the entire research. D.L. and Z.M. developed the theoretical model and analyzed the data. J.-H.S. and Z.M. developed the generic heterostructure fabrication methods. S.J.C., J.-H.S., K.K., and Z.M. fabricated and characterized the heterostructures and devices. D.L. and Z.M. wrote the paper.")**

**References:**

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**temperature dependence so not sure if the data will be useful but could be useful just for comparing paper structures)**

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**15.** Cristea, Miron J. “Capacitance-Voltage Profiling Techniques for Characterization of Semiconductor Materials and Devices.” SSRN Electronic Journal, Nov. 2010, doi:10.2139/ssrn.3433675. **(Paper that could be useful for CV data analysis and discussion if I end up including in the paper)**

i. **Need to find and add more references before submitting paper for publication**
ii. **Should the references be organized by what topic/part of the paper they are related to or alphabetically or by some other metric?**
    - **(Suggestion I have found in a couple places is “It should be arranged in alphabetical order by the last name of the first author. If you have more than one entry by the same author, they should be further ordered by increasing publication date (more recent papers last)) (Can be easily done in word by going to “Home” “Sort” then sort by paragraph text**
iii. **Will also need to go back through paper to add reference citations once the whole thing is written**