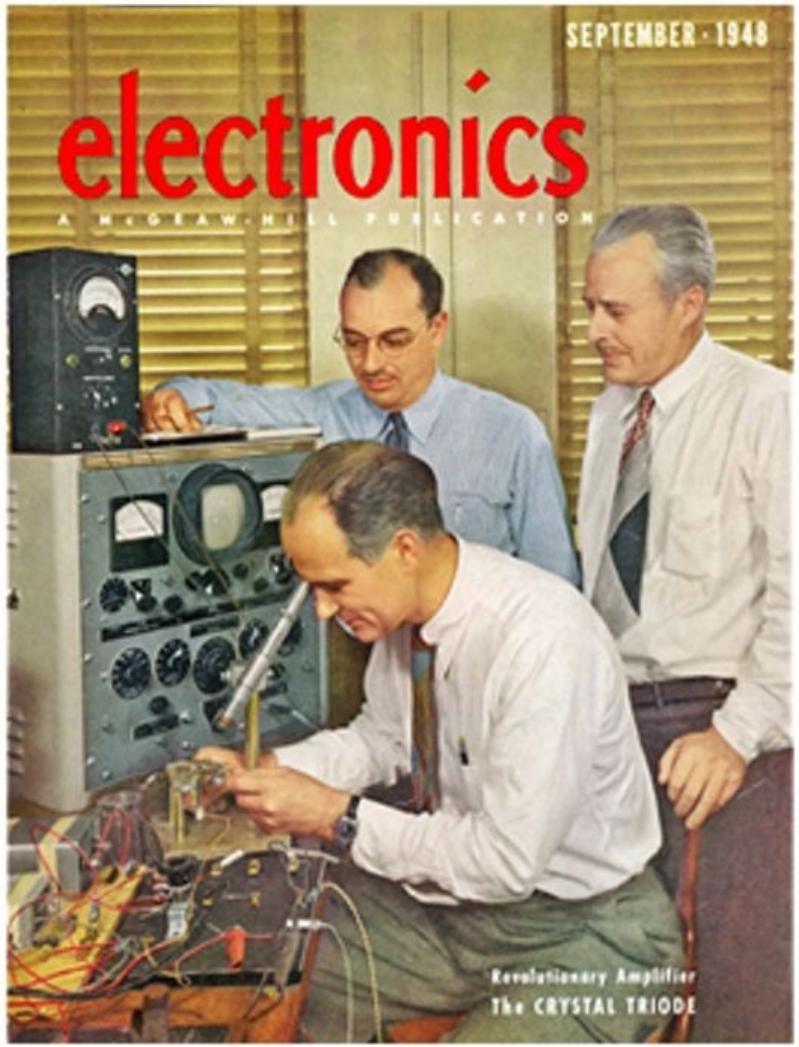
Physics of semiconductor devices – CO 4

P and N type semiconductors, carrier concentration in N and P type semiconductors, Hall effect, LDR, LED, LCD

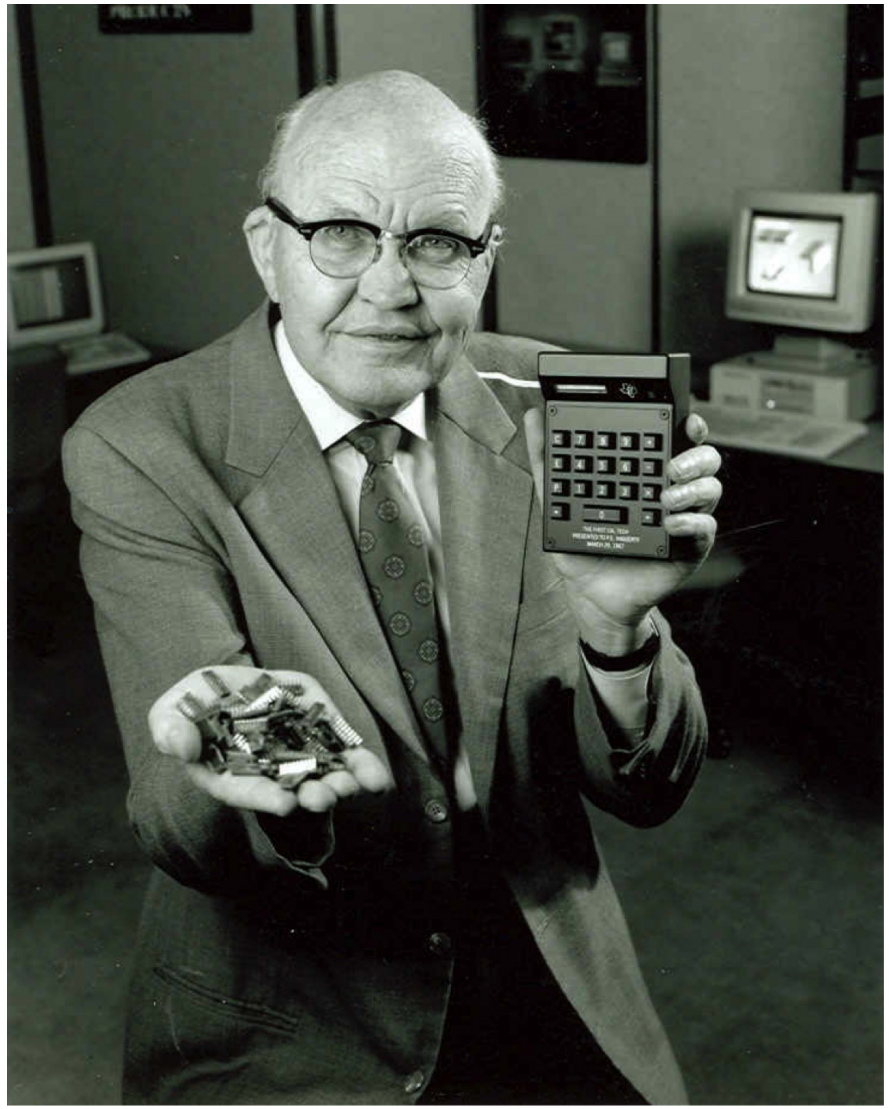


The Nobel Prize in Physics 1956

William Bradford Shockley
Prize share: 1/3

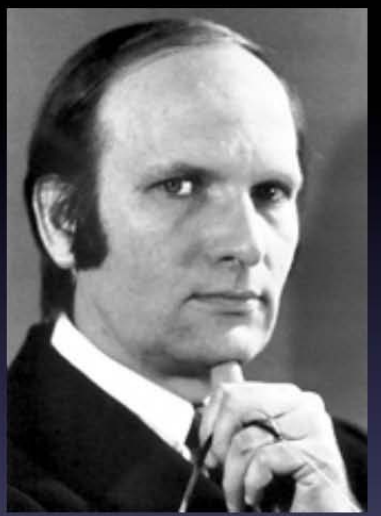
John Bardeen
Prize share: 1/3

Walter Houser Brattain
Prize share: 1/3



John Bardeen

Leon N. Cooper



John R. Schrieffer

What makes a semiconductor so important?

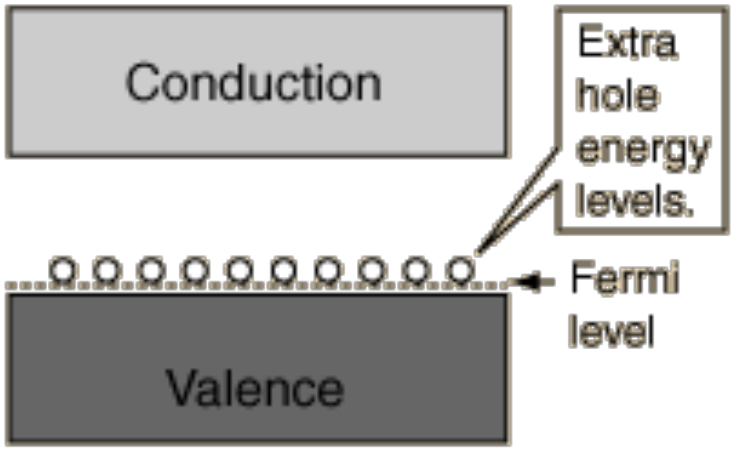
- Wide choice to alter physical properties – high to low resistivity, UV to far IR applications
- Ultra fast response times
- Multi functional devices (source, detection) and tailoring opportunity

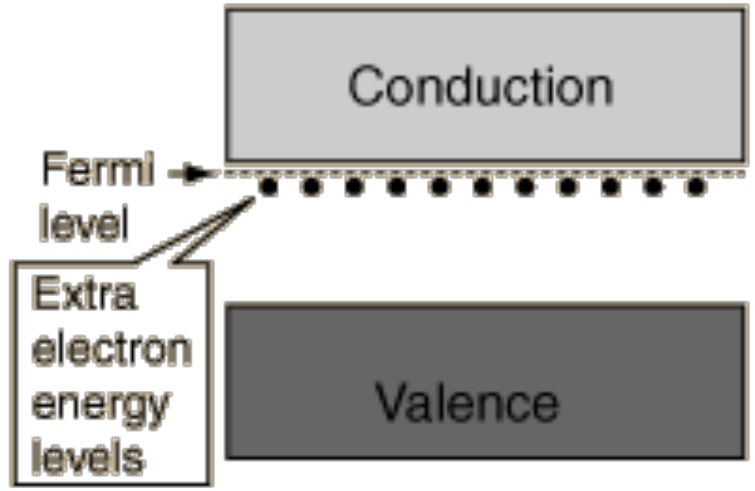
What is an intrinsic semiconductor?

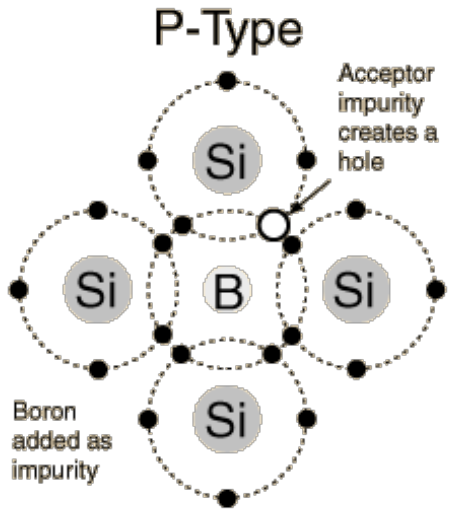
It is a semiconductor that is pristine, pure nothing has been added no impurities. It is an equilibrium if we talk about an equilibrium then an intrinsic semiconductor, the number of electrons and number of holes has to be exactly same.

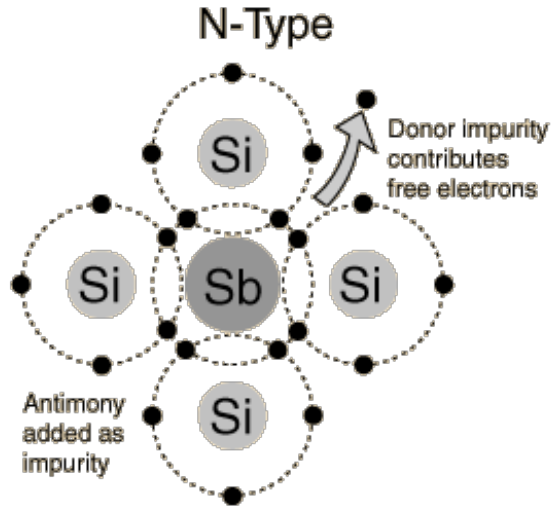
N-type (extrinsic) – addition of pentavalent impurities such as Sb, As or P contributes free electrons, increasing the conductivity of intrinsic semiconductors. Phosphorous is added by diffusing Phosphine gas

P-type (intrinsic) – addition of trivalent impurities such as Boron, Al or Ga creates holes increasing the conductivity of intrinsic semiconductors.

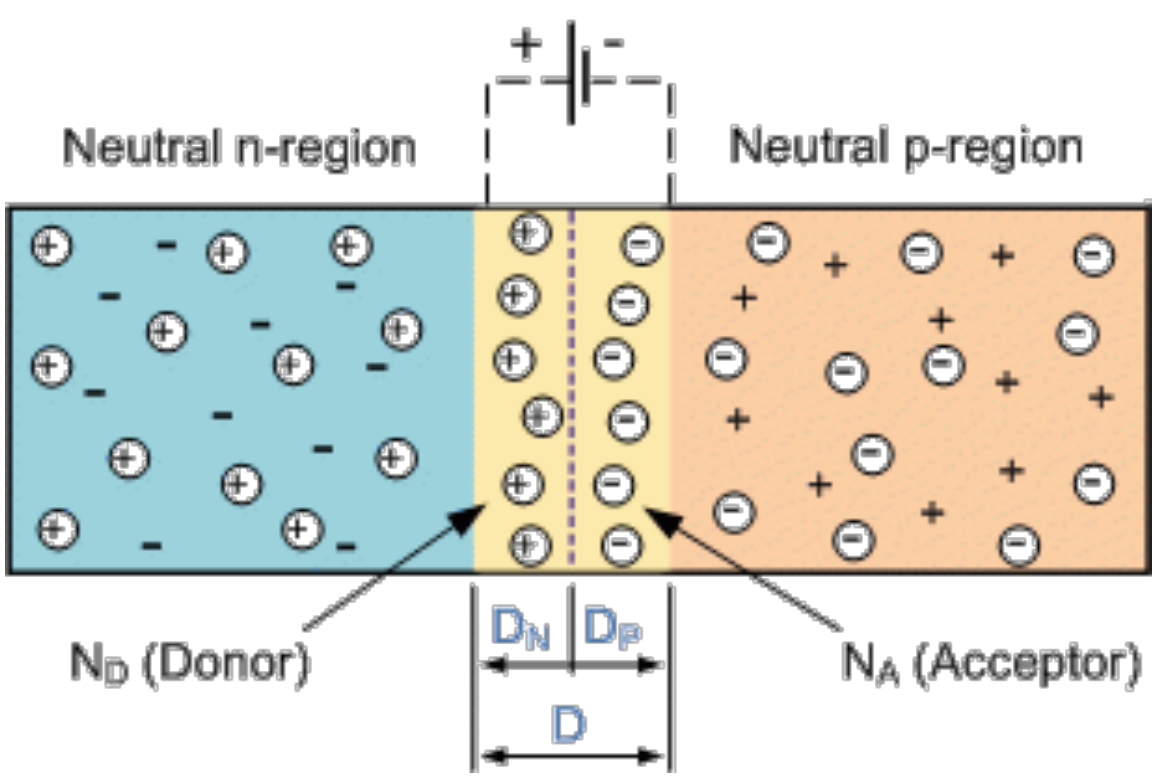

Conduction
Extra hole energy levels.
Fermi level
Valence

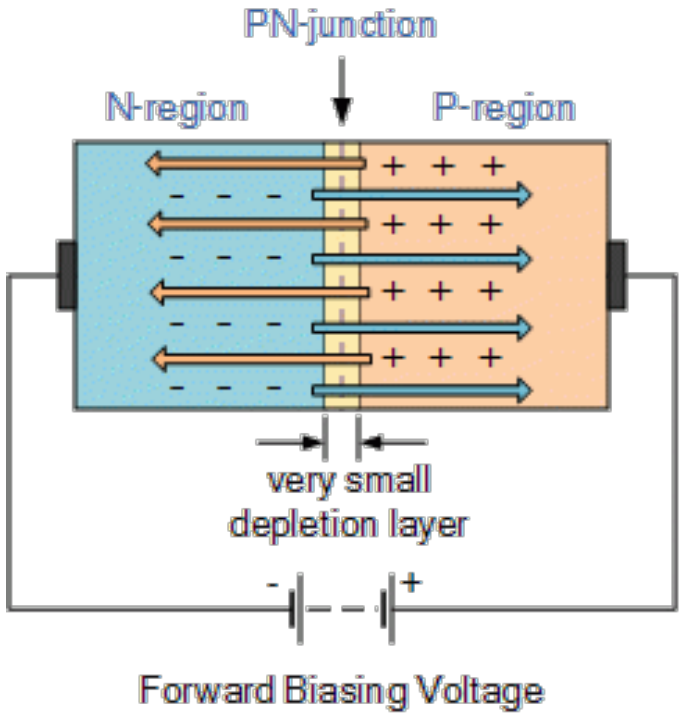

Conduction
Fermi level
Extra electron energy levels
Valence


P-Type
Acceptor impurity creates a hole
Si
Si
B
Si
Si
Boron added as impurity

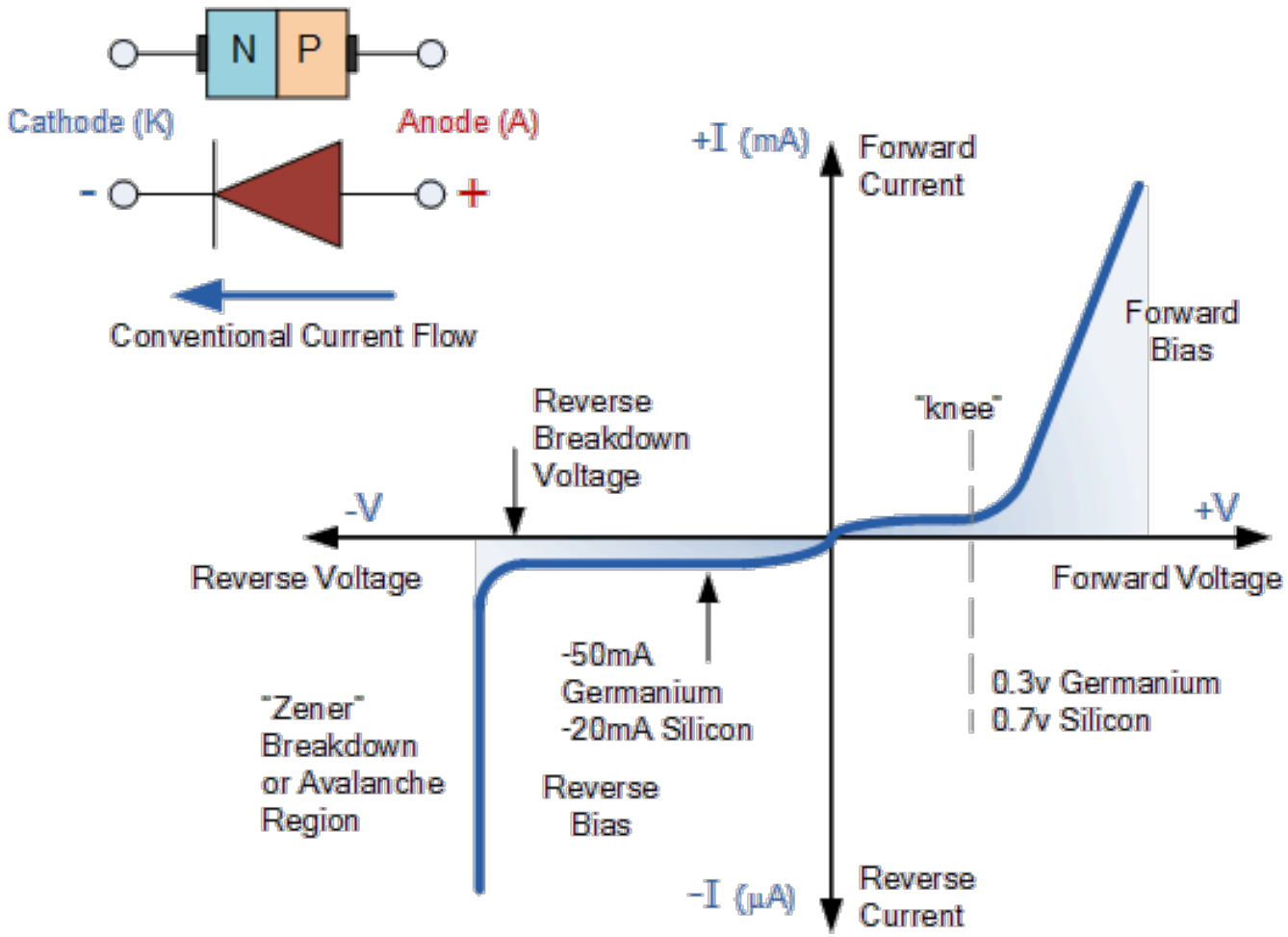

N-Type
Donor impurity contributes free electrons
Si
Si
Sb
Si
Si
Antimony added as impurity

A pn junction is formed when p type material is fused into n type material creating a semiconductor diode





- When n and p type semiconductors are first joined together a very large density gradient exists between the both sides of the junction. The result is some of the free electrons from the donor impurity atoms being to migrate across the newly formed junction to fill the holes in the p-type producing negative ions.
- Now diffusion of carriers takes place. Electrons leave positively charged donor ions in the n-type region and holes leave negatively charged acceptor ions in the p-type region
- Eventually a state of equilibrium occurs preventing further migration creating a potential barrier
- This region is now depleted of free carriers and hence called depletion region


N
P
Cathode (K)
Anode (A)
-
+
Conventional Current Flow
+I (mA)
Forward
Current
Forward
Bias
"knee"
Reverse
Breakdown
Voltage
-V
+V
Reverse Voltage
Forward Voltage
-50mA
Germanium
-20mA Silicon
0.3v Germanium
0.7v Silicon
"Zener"
Breakdown
or Avalanche
Region
Reverse
Bias
-I (µA)
Reverse
Current

Elemental and compound semiconductors

- Si – 1.1 eV
- Ge – 0.69 eV
- GaAs – 1.4 eV
- CdTe – 1.5 eV
- PbS
- $CuInSe_2$
- $CuInGaSe_2$

In direct band gap

Direct band gap

How do you classify semiconductors

Resistivity

1. Intrinsic and extrinsic semiconductors

Band gap

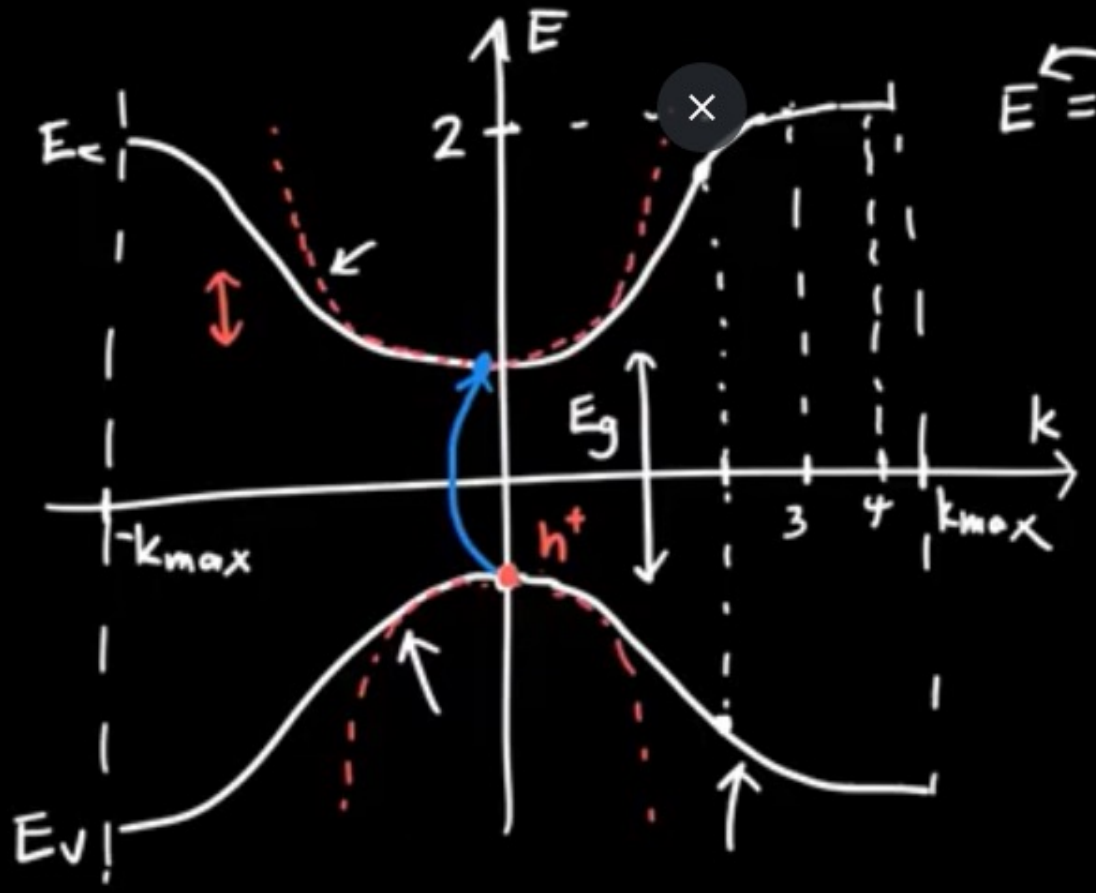
1. Direct band gap and indirect band gap

Composition

1. Elemental 2. compound semiconductors

Doping

1. n-type 2. p-type semiconductor



$E = \frac{p^2}{2m}$

$m = \frac{p^2}{2E} = \frac{\hbar^2 k^2}{2E}$

$m = \frac{\hbar^2 9}{2 \cdot 2}$

$m = \hbar^2 \frac{9}{4}$

$m = \hbar^2 \frac{16}{4}$

m_e = negative

$E = \frac{\hbar^2 k^2}{2m}$

$\frac{\partial E}{\partial k} = \frac{2\hbar^2 k}{2m}$

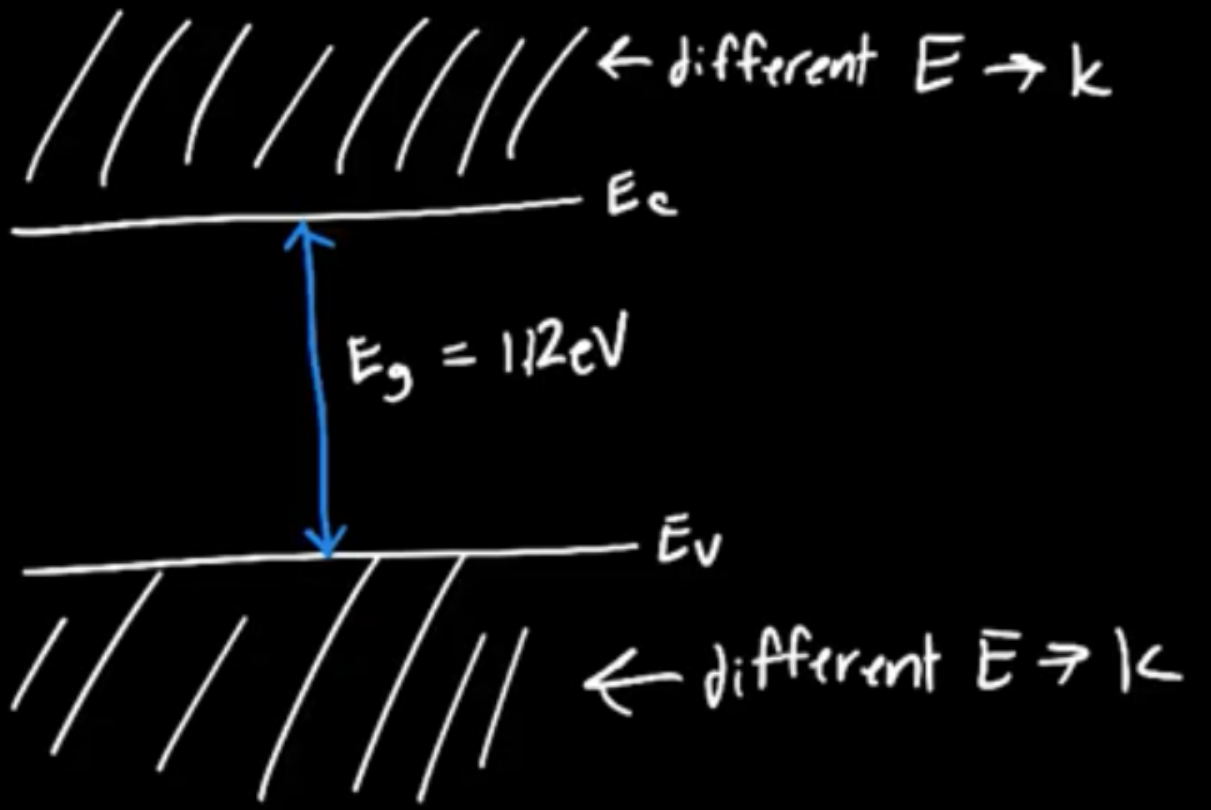
$\frac{\partial^2 E}{\partial k} = \frac{\hbar^2}{m}$

can be evaluated
for any E/k diagram

$$m^* = \frac{\hbar^2}{\left(\frac{\partial^2 E}{\partial k^2}\right)}$$

m^*: effective mass

m_e m_h $m_e^* \approx 0.82\, m_e$



EFFECTIVE MASS OF e^- (m_e^*)

$F = m_e^* a$ — ①

GROUP VELOCITY

$v_g = \frac{d\omega}{dk}$ $\left[\because \omega = 2\pi\nu,\ E = h\nu,\ \omega = 2\pi \cdot \frac{E}{h},\ \omega = \frac{E}{\hbar}\right]$

$v_g = \frac{d}{dk}\left(\frac{E}{\hbar}\right)$

$\boxed{v_g = \frac{1}{\hbar}\frac{dE}{dk}}$ — ① $\left(\frac{2\pi}{h} = \hbar\right)$

Diff eqn ① w.r.t 't'

$a = \frac{d}{dt}(v_g) = \frac{d}{dt}\left(\frac{1}{\hbar}\frac{dE}{dk}\right)$

$a = \frac{1}{\hbar}\frac{d}{dt}\left(\frac{dE}{dk}\right)$

$a = \frac{1}{\hbar}\frac{d}{dk}\left(\frac{dE}{dt}\right) = \frac{1}{\hbar}\frac{d}{dk}\left(\frac{dE}{dk}\cdot\frac{dk}{dt}\right)$ — ②

W.K.T $\lambda = \frac{h}{p}$

$\because k = \frac{2\pi}{\lambda}$ ⇒ WAVE VECTOR

$\frac{2\pi}{k} = \frac{h}{p} \Rightarrow p = \frac{h}{2\pi}k$

$\boxed{p = \hbar k}$

Diff above eqn w.r.t 't'

$\frac{dp}{dt} = \frac{d}{dt}(\hbar k)$

$F = \hbar\frac{dk}{dt}$

$\Rightarrow \boxed{\frac{dk}{dt} = \frac{F}{\hbar}}$ — ③

$\frac{d}{dt}p = \frac{d}{dt}mv = m\frac{dv}{dt} = m.a = F$

Sub ③ in ②

$a = \frac{1}{\hbar}\frac{d}{dk}\left(\frac{dE}{dk}\cdot\frac{F}{\hbar}\right)$

$\boxed{a = \frac{F}{\hbar^2}\frac{d^2E}{dk^2}}$

$F = \left[\frac{\hbar^2}{\left(\frac{d^2E}{dk^2}\right)}\right]a$ — ⑤

$\boxed{m_e^* = \frac{\hbar^2}{(d^2E/dk^2)}}$

UPTO INFLECTION Pt k_0

$v \Rightarrow a = \Rightarrow \frac{d^2E}{dk^2} =$

$\Rightarrow m_e^* =$

AT INFLECTION Pt

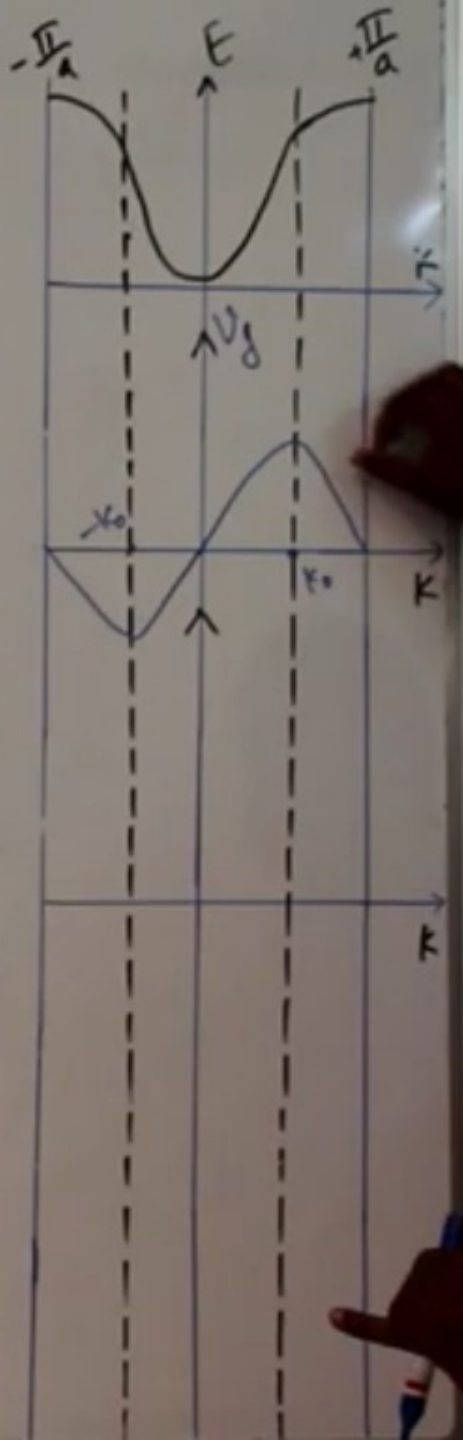
$v = \Rightarrow a =$

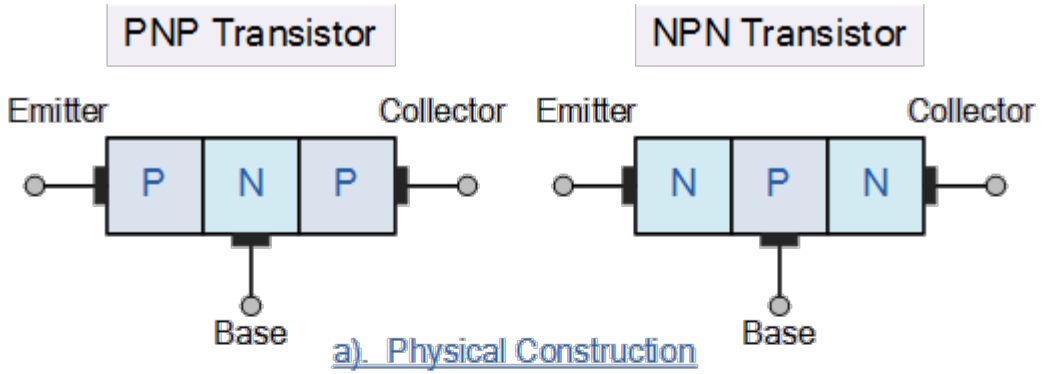
$\Rightarrow m_e^* =$

BEYOND INFLECTION Pt

$v \Rightarrow a = \Rightarrow \frac{d^2E}{dk^2} =$

$\Rightarrow m_e^* =$

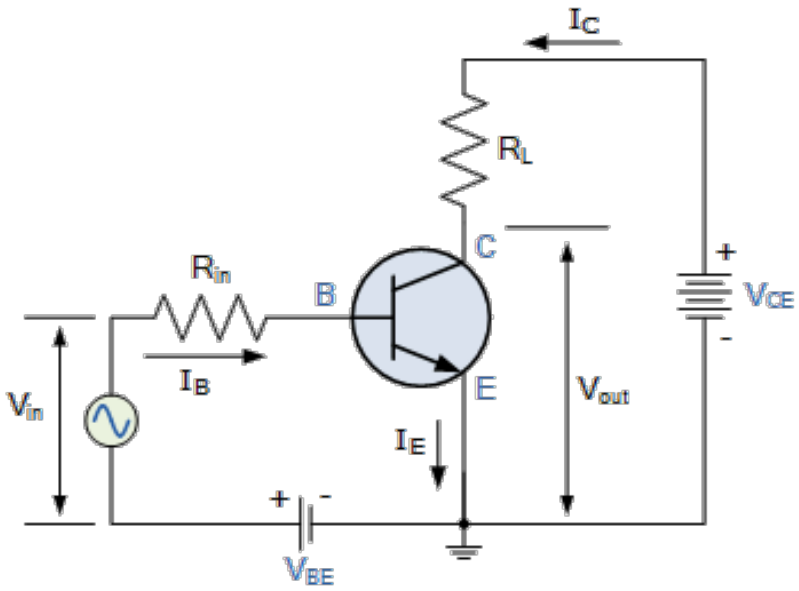




Bipolar Transistor Configurations

As the Bipolar Transistor is a three terminal device, there are basically three possible ways to connect it within an electronic circuit with one terminal being common to both the input and output. Each method of connection responding differently to its input signal within a circuit as the static characteristics of the transistor vary with each circuit arrangement.

Common Base Configuration – has Voltage Gain but no Current Gain.
Common Emitter Configuration – has both Current and Voltage Gain.
Common Collector Configuration – has Current Gain but no Voltage Gain.



$$\text{Alpha},(\alpha) = \frac{I_C}{I_E} \quad \text{and} \quad \text{Beta},(\beta) = \frac{I_C}{I_B}$$

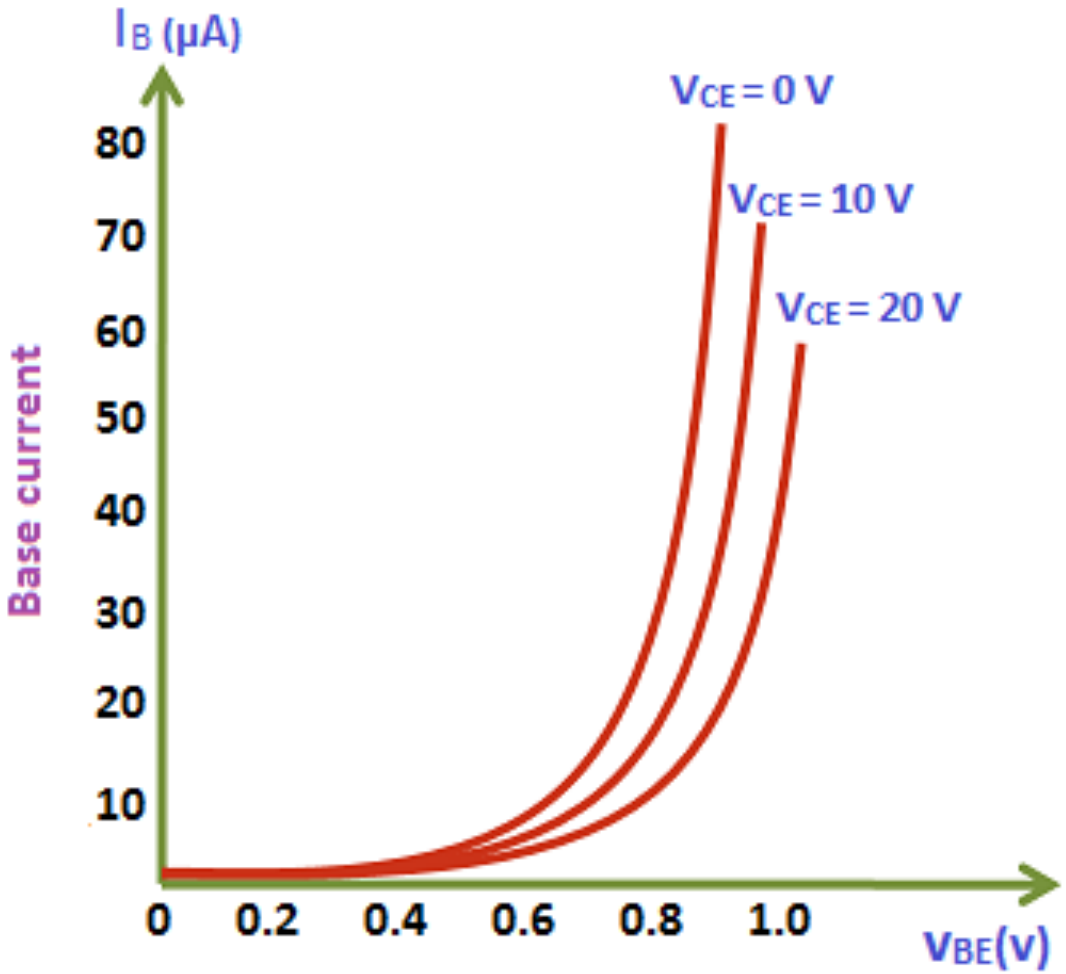
$$\therefore I_C = \alpha.I_E = \beta.I_B$$

$$\text{as: } \alpha = \frac{\beta}{\beta + 1} \qquad \beta = \frac{\alpha}{1 - \alpha}$$

The Common Emitter (CE) Configuration

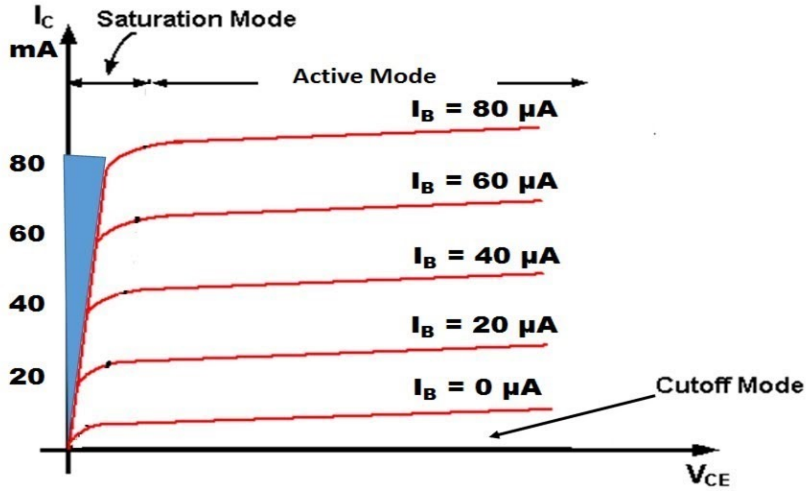
- In the Common Emitter or grounded emitter configuration, the input signal is applied between the base and the emitter, while the output is taken from between the collector and the emitter as shown. This type of configuration is the most commonly used circuit for transistor based amplifiers and which represents the “normal” method of bipolar transistor connection.

- The common emitter amplifier configuration produces the highest current and power gain of all the three bipolar transistor configurations. This is mainly because the input impedance is LOW as it is connected to a forward biased PN-junction, while the output impedance is HIGH as it is taken from a reverse biased PN-junction.



I/P characteristics CE configuration

Common emitter Output characteristics



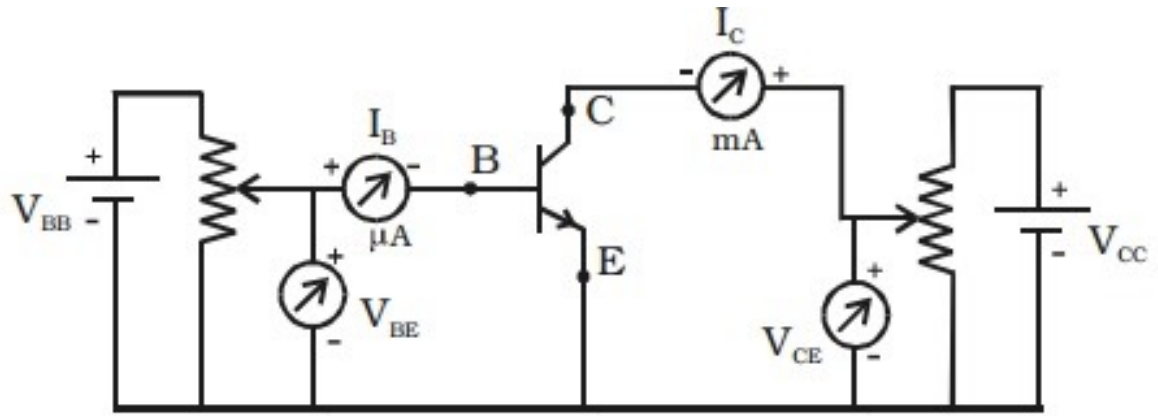


Fig Transistor circuit in CE mode.

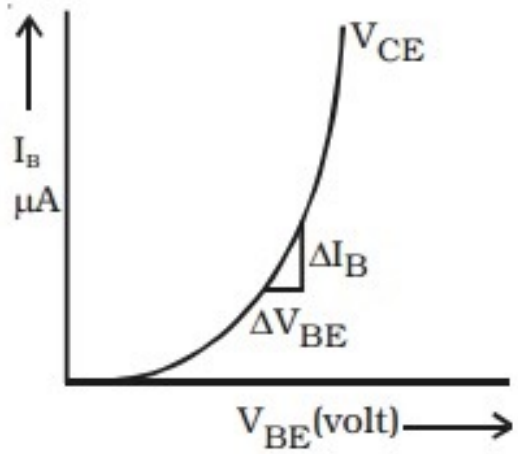


Fig Input characteristics

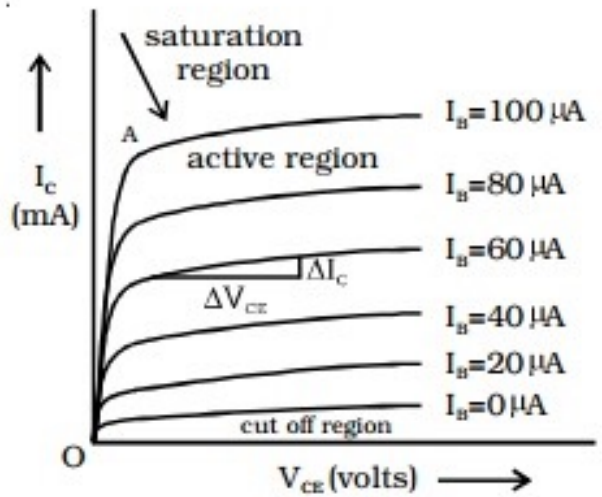


Fig Output characteristics

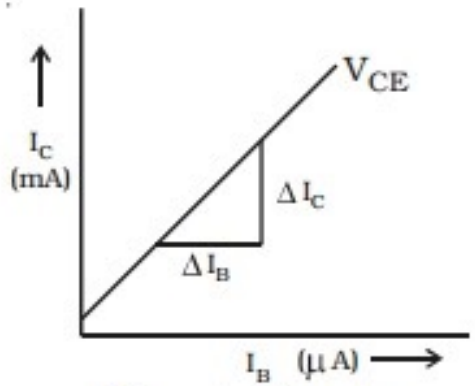


Fig Transfer characteristic curve

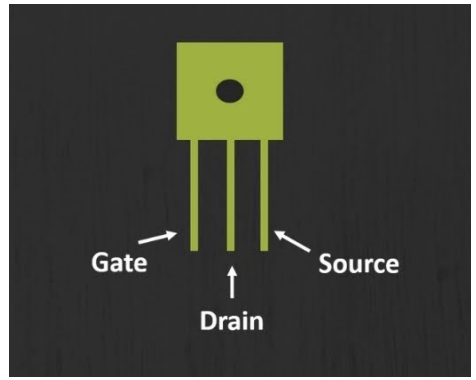
FET

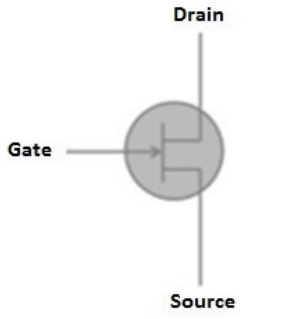
- A Field Effect Transistor (FET) is a three-terminal semiconductor device. Its operation is based on a controlled input voltage. By appearance JFET and bipolar transistors are very similar. However, BJT is a current controlled device and JFET is controlled by input voltage. Most commonly two types of FETs are available.
- Junction Field Effect Transistor (JFET)
- Metal Oxide Semiconductor FET (IGFET)

JFET

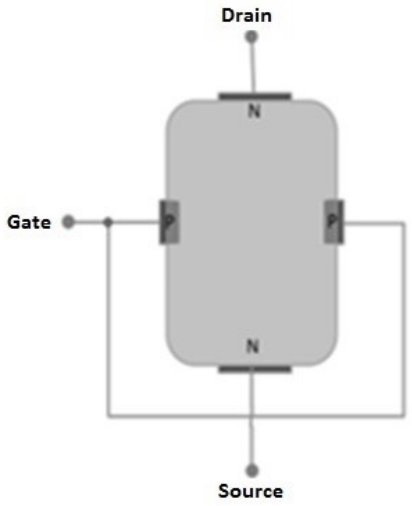
- The functioning of Junction Field Effect Transistor depends upon the flow of majority carriers (electrons or holes) only. Basically, JFETs consist of an **N** type or **P** type silicon bar containing PN junctions at the sides. Following are some important points to remember about FET −
- **Gate** − By using diffusion or alloying technique, both sides of N type bar are heavily doped to create PN junction. These doped regions are called gate (G).
- **Source** − It is the entry point for majority carriers through which they enter into the semiconductor bar.
- **Drain** − It is the exit point for majority carriers through which they leave the semiconductor bar.
- **Channel** − It is the area of N type material through which majority carriers pass from the source to drain.
- There are two types of JFETs commonly used in the field semiconductor devices: **N-Channel JFET** and **P-Channel JFET**.

N channel and P channel FET

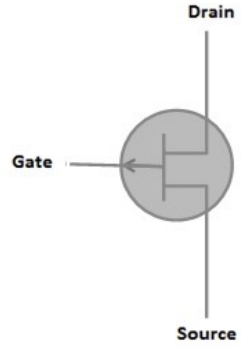




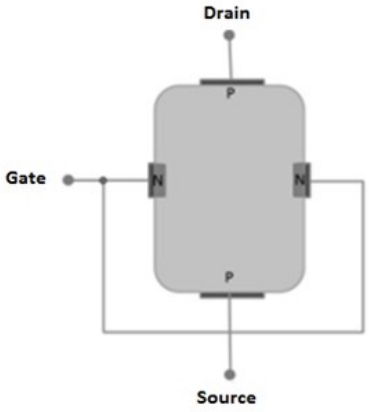
Symbol of N-Channel JFET



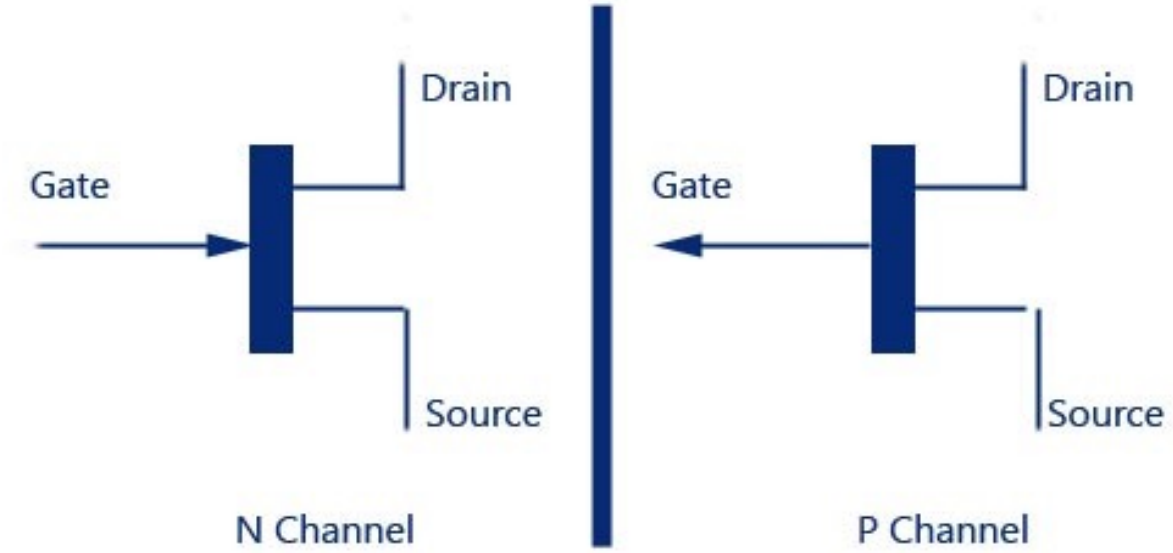
N-Channel JFET



Symbol of P-Channel JFET



P-Channel JFET

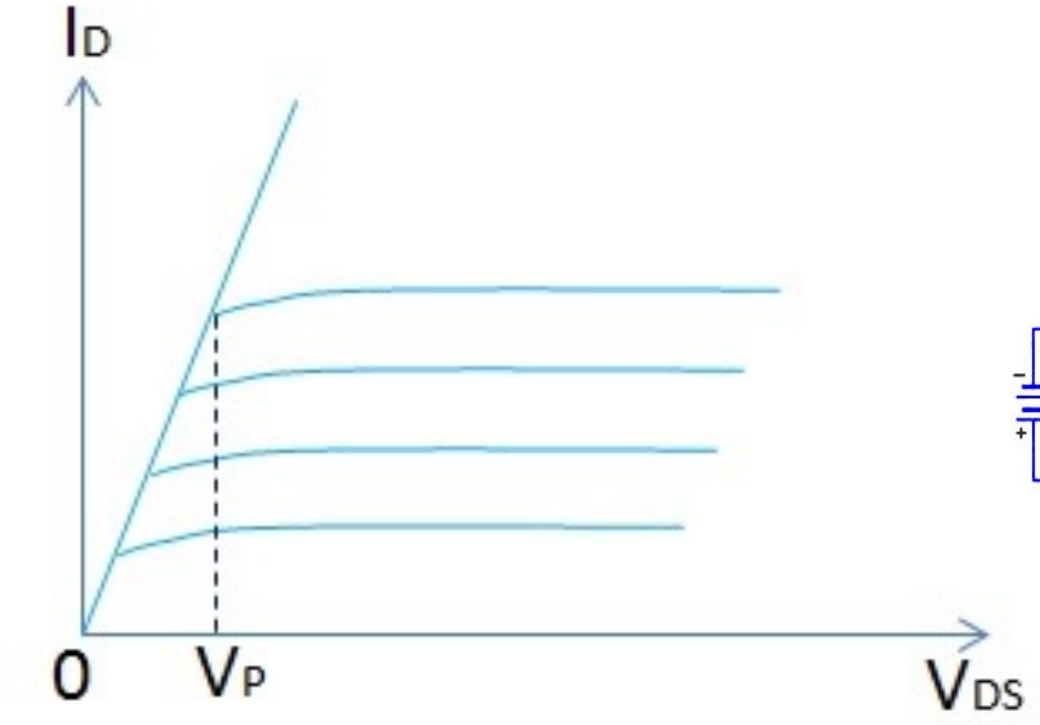


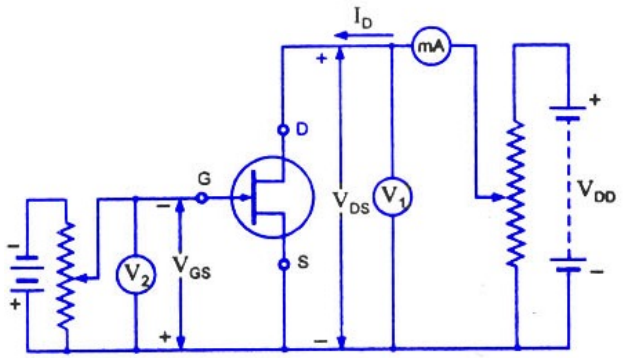
FET

Field Effect Transistor FET

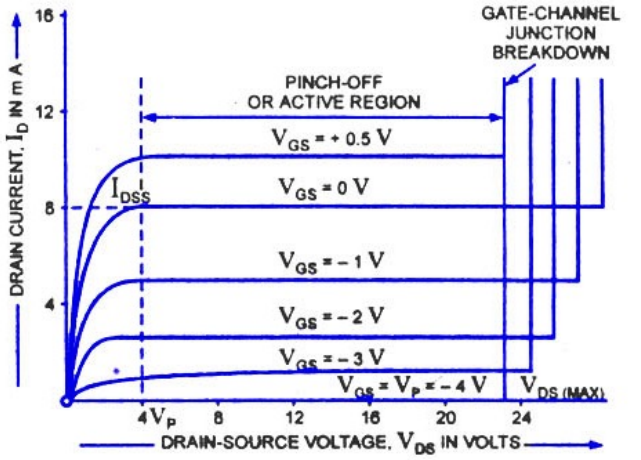
Output characteristics of FET

- Initially, the drain current (ID) rises rapidly with drain source voltage (VDS) however suddenly becomes constant at a voltage known as pinch-off voltage (VP). Above pinch-off voltage, the channel width becomes so narrow that it allows very small drain current to pass through it. Therefore, drain current (ID) remains constant above pinch-off voltage





Circuit Diagram For Determining Drain Characteristic With External Bias For An N-Channel JFET



JFET Drain-Characteristics With External Bias

JFET parameters

- **AC drain resistance (R_d)** − It is the ratio of change in the drain source voltage (ΔV_{DS}) to the change in drain current (ΔI_D) at constant gate-source voltage. It can be expressed as,

- $R_d = (\Delta V_{DS})/(\Delta I_D)$ at Constant V_{GS}

- **Transconductance (g_{fs})** − It is the ratio of change in drain current (ΔI_D) to the change in gate source voltage (ΔV_{GS}) at constant drain-source voltage. It can be expressed as,

- gfs = $(\Delta I_D)/(\Delta V_{GS})$ at constant V_{DS}

- **Amplification Factor (u)** − It is the ratio of change in drain-source voltage (ΔVDS) to the change in gate source voltage (ΔV_{GS}) constant drain current (ΔI_D). It can be expressed as,

- u = $(\Delta V_{DS})/(\Delta V_{GS})$ at constant I_D

Integrated circuits

- RTL logic
- DTL logic
- TTL logic
- CMOS logic (VLSI, SVLSI)
- Logic gate IC’s
- Timer IC’s
- Op amp
- Voltage regulators