

# SUGASHINI T

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📁 PORTFOLIO : <https://sugathiyagu.github.io/CV/>



## PROFILE

Passionate about developing innovative solutions to enhance systems and processes. With a strong foundation in programming and design, I aim to contribute to your team and support the company's growth while continuously learning and exploring new technologies

## EDUCATION

<b>ME – VLSI Design</b> , K. Ramakrishnan College of Technology Anna university , CGPA : 9.57	2021 – 2023 India
<b>BE – ELECTRONICS &amp; COMMUNICATION</b> , K. Ramakrishnan College of Engineering Anna university , CGPA : 8.41	2016 – 2020 India
<b>HSC- State Board</b> , Brindavan Higher Secondary School Percentage : 88%	2015 – 2016 India

## SKILLS

Languages	Databases	Frameworks	Tools and Software
<ul style="list-style-type: none"><li>• C</li><li>• CSS3</li><li>• HTML5</li><li>• VERILOG</li><li>• JAVASCRIPT</li><li>• SYSTEM VERILOG</li></ul>	<ul style="list-style-type: none"><li>• SQL</li><li>• MYSQL</li><li>• MONGODB</li></ul>	<ul style="list-style-type: none"><li>• BOOTSTRAP</li></ul>	<ul style="list-style-type: none"><li>• XILINX</li><li>• TANNER</li><li>• MS OFFICE</li><li>• MICROWIND</li><li>• VISUAL STUDIO</li></ul>

## PROJECTS

<b>IMPLEMENTATION OF AREA EFFICIENT APPROXIMATE KARATSUBA USING WALLACE TREE MULTIPLIER.</b>	2023
<ul style="list-style-type: none"><li>• Designed Wallace tree multiplier using XOR gate and carry-in prediction techniques to reduce area, power and delay.</li></ul>	
<b>IRIS RECOGNITION USING DCNN.</b>	2020
<ul style="list-style-type: none"><li>• Developed a DCNN algorithm for semantic segmentation to determine time interval and identify matching iris samples, useful in forensic analysis.</li></ul>	

## INTERNSHIP

**Embedded system Intern**, Pantech Protech Ltd | 2020.

- Gained hands-on experience in developing embedded system and applications.

## ACHIVEMENTS

- Secured third place as the class topper in the fifth semester | 2018-2019.
- Achieved 69%(ELITE) for the course "System design through Verilog" in NPTEL | 2022.

## AREA OF INTEREST

- RTL Code.
- ASIC Design.
- Digital IC Design.
- Digital Electronics.
- Front End Developer.

## CERTIFICATES

- Workshop on Intel FPGA for Embedded, AI/ML and heterogeneous application | 2023.
- Workshop on FPGA Design Using Xilinx, Vivado and Mentor Graphics | 2023.
- Diploma in PHP Full Stack Developer | 2023.
- Course completion in C, C++, PYTHON programming | 2021.
- Mini project contest "EINSTACTOMIA" | 2019
- Three day Workshop on Robotics using Arduino | 2018.

## CAPABILITIES

- Skilled in managing demanding workloads and deadlines.
- Collaborative team player.
- Eagerness to learn new things.

## LANGUAGES

- English
- Tamil

## DECLARATION

I hereby declare that the above mention details about me are true to the best of my knowledge and belief.

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