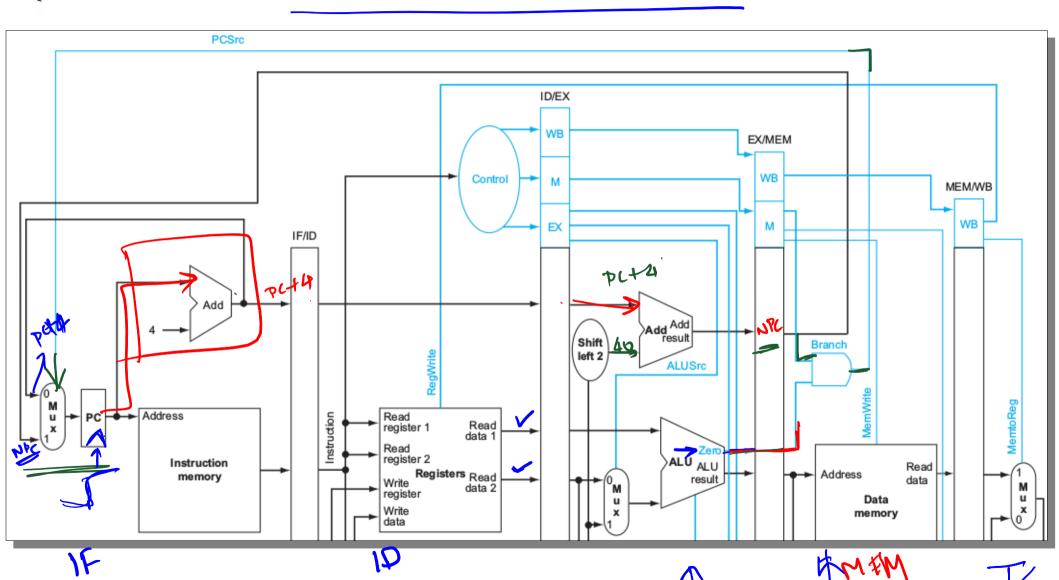
### **Outline**

- Pipeline, Pipelined datapath
- Dependences, Hazards
  - Structural, Data Stalling, Forwarding
- Control Hazards
- Branch prediction

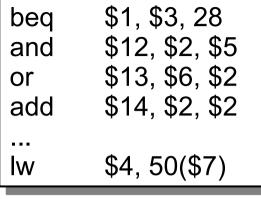
 Arise from the pipelining of branches and other instructions that change the PC

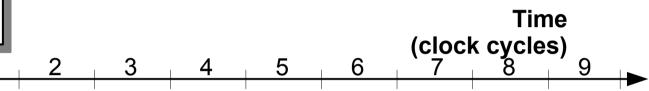
- Arise from the pipelining of branches and other instructions that change the PC
- Also called Branch Hazards

beg \$1,\$2,000 Branch Evaluation

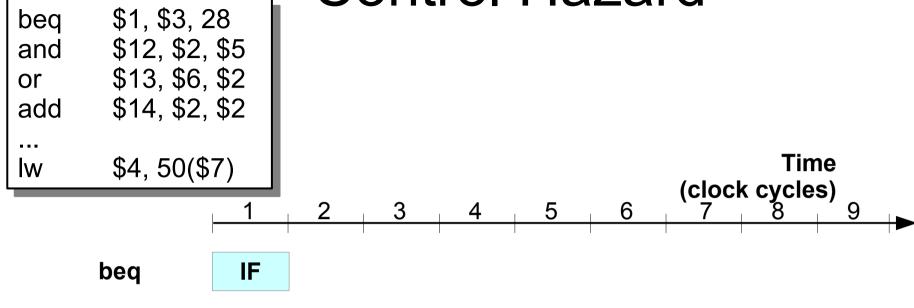


```
beq $1, $3, 28
and $12, $2, $5
or $13, $6, $2
add $14, $2, $2
...
lw $4, 50($7)
```





beq

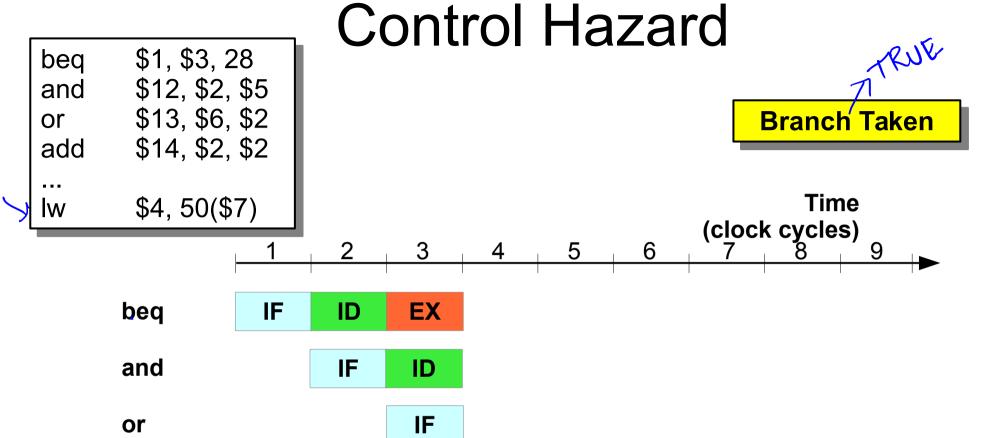


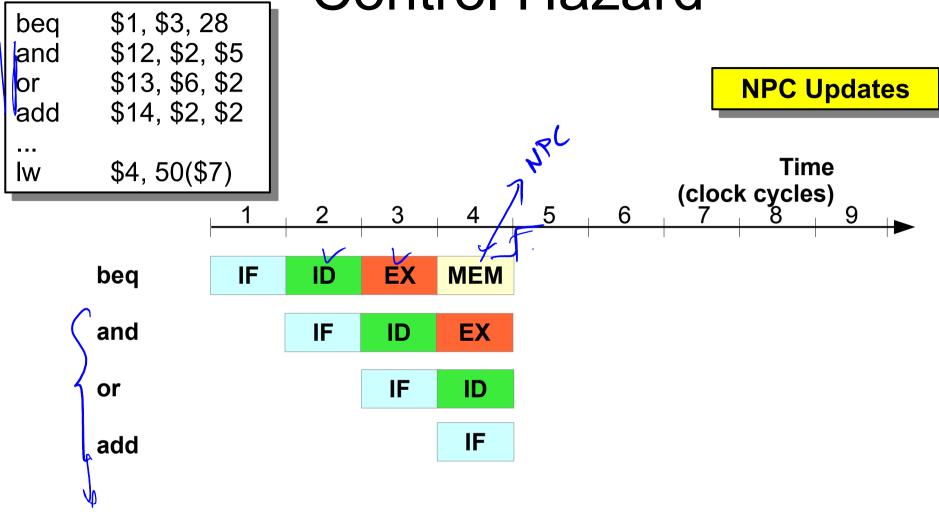
and

**Control Hazard** \$1, \$3, 28 beq \$12, \$2, \$5 and \$13, \$6, \$2 or \$14, \$2, \$2 add **Time** \$4, 50(\$7) lw (clock cycles) 5 4 6 9 IF beg. ID EX and IF ID

IF

or





EX

ID

IF

**Insert NOP** 

ID

IF

\$1, \$3, 28 beq \$12, \$2, \$5 and \$13, \$6, \$2 or \$14, \$2, \$2 add \$4, 50(\$7) lw 5 6 **MEM** IF EX ID beq

IF

and

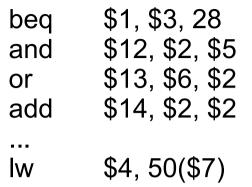
or

add

Time (clock cycles) 7 8 9

**NPC Updates** 





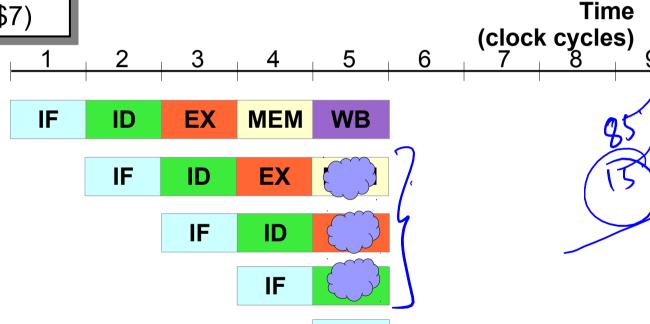
beq

and

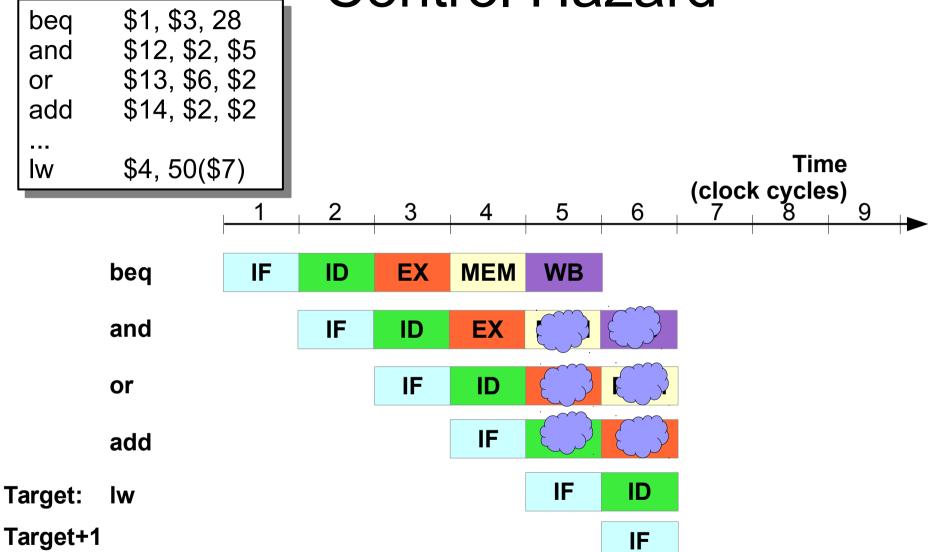
or

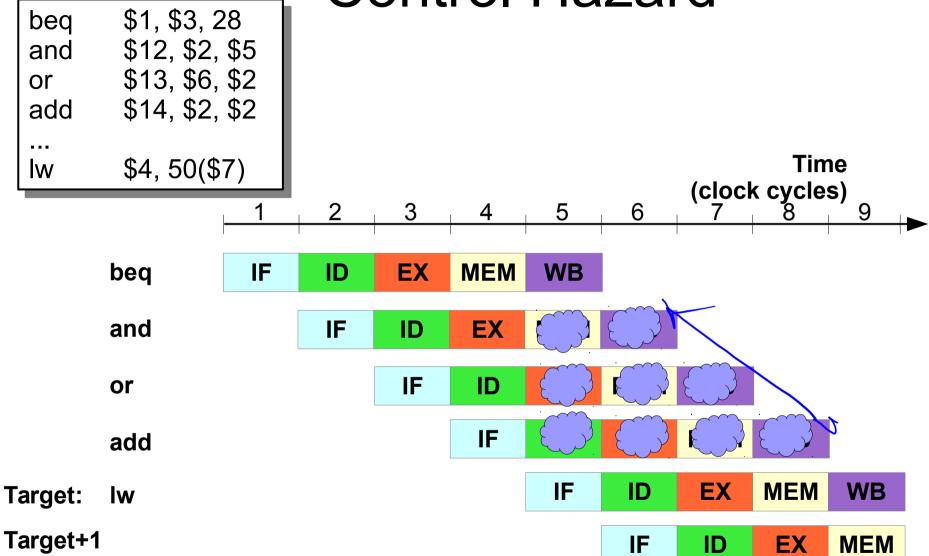
add

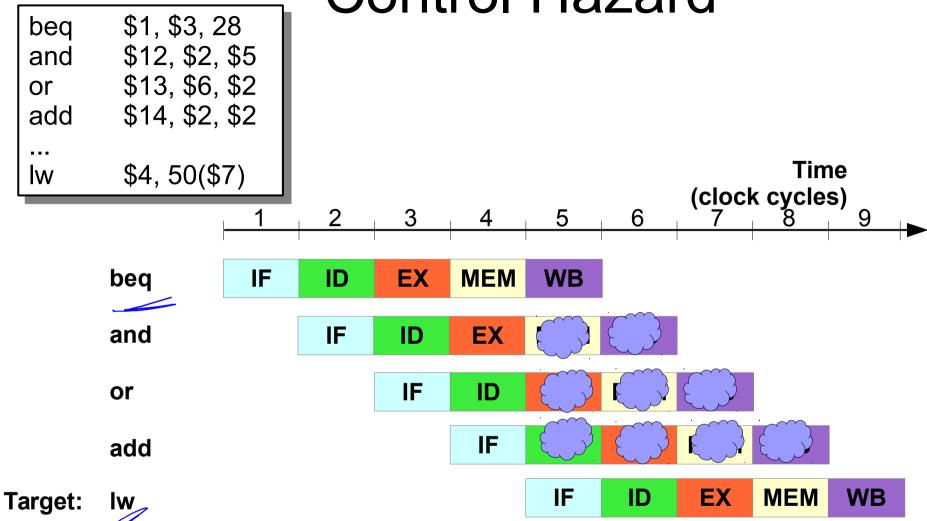
Branch target enters the pipeline



IF



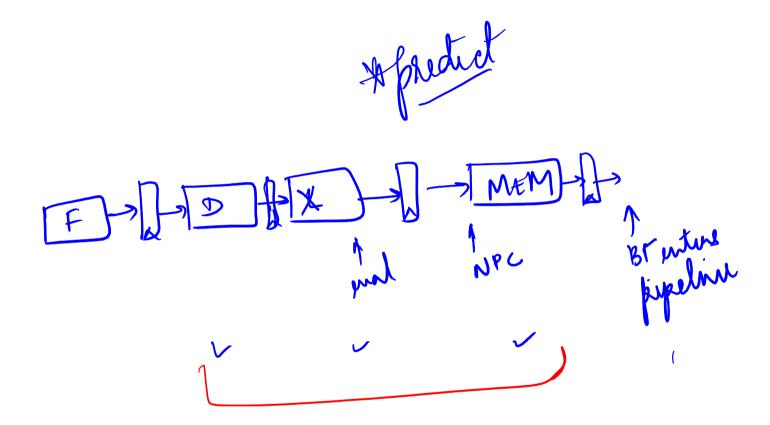




**Branch Penalty = 3 cycles** 

- Branch evaluation occurs in EX stage.
- PC updates in MEM stage.
- Branch target loads in the next cycle
- The delay in determining the proper instruction to fetch is called a Control Hazard or Branch Hazard.

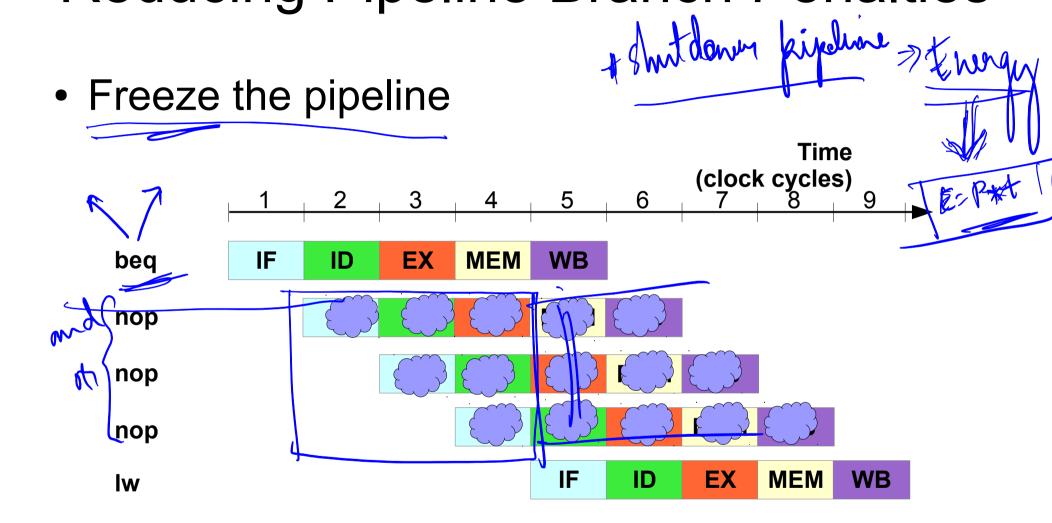
# Reducing Pipeline Branch Penalties



# Reducing Pipeline Branch Penalties

Freeze the pipeline

Reducing Pipeline Branch Penalties



\* branch penalty = 3 cycles

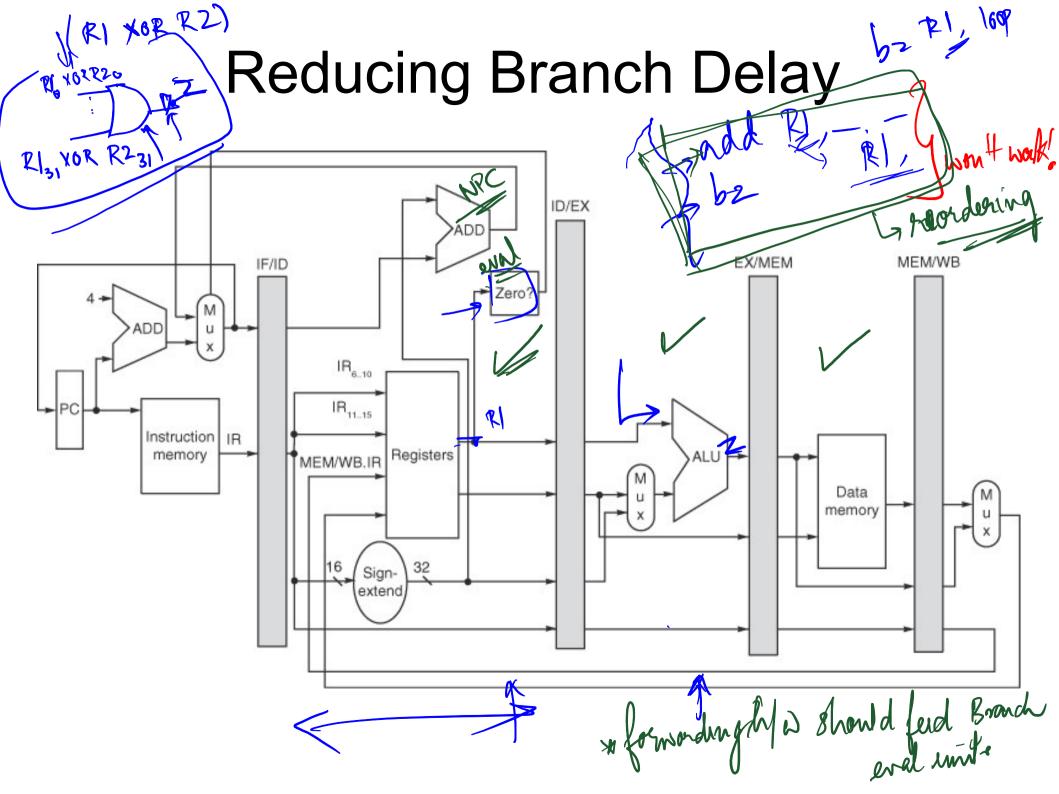


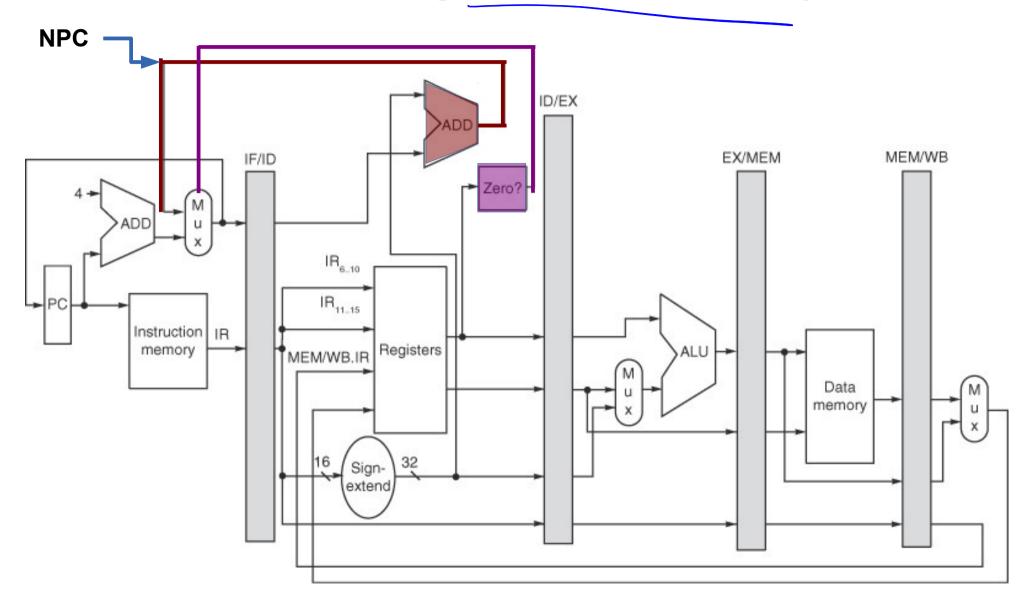
- Most branches rely on simple tests (equality or sign)
- Move the branch decision up

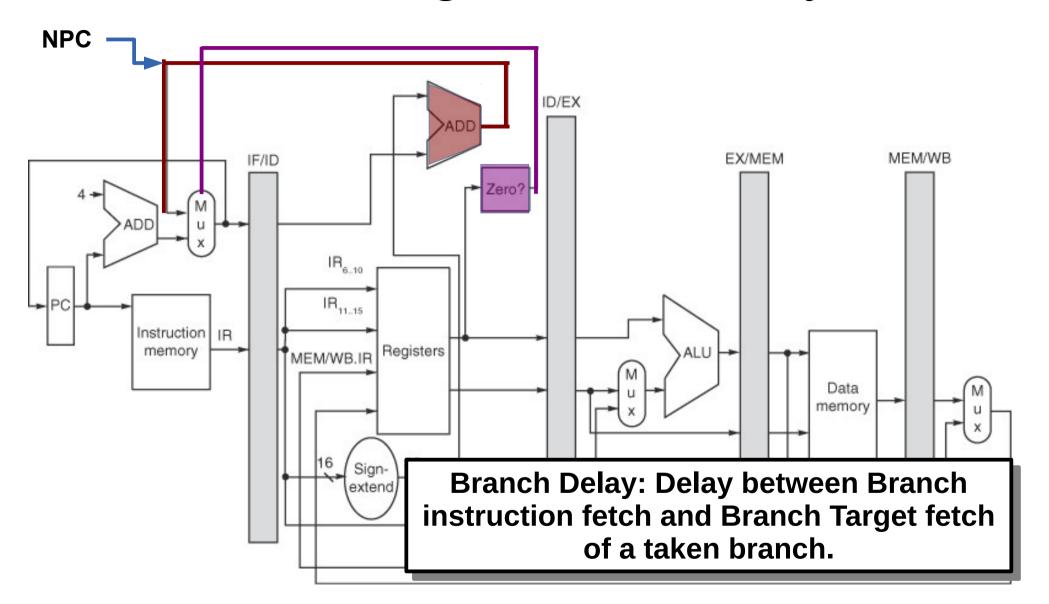
- Most branches rely on simple tests (equality or sign)
- Move the branch decision up

  - Compute NPC earlier

    Evaluate branch at the earliest

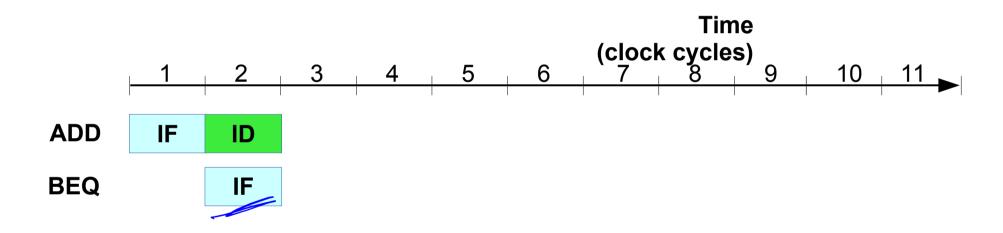






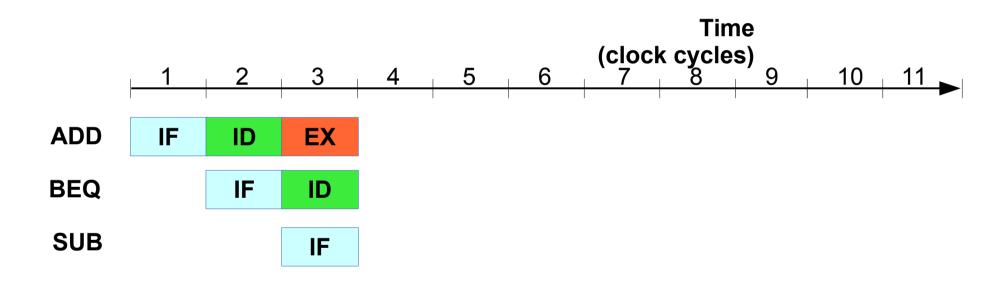
```
ADD R2, R3,R4
BEQ R2, R4, loop
SUB R5, R5,R4
```

---



```
ADD R2, R3,R4
BEQ R2, R4, loop
SUB R5, R5,R4
```

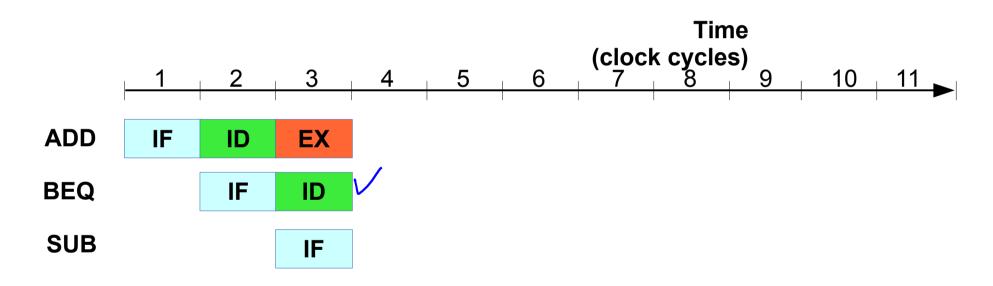
---



```
ADD R2, R3,R4
BEQ R2, R4, loop
```

SUB R5, R5, R4

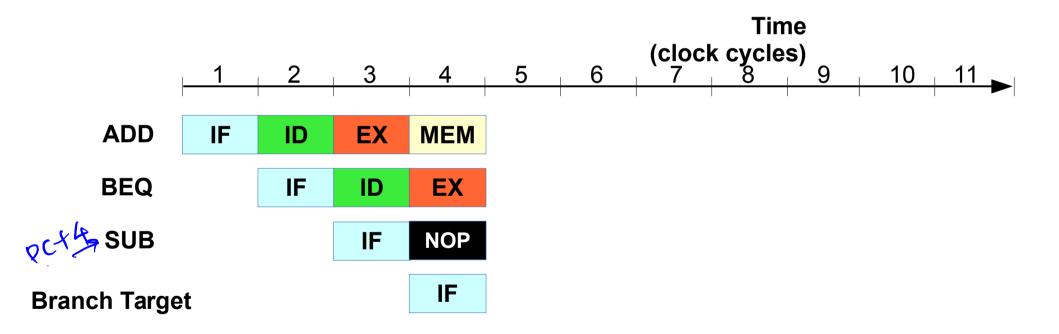
---



PC = PC + Offset

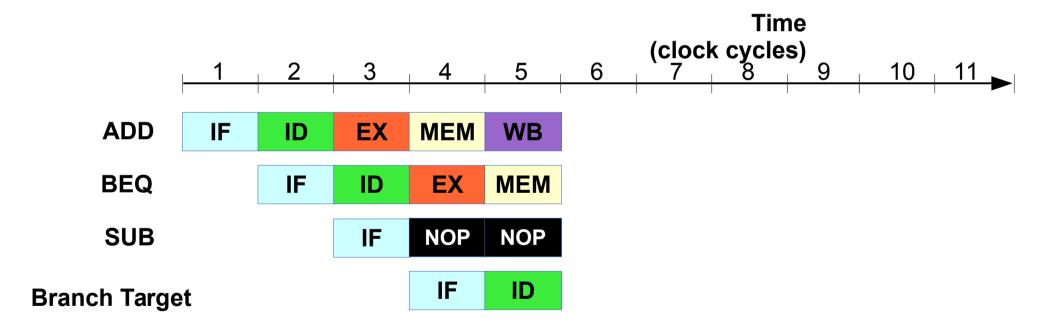
```
ADD R2, R3,R4
BEQ R2, R4, loop
SUB R5, R5,R4
```

---



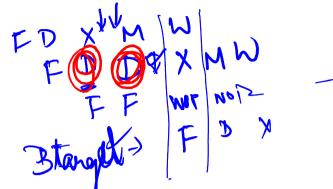
```
ADD R2, R3,R4
BEQ R2, R4, loop
SUB R5, R5,R4
```

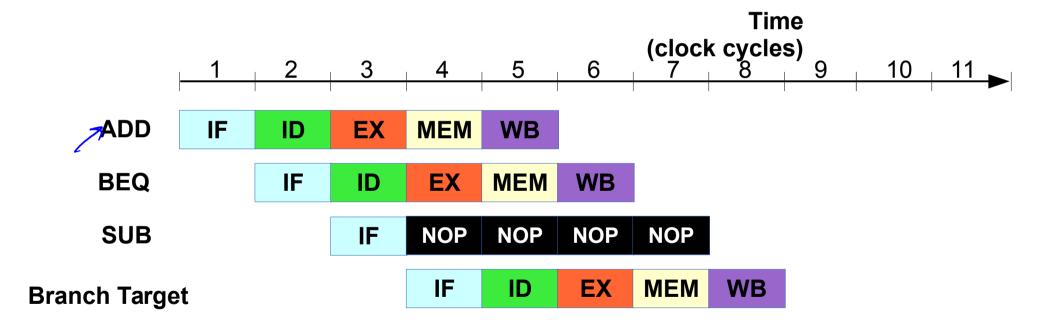
---



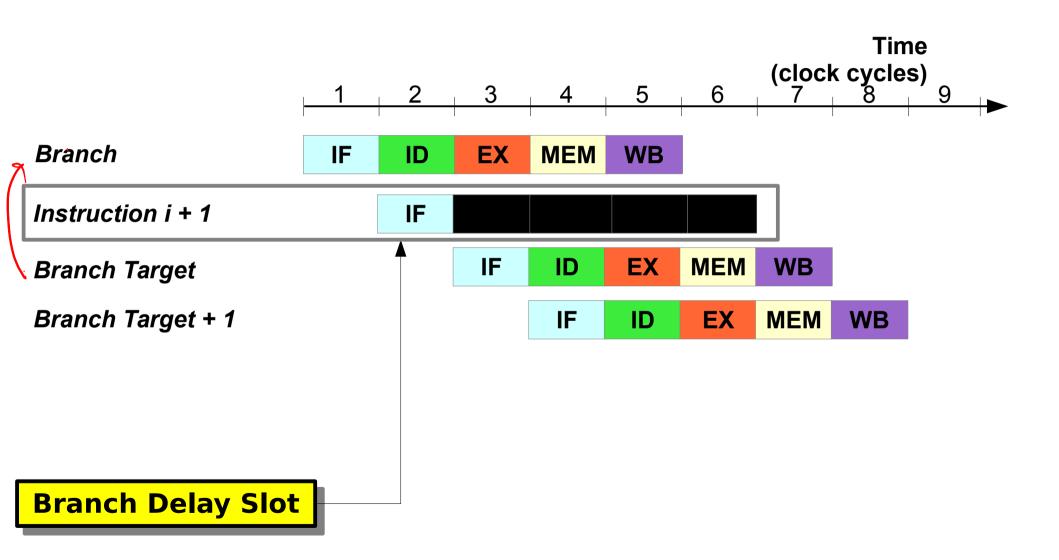
ADD R2, R3,R4 BEQ R2, R4, loop SUB R5, R5,R4

. . .

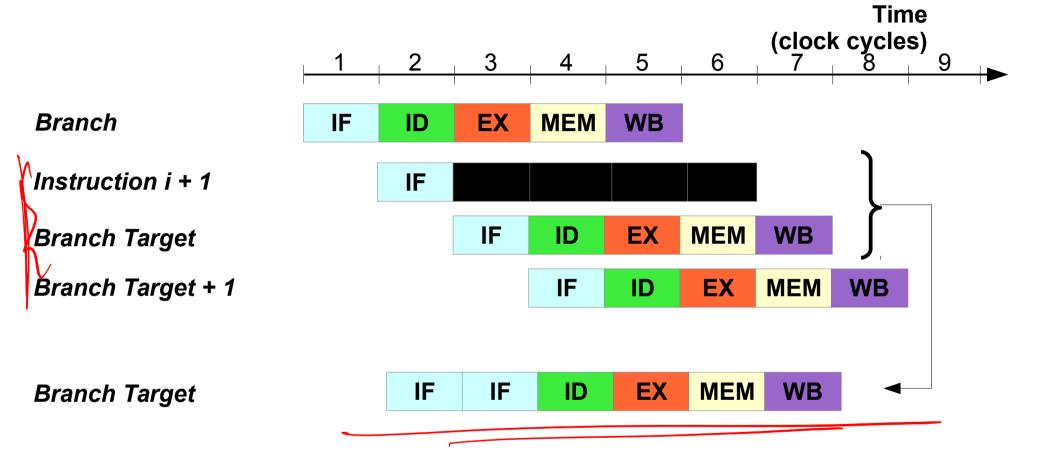




# **Branch Delay Slot**



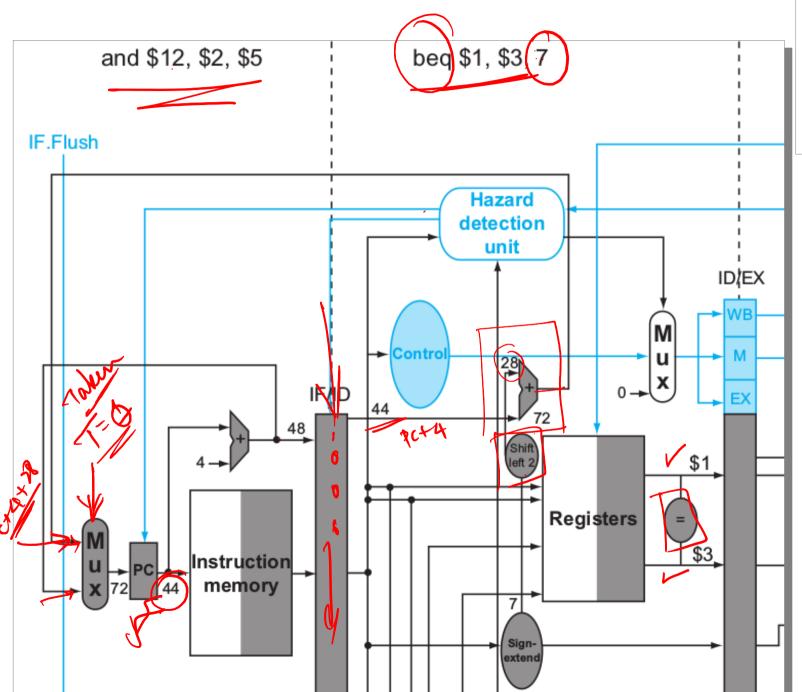
## **Branch Hazards**



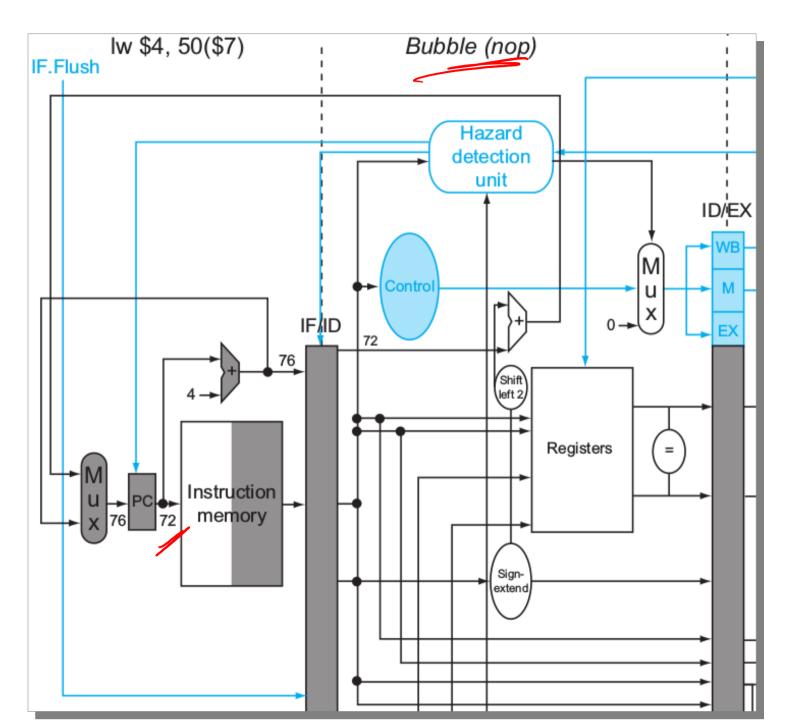
 1 stall cycle for every branch yields a performance loss of 10% to 30%!

## Example – Branch Taken

```
36 sub $10, $4, $8
40 beq $1, $3, 7
44 and $12, $2, $5
48 or $13, $2, $6
52 add $14, $4, $2
56 slt $15, $6, $7
. . . .
72 lw $4, 50($7)
```



36 sub \$10, \$4, \$8
40 beq \$1, \$3, 7 #
44 and \$12, \$2, \$5
48 or \$13, \$2, \$6
52 add \$14, \$4, \$2
56 slt \$15, \$6, \$7
. . .
72 lw \$4, 50(\$7)



```
36 sub $10, $4, $8

40 beq $1, $3, 7 #

44 and $12, $2, $5

48 or $13, $2, $6

52 add $14, $4, $2

56 slt $15, $6, $7

. . .

72 lw $4, 50($7)
```

## Branch Evaluation in ID - Steps

Are beq inputs ready?

## Branch Evaluation in ID — Steps

- Decode the instruction
- Decide whether to bypass/forward to the equality unit
  - Forwarding Logic has to be modfied
- Complete the comparison
- If branch taken, set the PC to the branch target address.

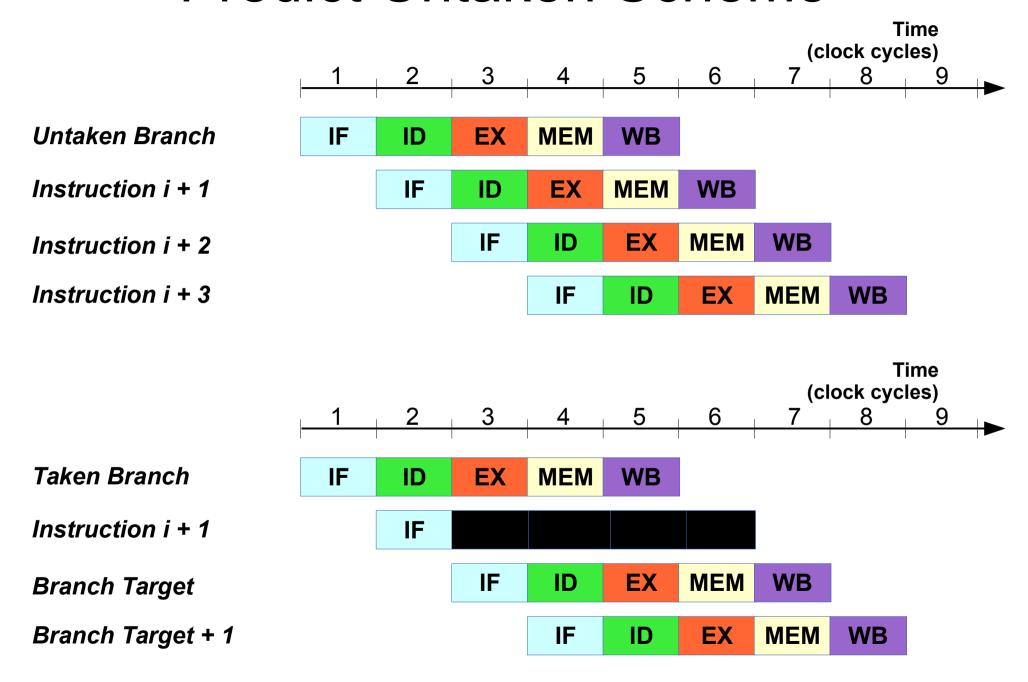
## Branch Evaluation – Forwarding

- New forwarding logic required
  - Source operands can come from ALU/MEM or MEM/WB
- If source operands are not ready, data hazard can occur and a stall will be needed.

```
...
add $1, $2, $2
beq $1, $3, 28
...
```

- Freeze the pipeline
- Static Prediction
  - Predict Untaken, Predict Taken
- Delayed Branch
  - Fill Branch Delay Slot

## Predict Untaken Scheme



Predict Taken

beq and	\$1, \$3, 28	
or	\$12, \$2, \$5 \$13, \$6, \$2	
add Iw	\$14, \$2, \$2 \$4, 50(\$7)	

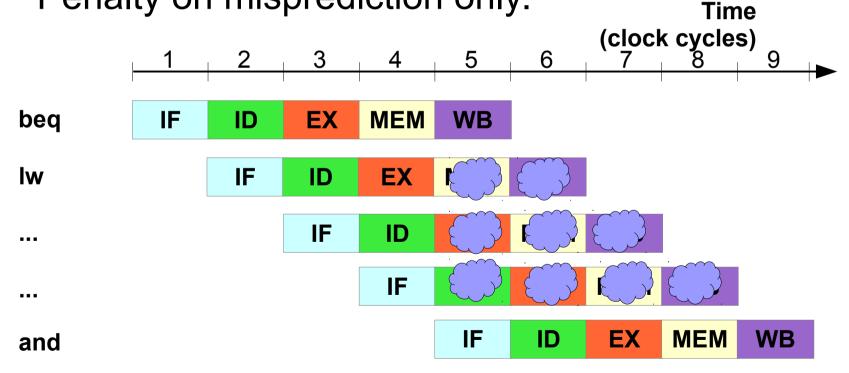
- Predict Taken
  - Great if prediction is correct

beq	\$1, \$3, 28	
and	\$12, \$2, \$5	
or	\$13, \$6, \$2	
add	\$14, \$2, \$2	
lw	\$4, 50(\$7)	

- Predict Taken
  - Great if prediction is correct.

beq \$1, \$3, 28 and \$12, \$2, \$5 or \$13, \$6, \$2 add \$14, \$2, \$2 lw \$4, 50(\$7)

Penalty on misprediction only.



Fill the branch delay slot

```
sll ...

srl $14, $2, $2

beq $1, $3, 28

and $12, $2, $5

...
```

Fill the branch delay slot

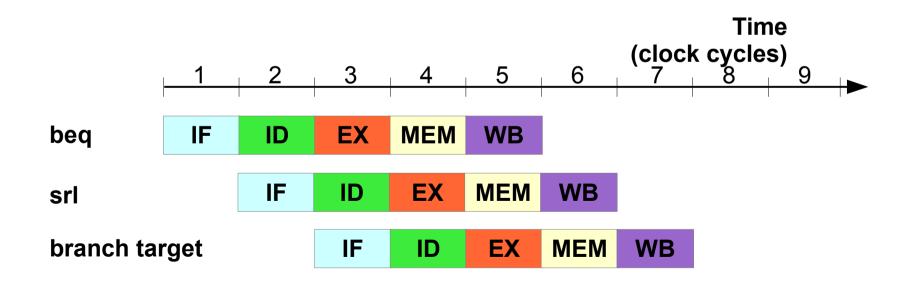
```
sll ...

srl $14, $2, $2

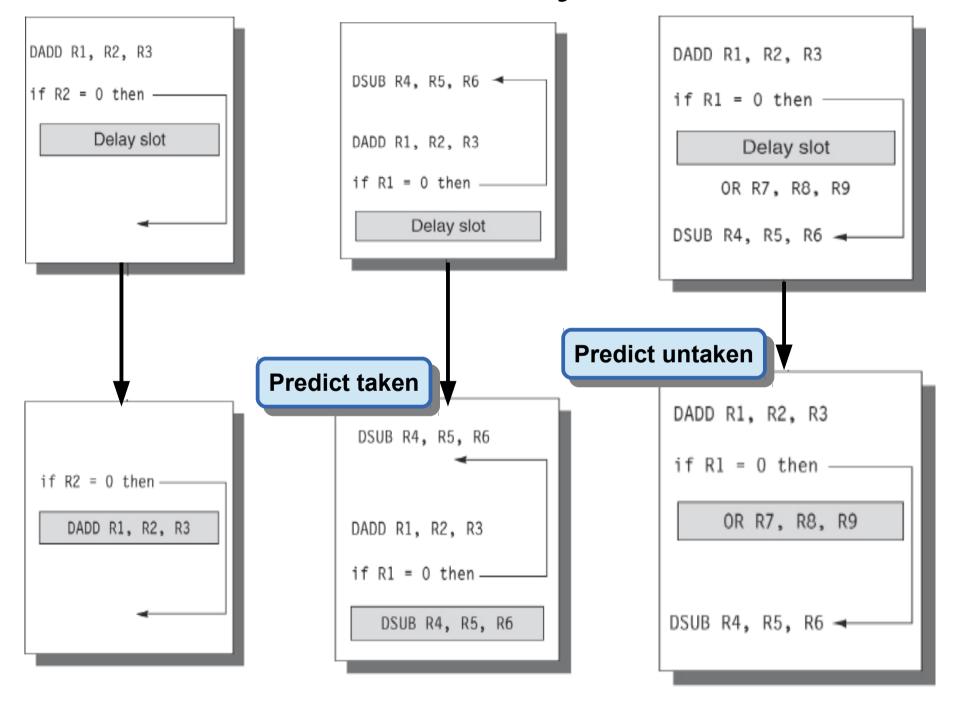
beq $1, $3, 28

and $12, $2, $5

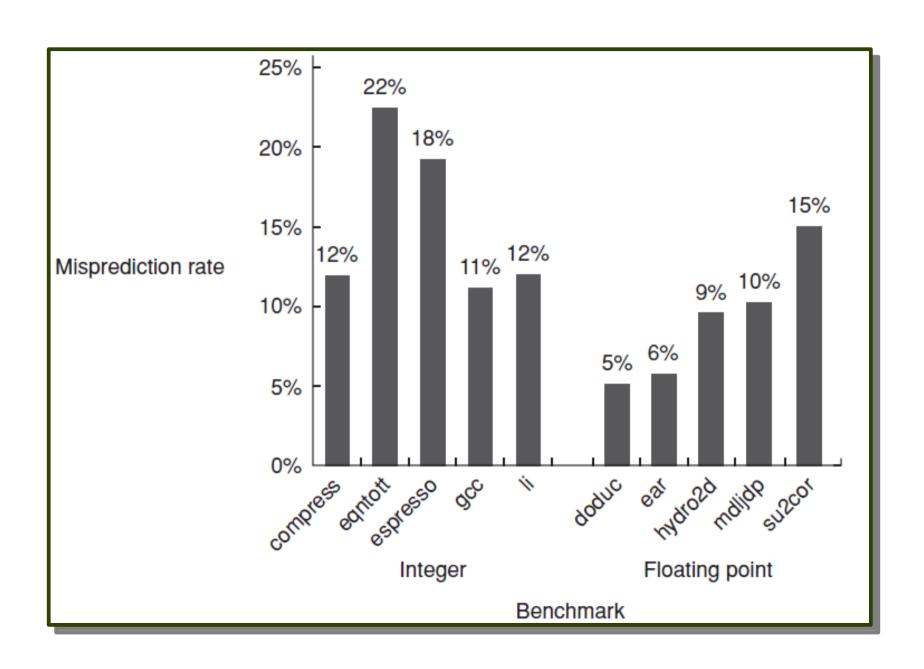
...
```



## **Branch Delay Slot**



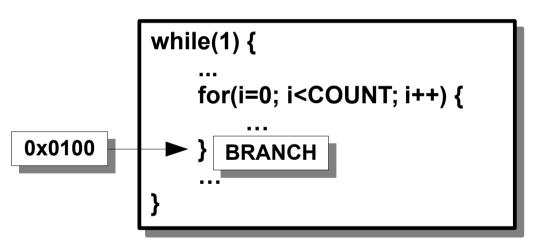
## Static Branch Prediction



```
while(1) {
...
for(i=0; i<COUNT; i++) {
...

Dx0100

BRANCH
...
}
```

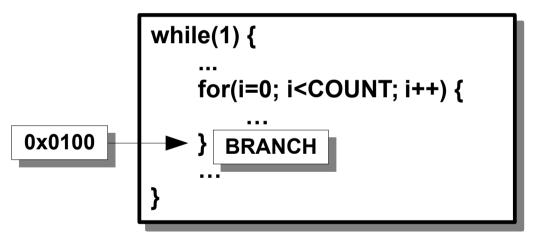


### **BRANCH TARGET BUFFER**

PC	Prediction	Target
0x0100 →	1	0x128
0x0154	. 0	0x080
0x0210	. 1	0x300
	1	

Addresses of branches in the program

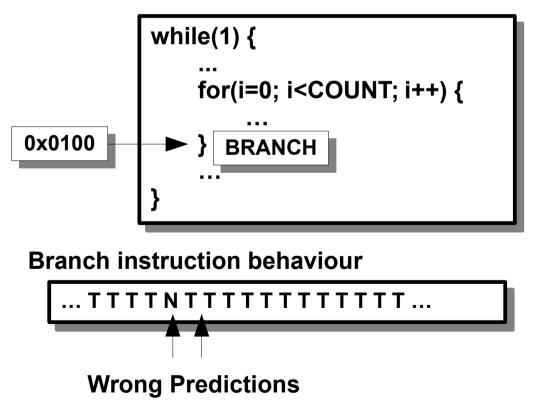
- Branch Target Buffer
  - Single bit predictors (1-bit bimodal predictor)
  - Change prediction with branch behaviour
  - No. of wrong predictions?



## BRANCH TARGET BUFFER PC Prediction Target 0x0100 1 0x128 0x0154 0 0x080 0x0210 1 0x300 ... 1 0x300 Addresses of branches 1 0x300

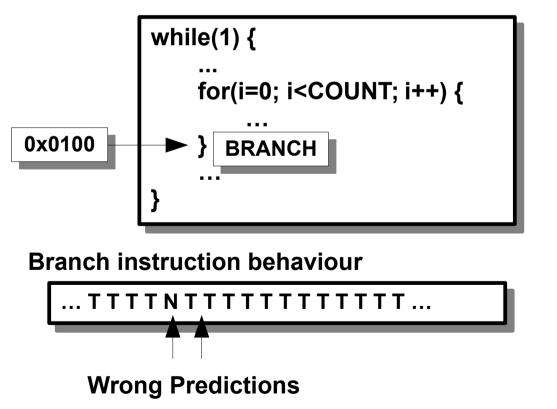
in the program

- Branch Target Buffer
  - Single bit predictors (1-bit bimodal predictor)
  - Change prediction with branch behaviour
  - No. of wrong predictions?



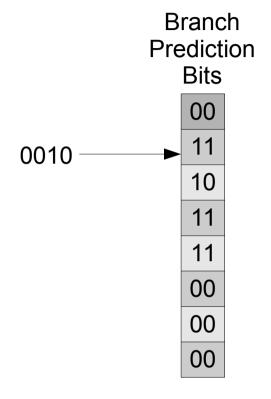
# PC 0x0100 0x0154 0x0210 1 0x300 1 0x300 1 0x300 1 Addresses of branches in the program

- Branch Target Buffer
  - Single bit predictors (1-bit bimodal predictor)
  - Change prediction with branch behaviour
  - No. of wrong predictions?

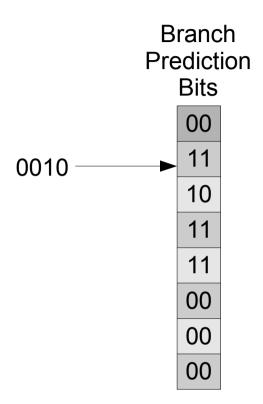


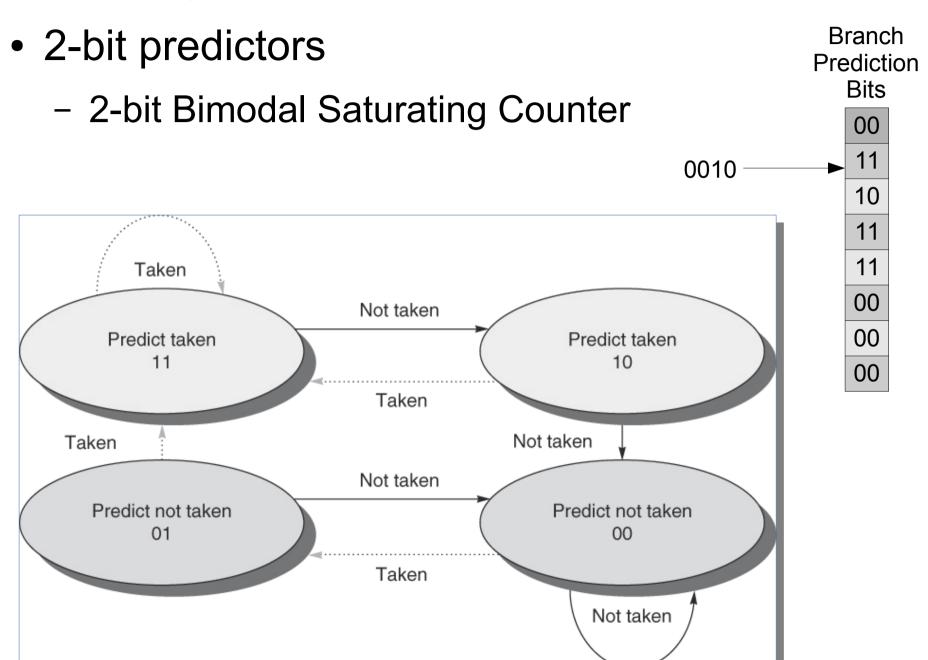
# PC Prediction Target 0x0100 1 0x128 0x0154 0 0x080 0x0210 1 0x300 1 Addresses of branches in the program

Can we do better?



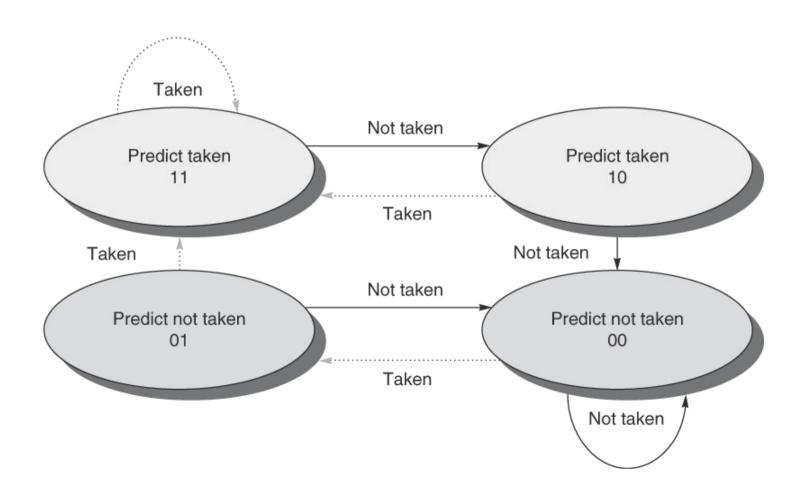
- 2-bit predictors
  - 2-bit Bimodal Saturating Counter

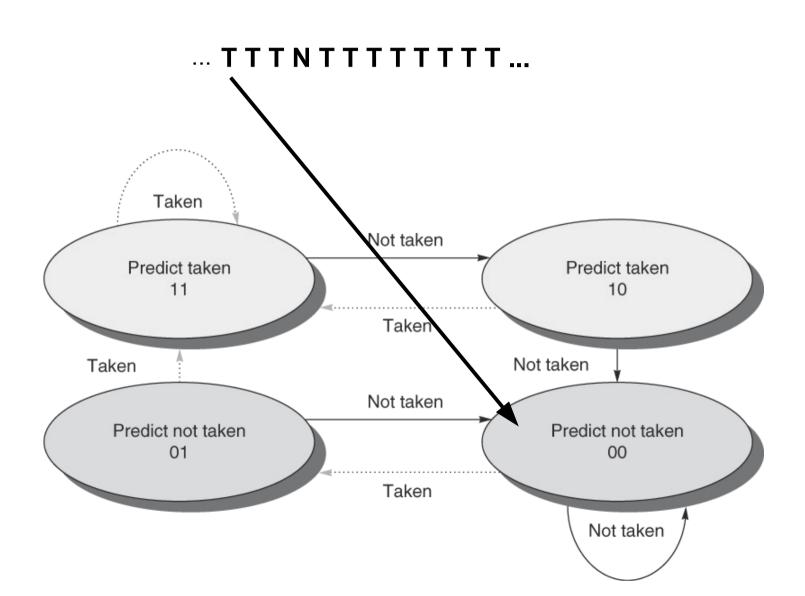


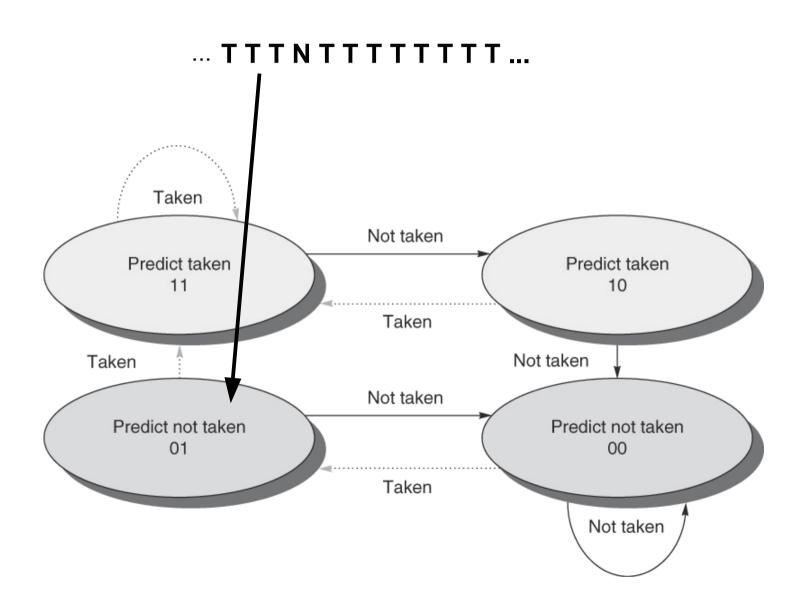


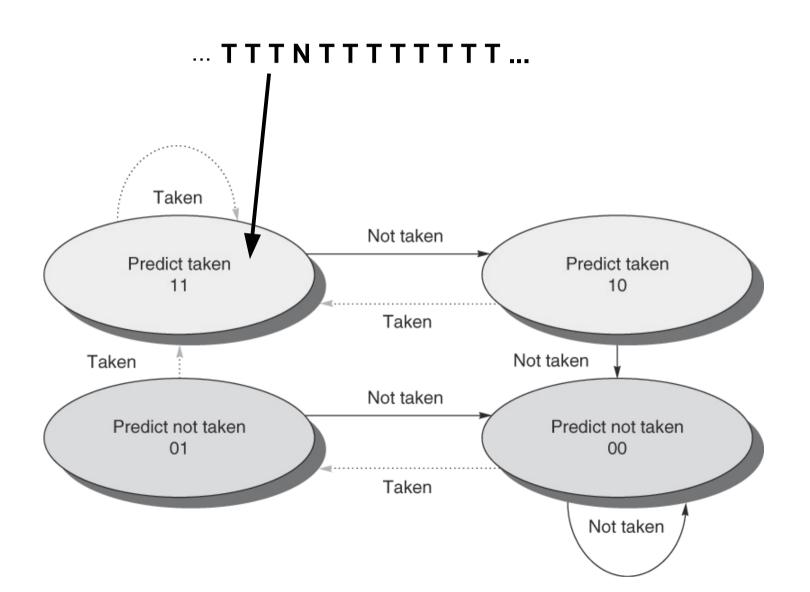
• 2-bit predictors

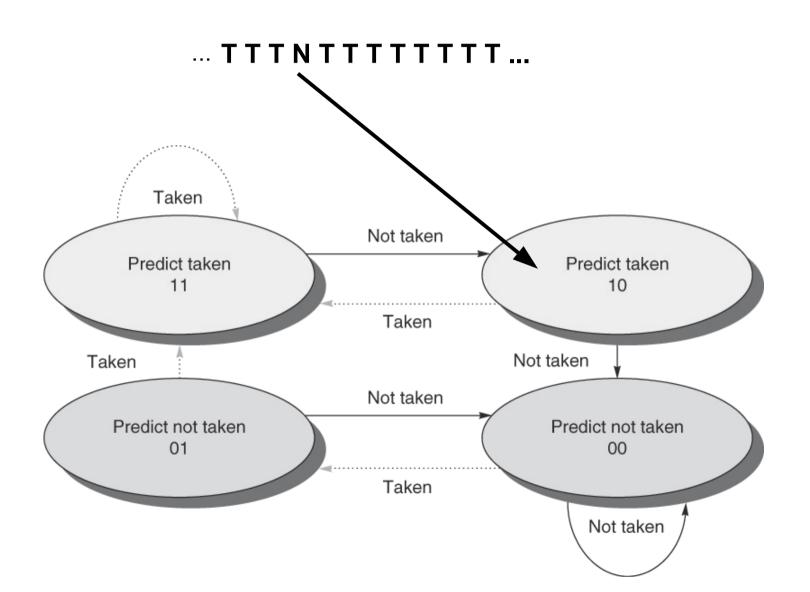
### ... TTTNTTTTTT...

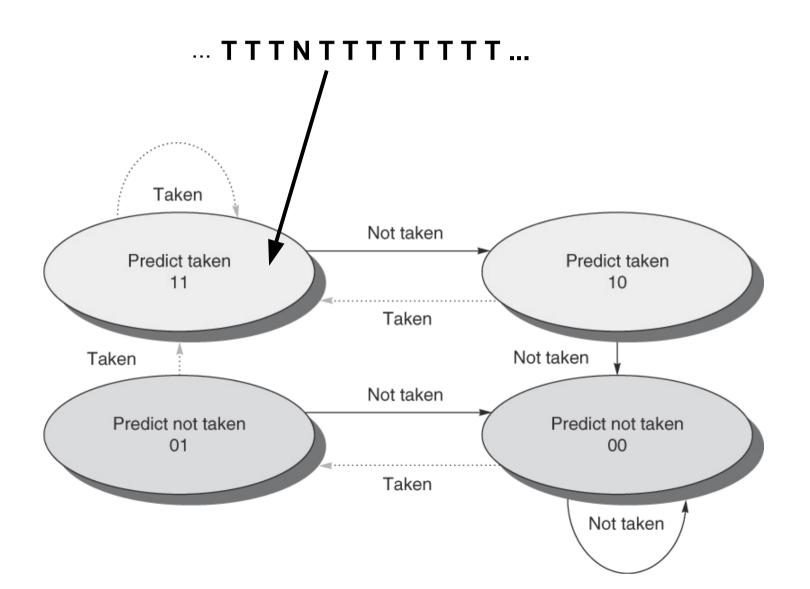


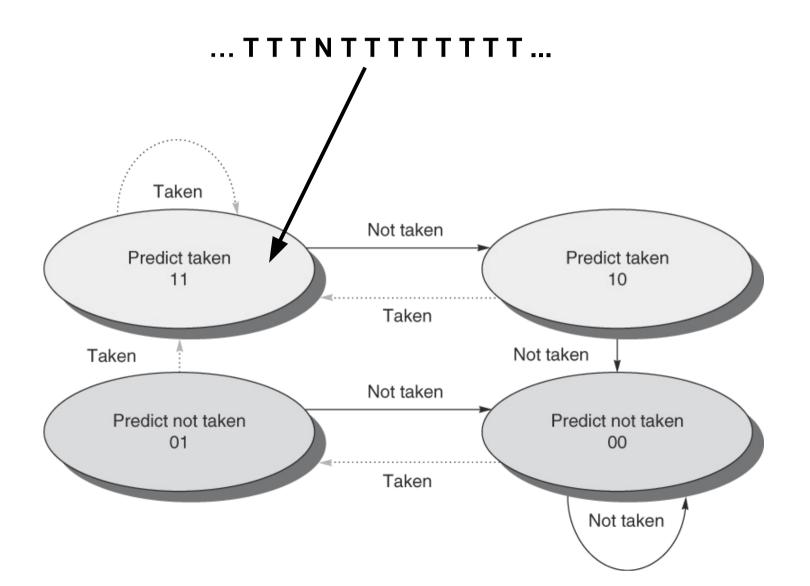






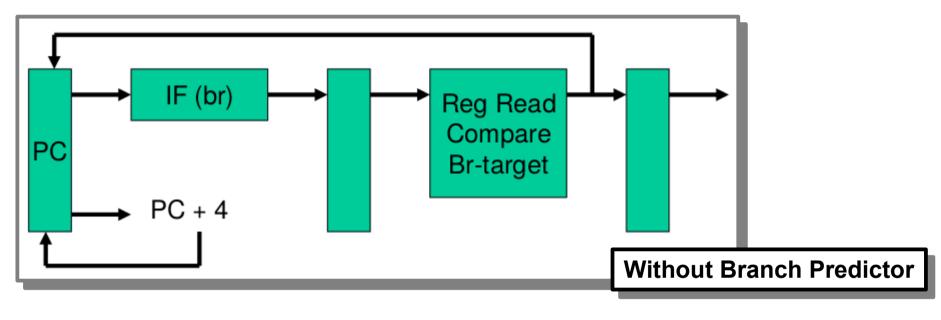


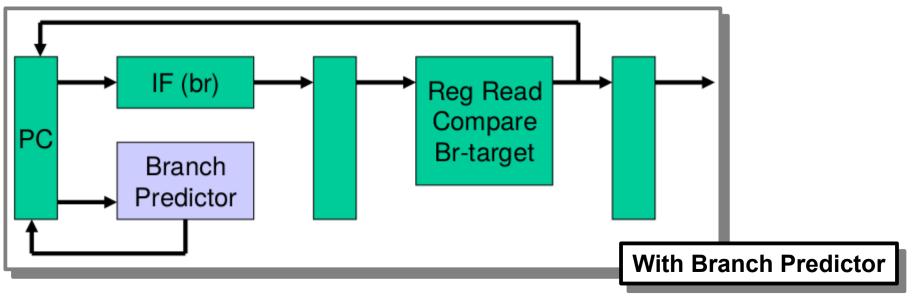


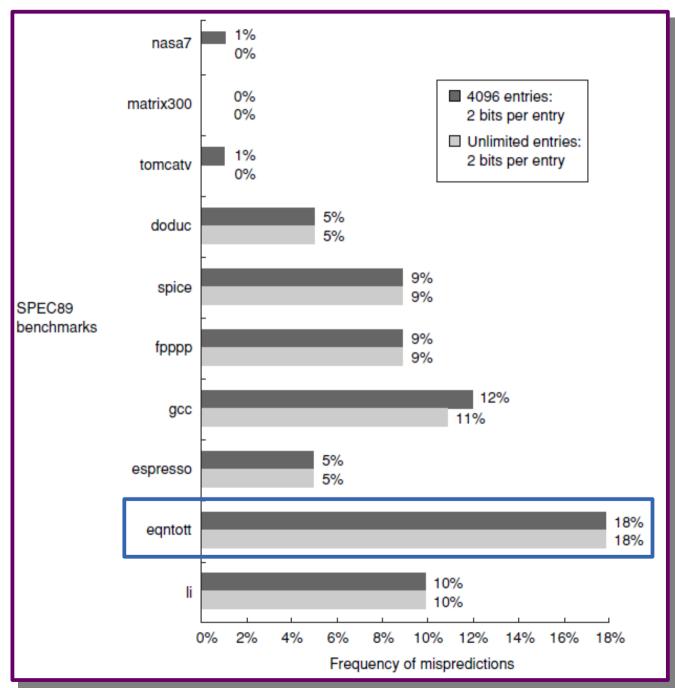


n-bit saturating counters

## **Branch Predictors**







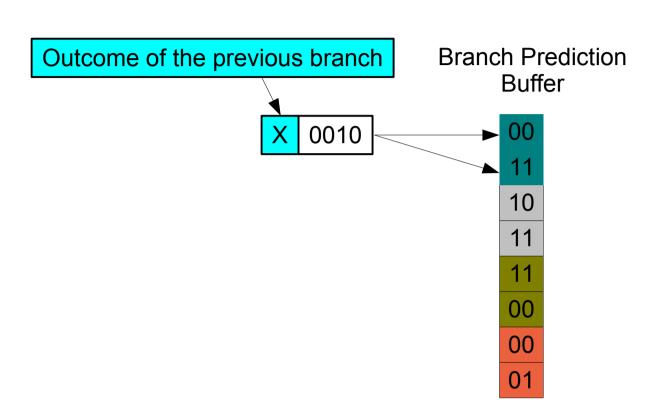
**Observations?** 

## Correlating Branch Predictors

```
if (aa == 2)
     aa = 0;
if (bb == 2)
     bb = 0;
if (aa!=bb) {
```

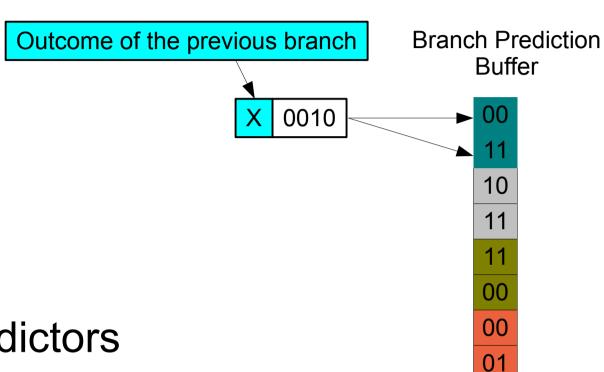
## Correlating Branch Predictors

```
if (aa == 2)
     aa = 0;
if (bb == 2)
     bb = 0;
if (aa!=bb) {
```



## Correlating Branch Predictors

```
if (aa == 2)
    aa = 0;
if (bb == 2)
    bb = 0;
if (aa!=bb) {
```



- Two-level predictors
  - (1,2) predictor

if (aa == 2)Outcome of the previous branch **Branch Prediction** aa = 0;Buffer if (bb == 2)0010 bb = 0; 10 if (aa!=bb) { 11 00 00 Two-level predictors - (1,2) predictor

```
if (aa == 2)

aa = 0;

if (bb == 2)

bb = 0;

if (aa!=bb) {

Outcomes of the previous 2 branches

**XX 0010

Outcomes of the previous 2 branches

**XX 0010

Outcomes of the previous 2 branches

**XX 0010

Outcomes of the previous 2 branch Prediction Buffer

**XX 0010

Outcomes of the previous 2 branch Prediction Buffer

**XX 0010

Outcomes of the previous 2 branch Prediction Buffer

**XX 0010

Outcomes of the previous 2 branch Prediction Buffer

**XX 0010

Outcomes of the previous 2 branch Prediction Buffer

**XX 0010

Outcomes of the previous 2 branches

Outcomes of the previous 2 branches

Outcomes of the previous 2 branch Prediction Buffer

Outcomes of the previous 2 branches

Outcomes of the previous 2 branches

Outcomes of the previous 2 branch Prediction Buffer

Outcomes of the previous 2 branches

Outcomes
```

```
if (aa == 2)

aa = 0;

if (bb == 2)

bb = 0;

if (aa!=bb) {

Outcomes of the previous 2 branches

XX 0010

Branch Prediction
Buffer

11

11

00

11

00

11

00

11

00

11

00

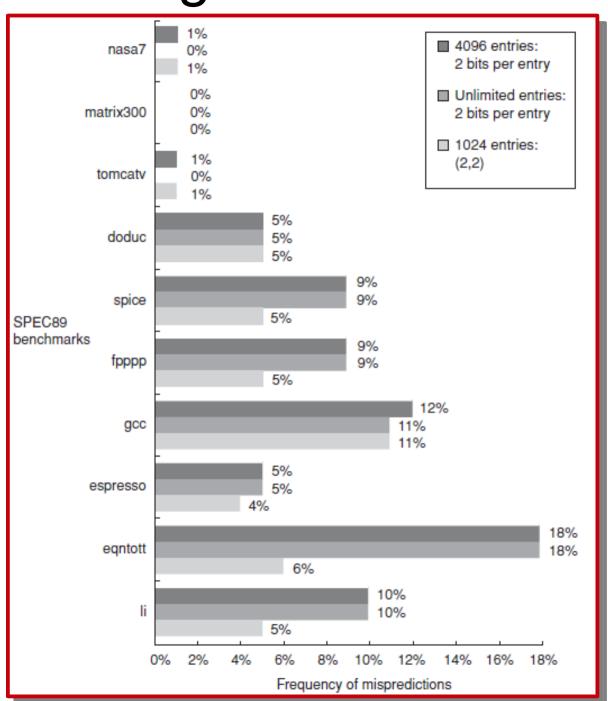
11

00

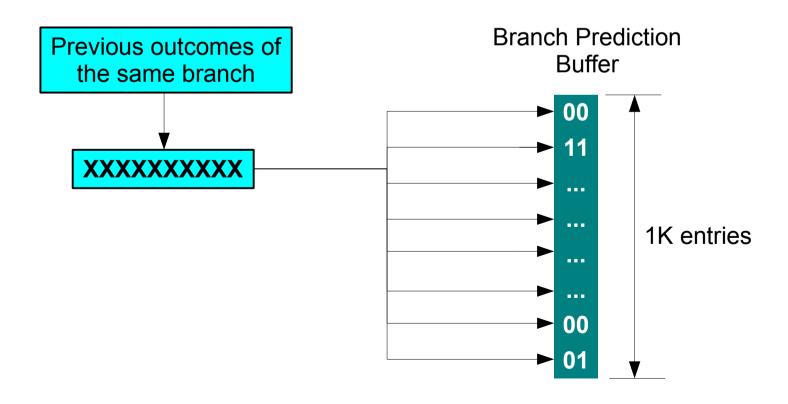
01
```

(m, n) BPB bits =  $2^m \times n \times No$ . of prediction entries

Yeh and Patt, Alternative implementations of two-level adaptive branch prediction, ISCA, 1992.

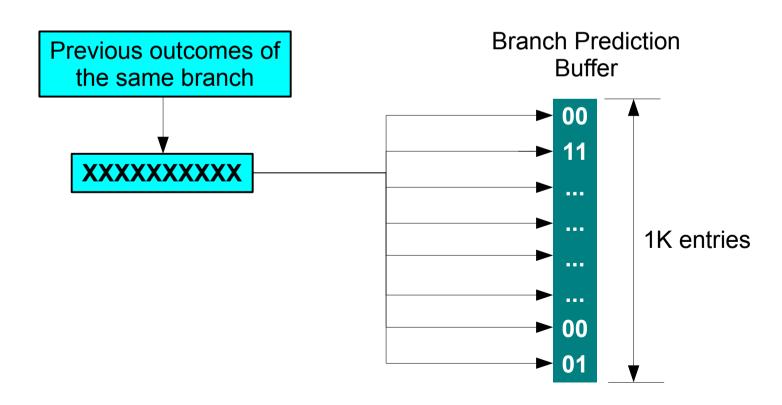


## **Local Predictors**



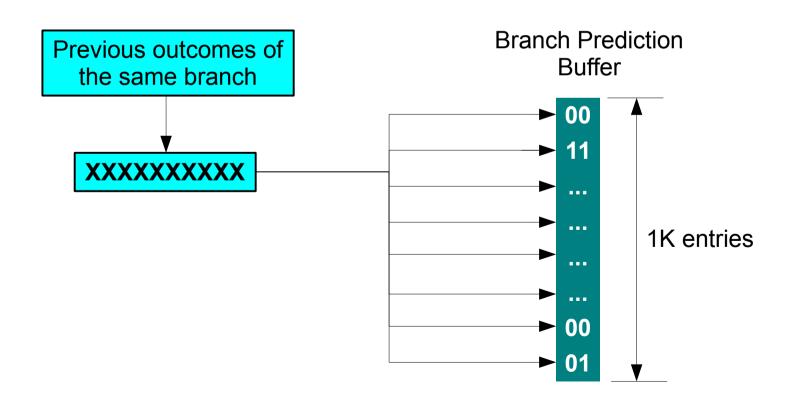
## **Local Predictors**

A history of branch behaviour is recorded



### **Local Predictors**

- A history of branch behaviour is recorded
- One for each possible combination of outcomes for the last n occurrences of this branch



# Local Predictors – Example

```
while(1) {
...
for(i=0; i<COUNT; i++) {
...

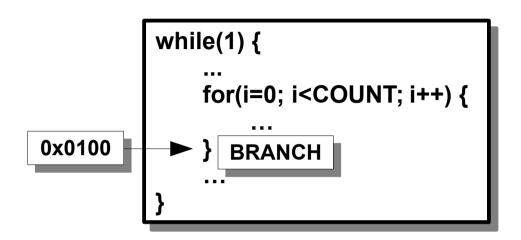
Dx0100

BRANCH
...
}
```

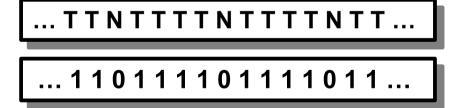
#### **Branch instruction behaviour**

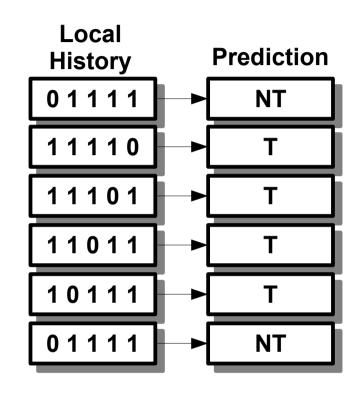
```
... TTNTTTTNTTTNTT...
... 11011110111...
```

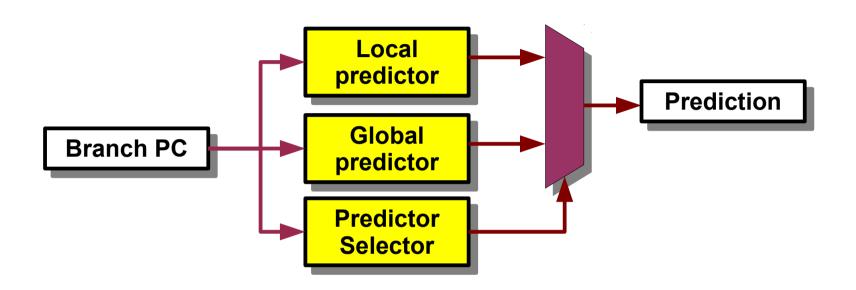
# Local Predictors – Example



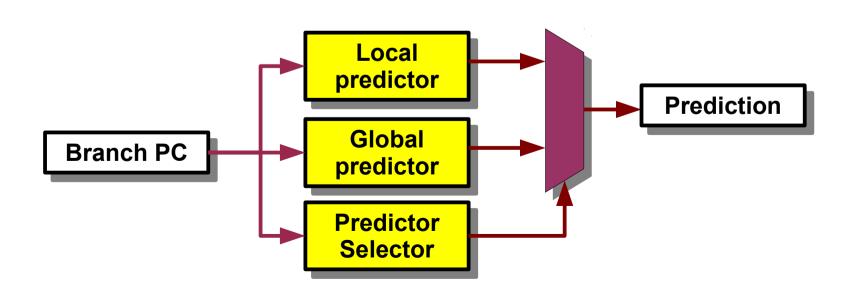
**Branch instruction behaviour** 



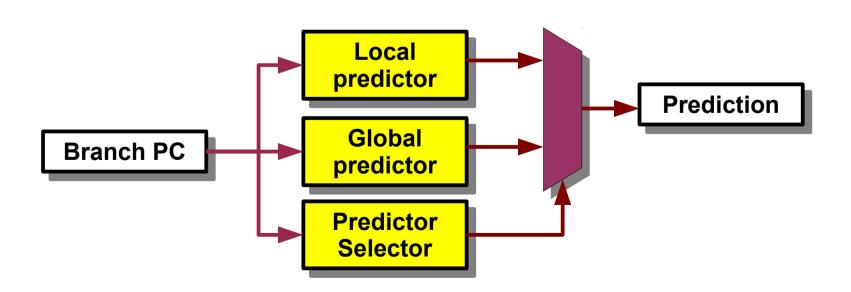


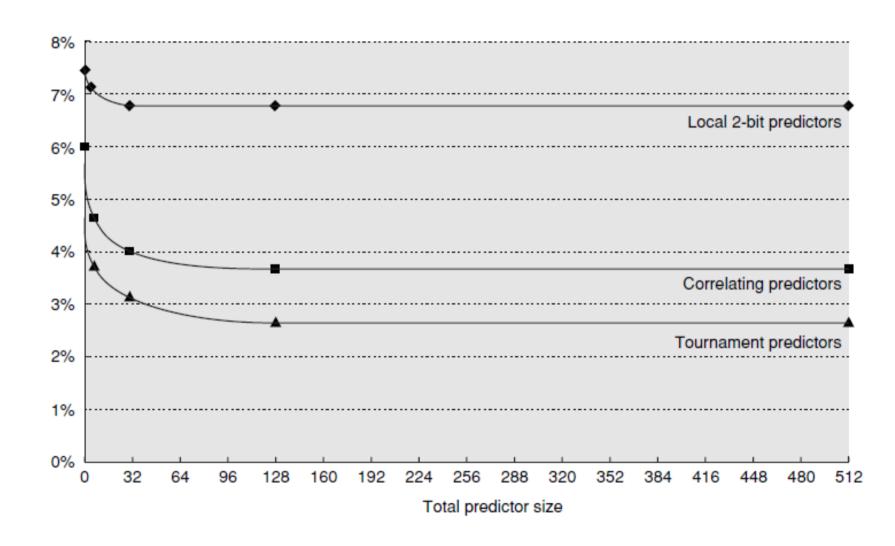


Use multiple predictors: Global, local or mix



- Use multiple predictors: Global, local or mix
- Combine them with a selector
  - 2 bit saturating counter to select the right predictor for the branch (global vs. local)





Conditional branch misprediction rate

### **Outline**

- Pipeline, Pipelined datapath
- Dependences, Hazards
  - Structural, Data Stalling, Forwarding
- Control Hazards
- Branch prediction