

# Simplified View of Memory

A Quick Look

# The Instruction Example

**a = b + c;**

- What are a, b, and c?

# The Instruction Example

**a = b + c;**

- What are a, b, and c?
- They identify unique locations in Memory
  - Addresses

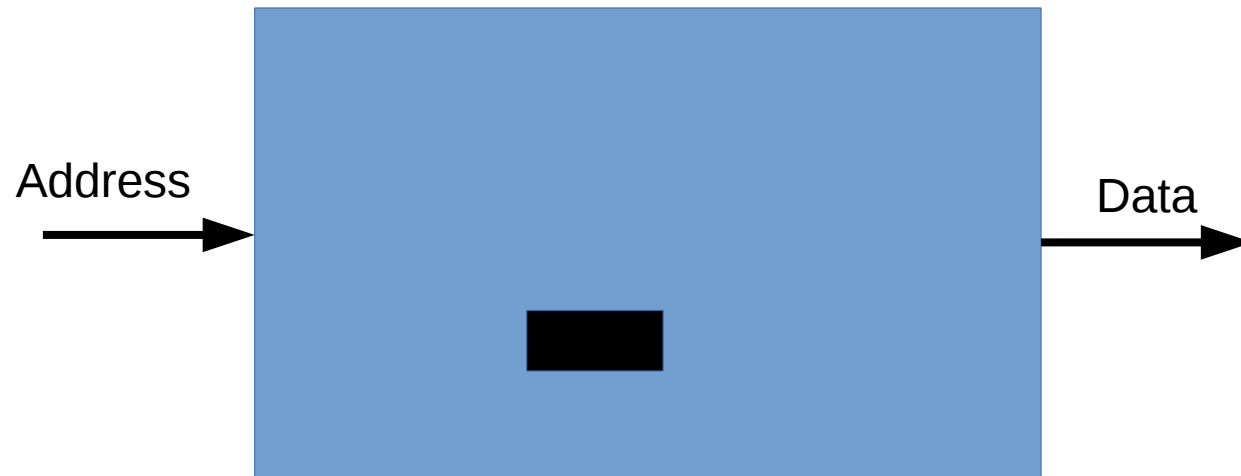
# Simplified View of Memory

- Memory stores bits

# Simplified View of Memory

- Memory stores bits
- What operations can a memory perform?
  - Read and Write

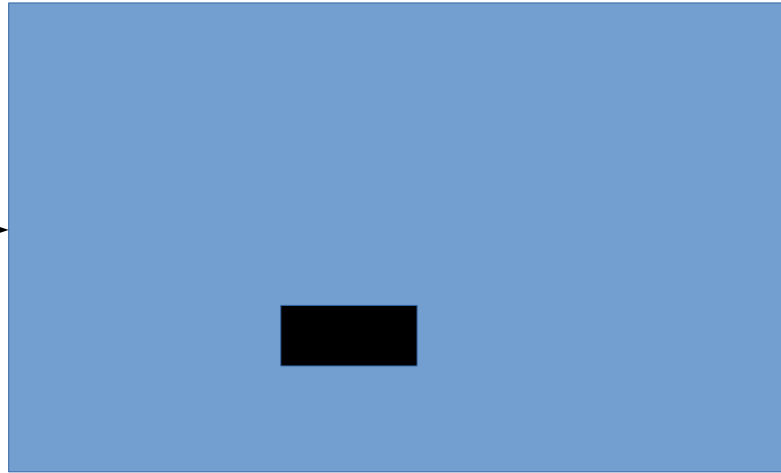
# Operations on Memory



# Operations on Memory

**Read Operation**

Address

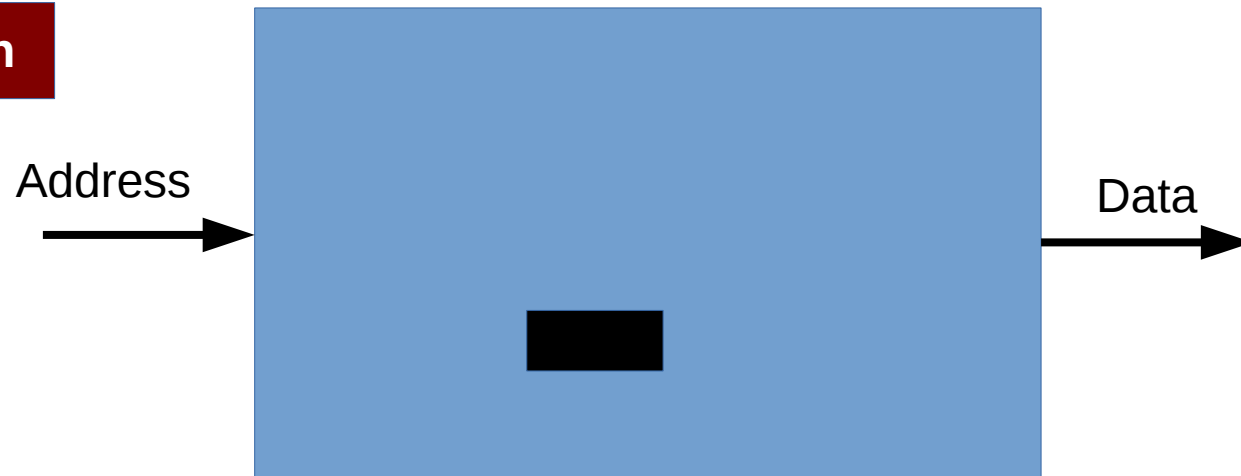


Data



# Operations on Memory

## Read Operation





# Operations on Memory

## Read Operation



## Write Operation



# Memory Capacities

- 1 KB of memory
- How many bytes in
- KB =
- MB =
- GB =
- PB =
- EB =

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- $\text{KB} = 1024 = 2^{10} \text{ Bytes}$
- $\text{MB} = 1024 \text{ KB} = 2^{20} \text{ Bytes}$
- $\text{GB} = 1024 \text{ MB} = 2^{30} \text{ Bytes}$
- $\text{TerraByte} = 1024 \text{ GB} = 2^{40} \text{ Bytes}$
- $\text{PetaByte} = 1024 \text{ TB} = 2^{50} \text{ Bytes}$
- $\text{ExaByte} = 1024 \text{ PB} = 2^{60} \text{ Bytes}$
- $\text{ZetaByte} = 1024 \text{ EB} = 2^{70} \text{ Bytes}$
- $\text{YotaByte} = 1024 \text{ ZB} = 2^{80} \text{ Bytes}$

# Memory Address Size

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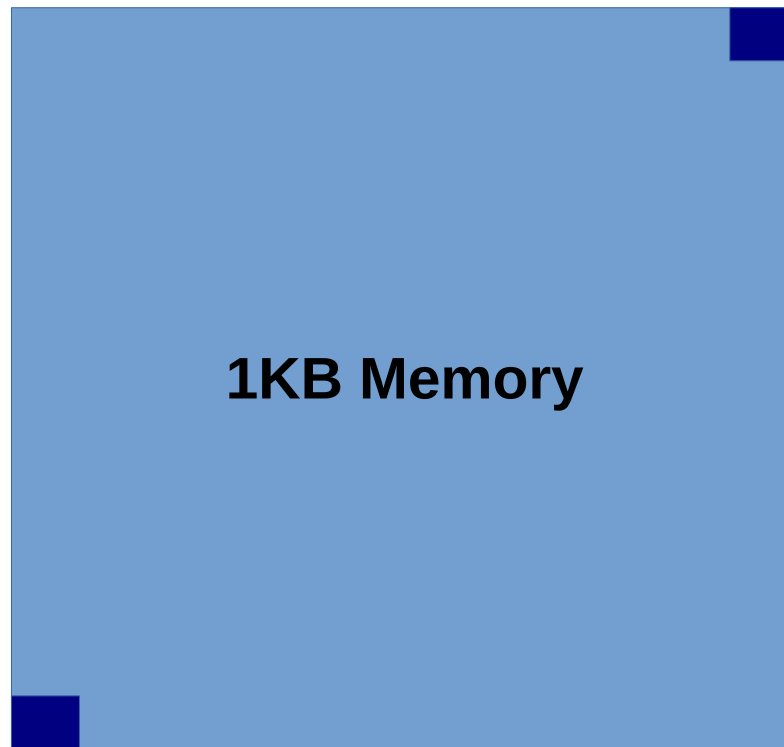
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- First Address = 0; Last address = 1023

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- Each byte has an address
- First Address = 0; Last address = 1023
- No. of bits in the address
  - $\log_2$  Size
  - $\log_2 1024 = 10$  bits

# Simplified 1KB Memory

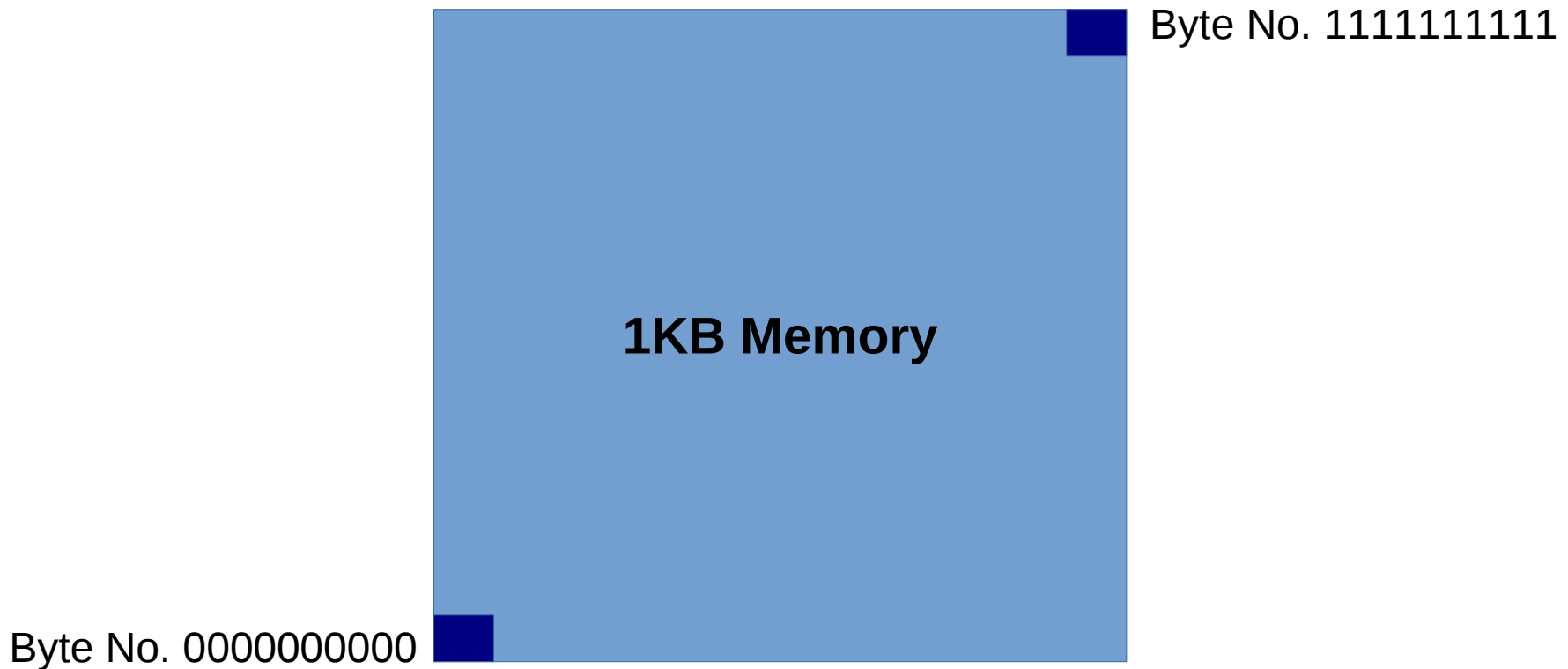
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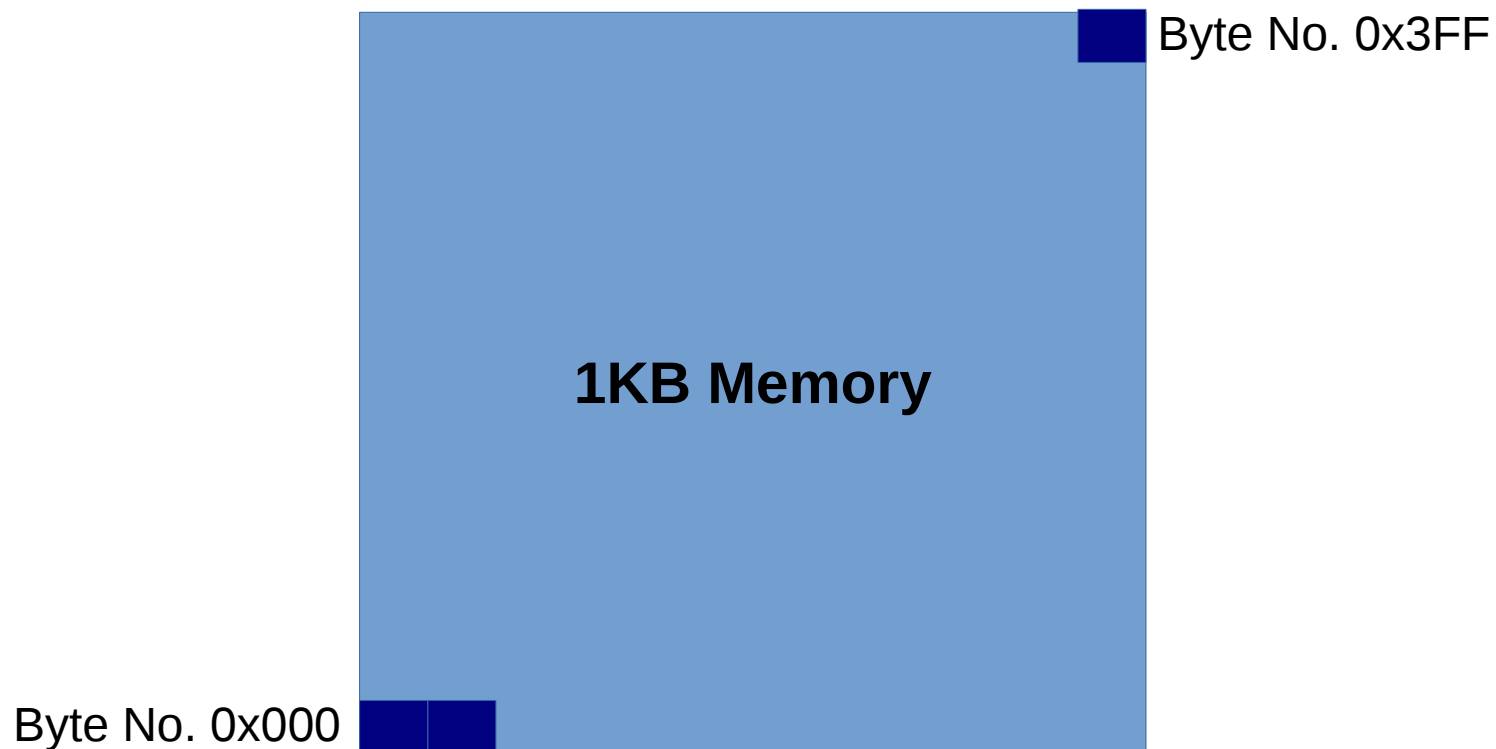
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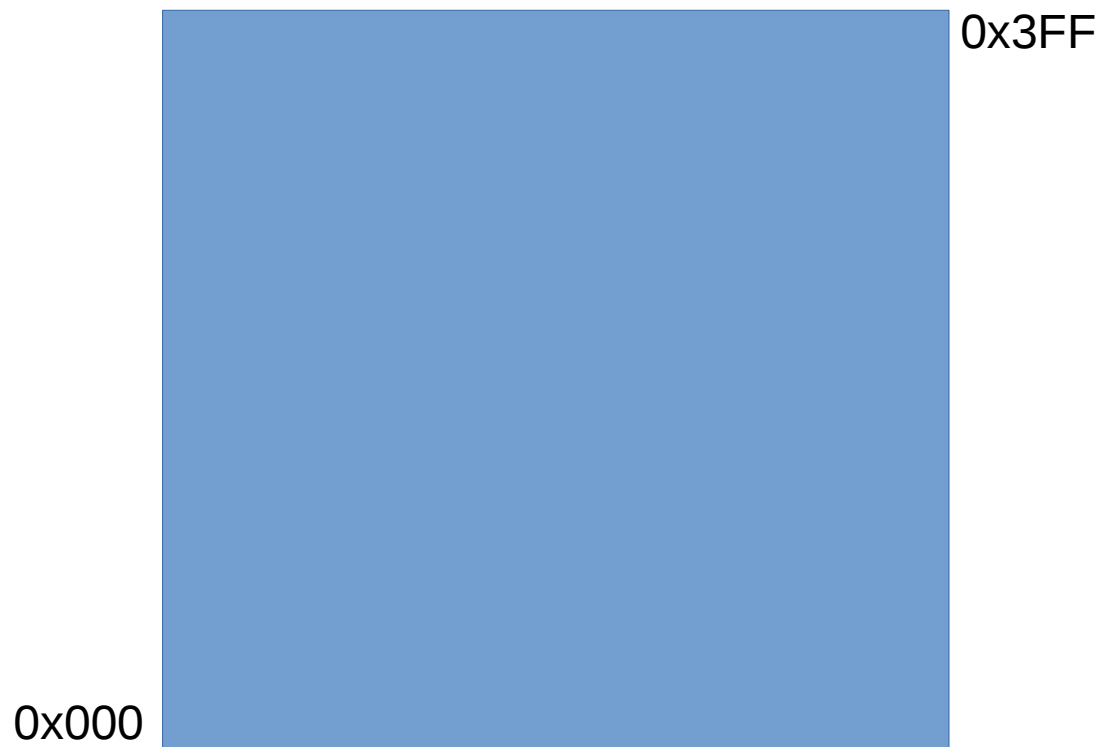
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# Simplified Memory

- Recall: Instructions and Data reside in the memory

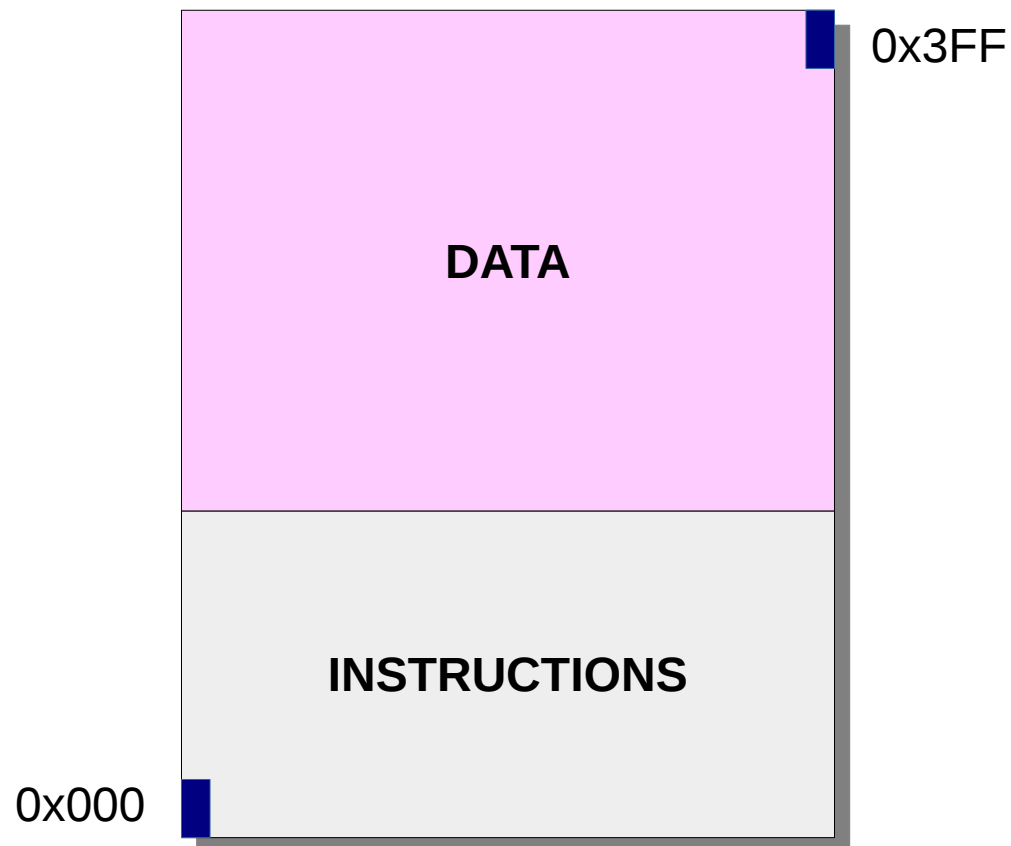


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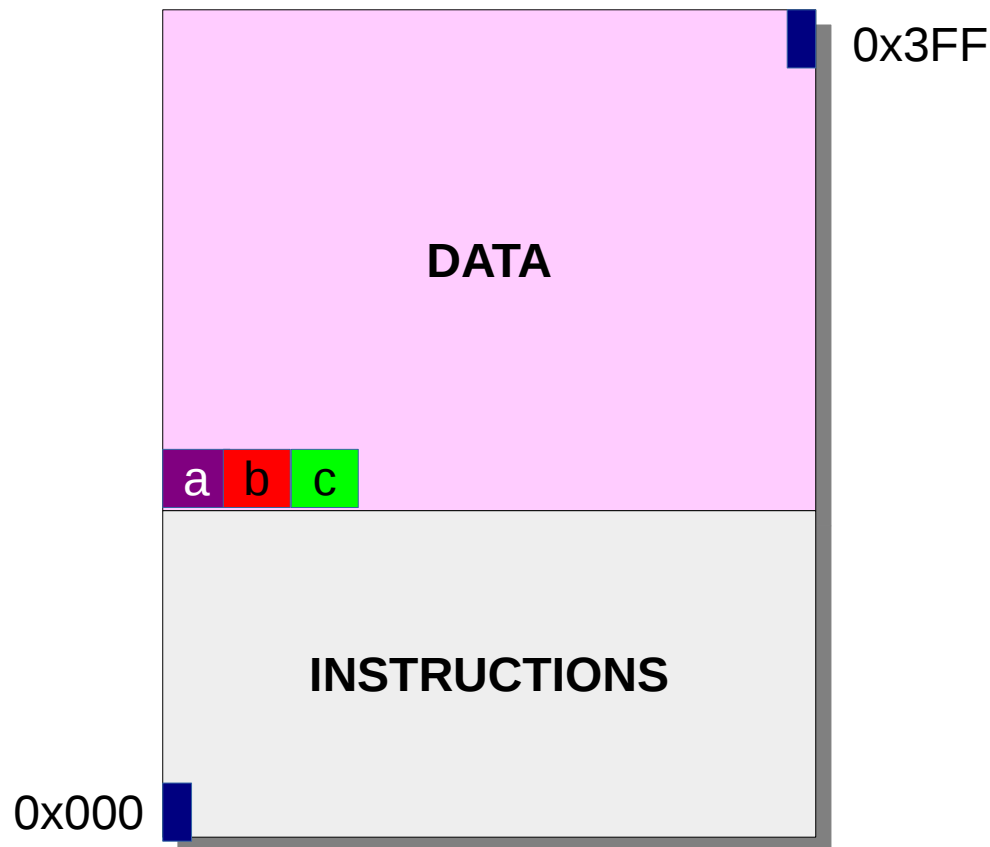
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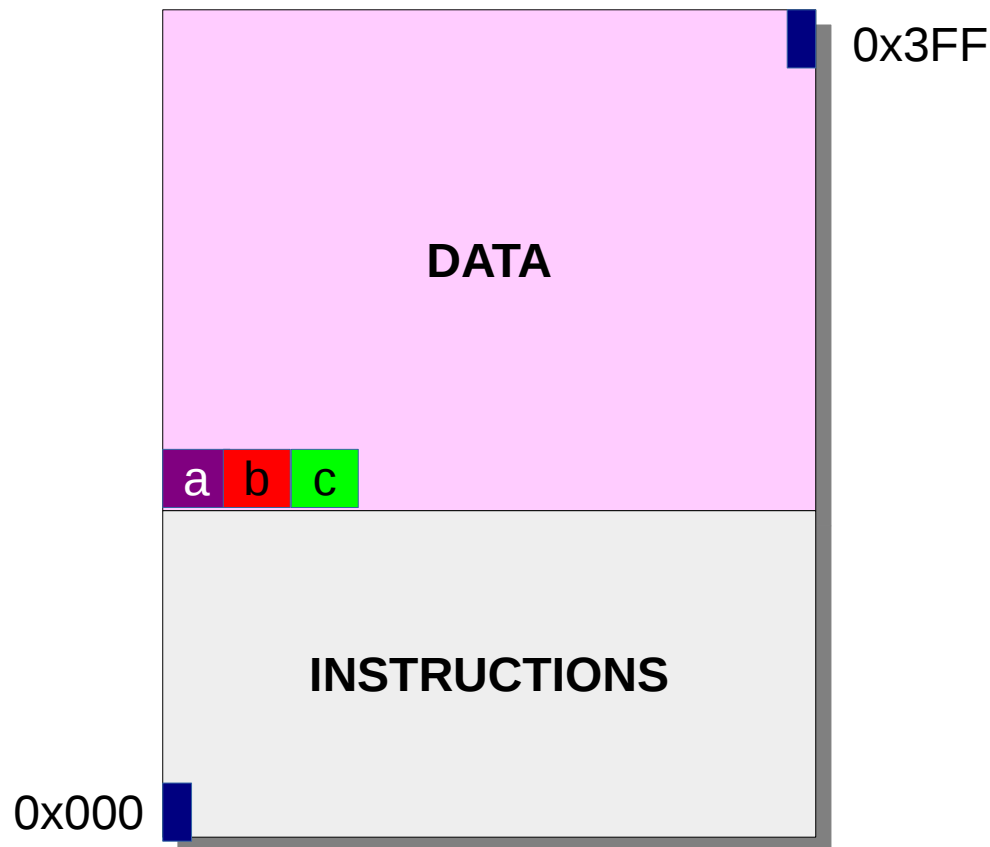
# Simplified Program Memory

- Instructions and Data reside in the memory
- Assume each of a, b, c are 4 Bytes



# Simplified Program Memory

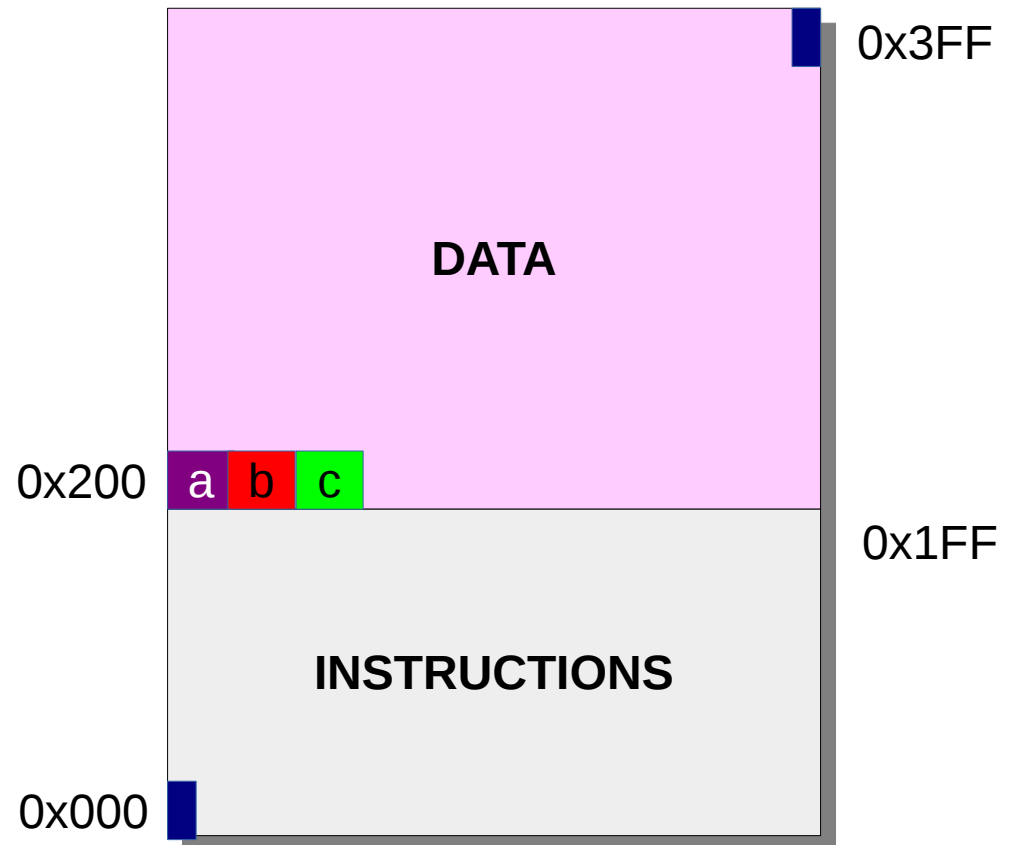
- Instructions and Data reside in the memory
- Assume each of a, b, c are 4 Bytes



If Instructions and data occupy equal bytes in the memory, What are the addresses of a, b, and c?

# Data Memory

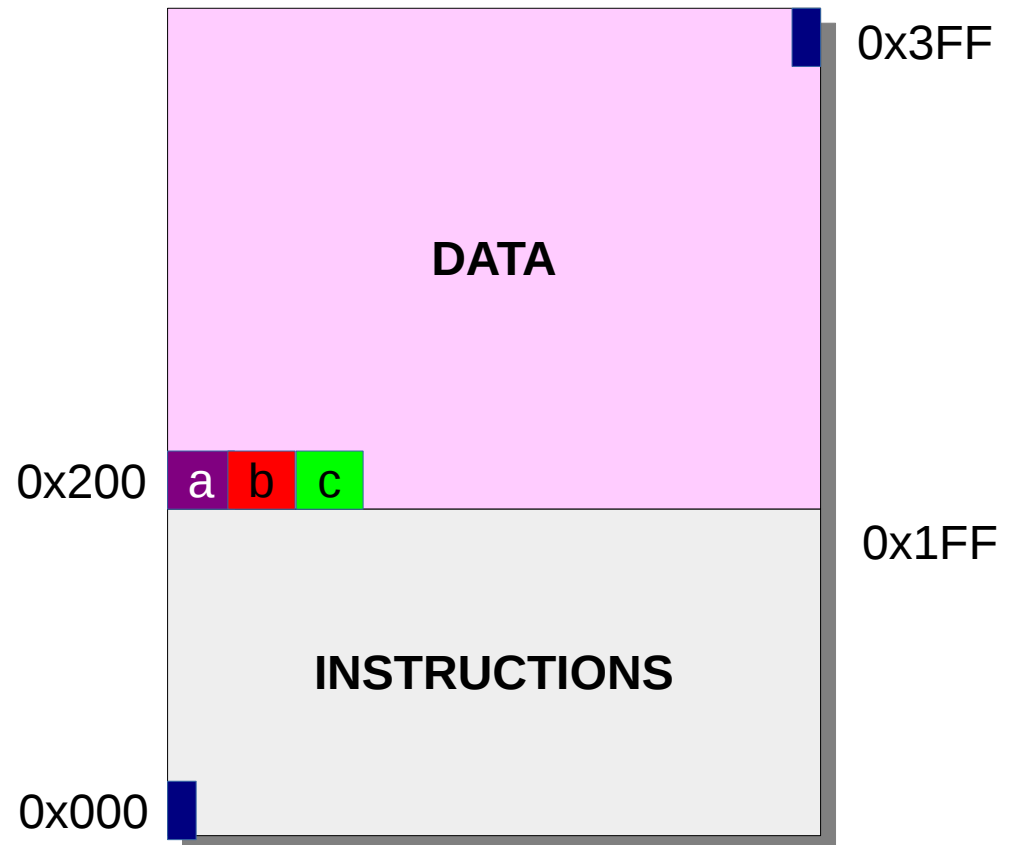
- Address range = 0 to 1023 Bytes = 1024 Bytes





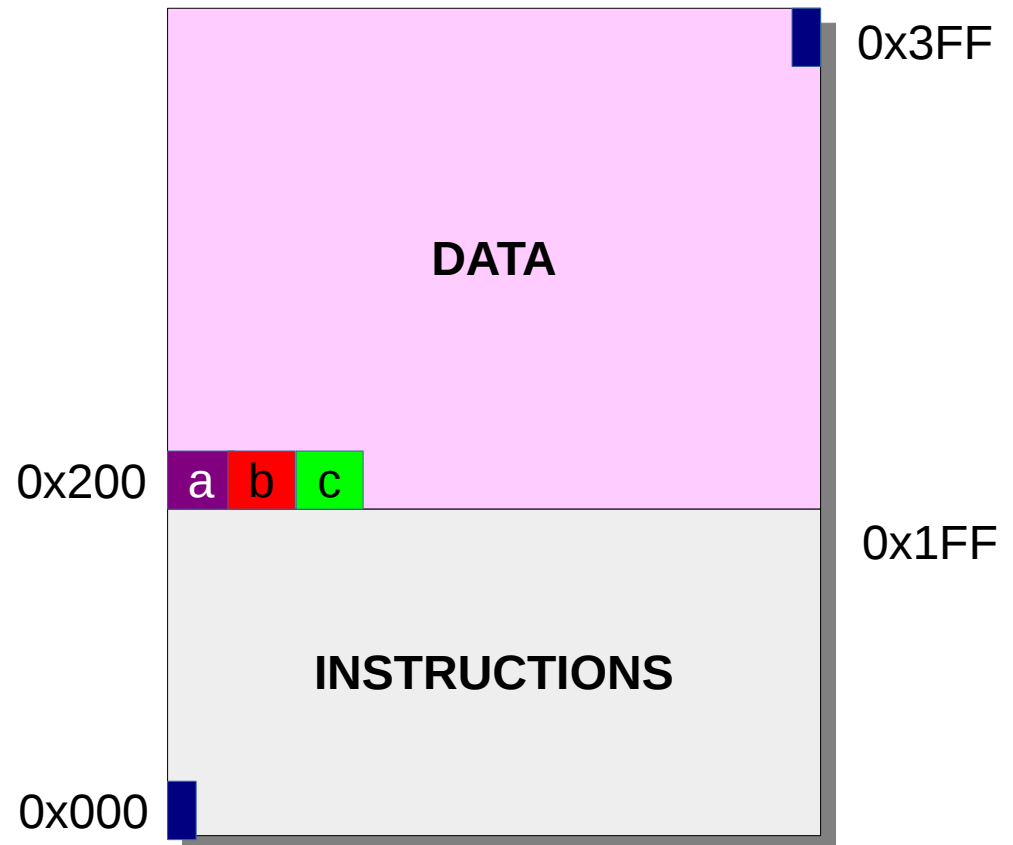
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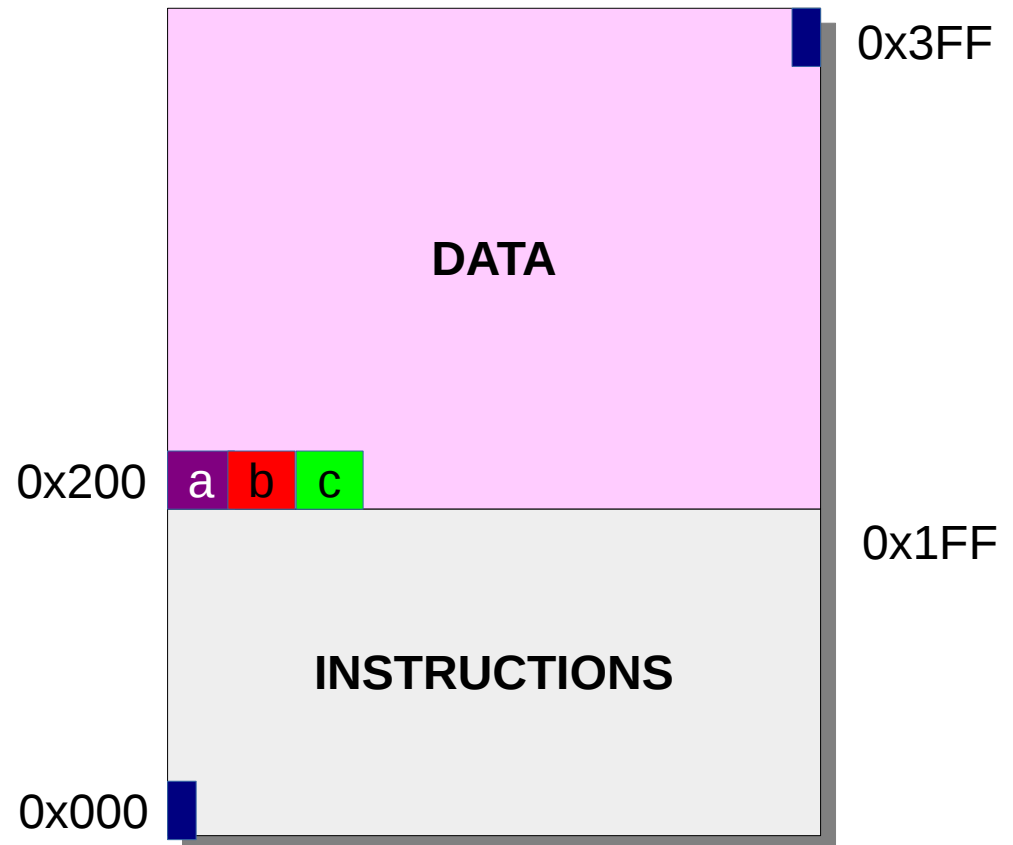
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- Instructions Address Range = 0 to 511 = 0 to 1111111111 = 0x000 to 0x1FF



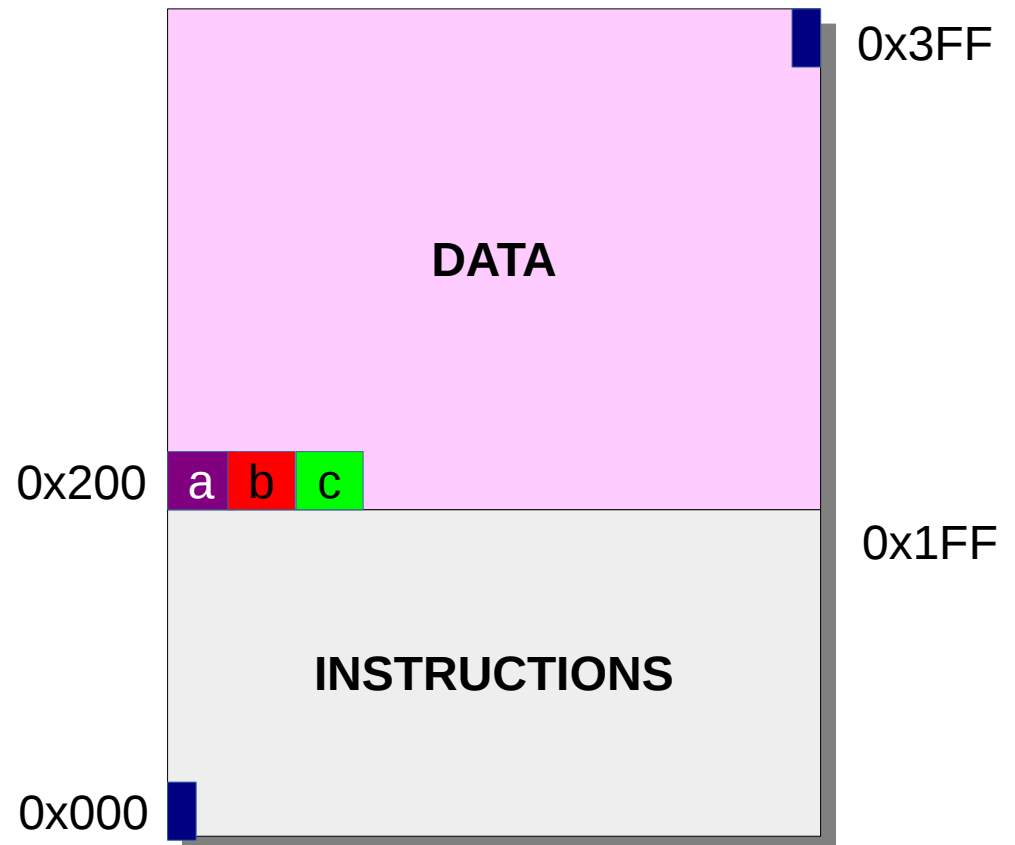
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- Data Address range = 0x200 to 0x3FF



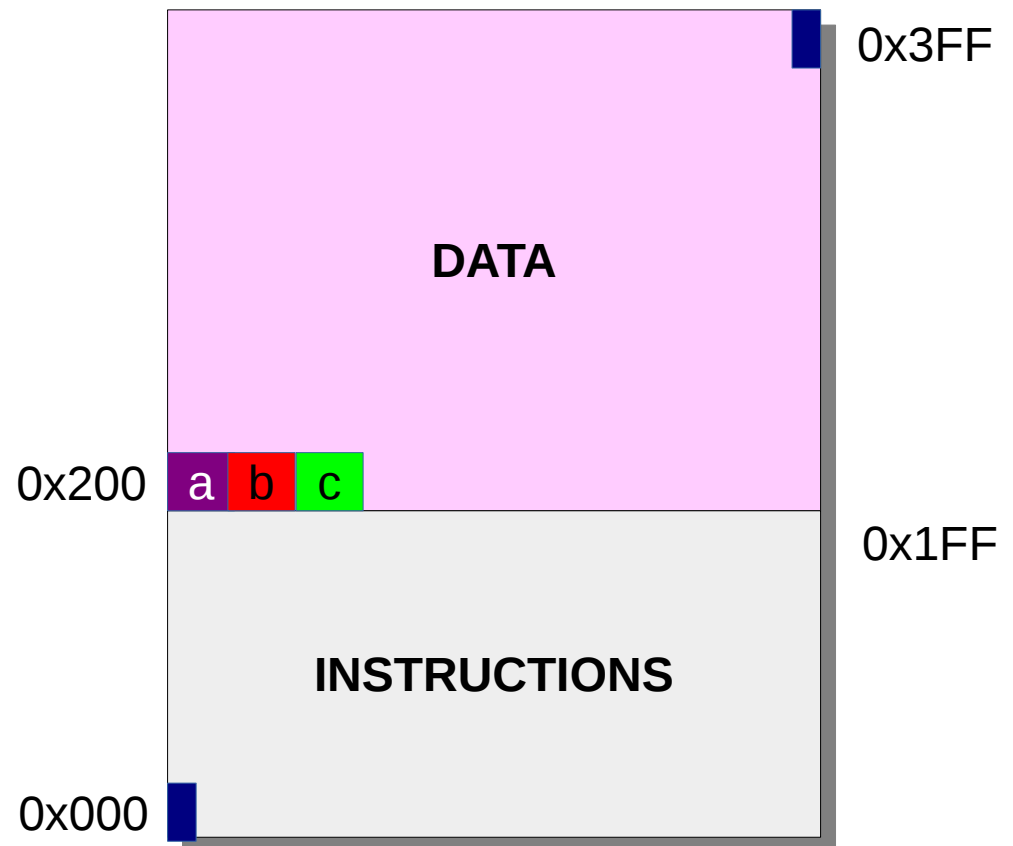
# Data Memory

- Address of first variable = 512; second variable =  $512+4$ ; third variable =  $512+8$ ; and so on.



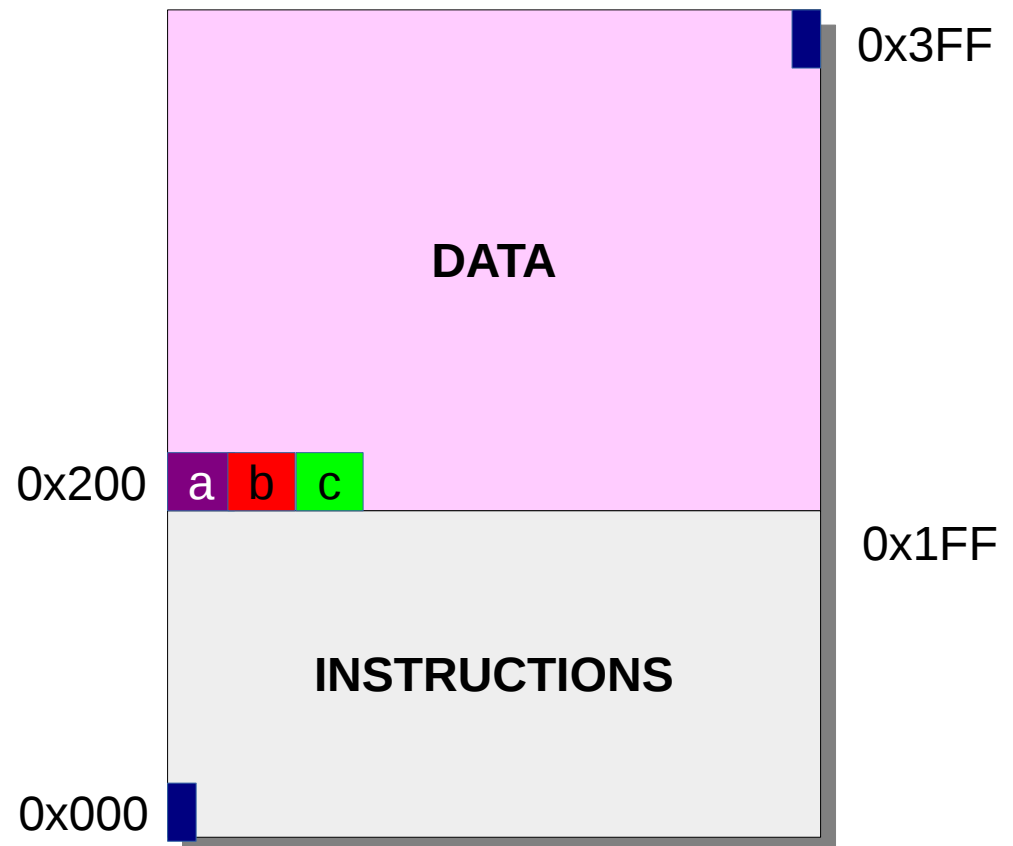
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- Address of first variable = 0x200; second variable =  $0x200+4$ ; third variable =  $0x200+8$ ; and so on.
- What is the address of the 10<sup>th</sup> variable?



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- Address of first variable =  $0x200$ ; second variable =  $0x200+4$ ; third variable =  $0x200+8$ ; and so on.



# Data Addresses

Variable	Decimal Address	
1	512	$0x200 + 0$
2	$512 + 4 = 516$	$0x200 + 1*4$
3	$512 + 8 = 520$	$0x200 + 2*4$
$i^{\text{th}}$	$512 + (i-1)*4$	$0x200 + (i-1)*4$

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- The  $i^{\text{th}}$  variable can be accessed at address

$$Address_i = BaseAddress + i * VariableSize$$

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$$Address_i = BaseAddress + i * VariableSize$$

- Where can such a scheme be useful?

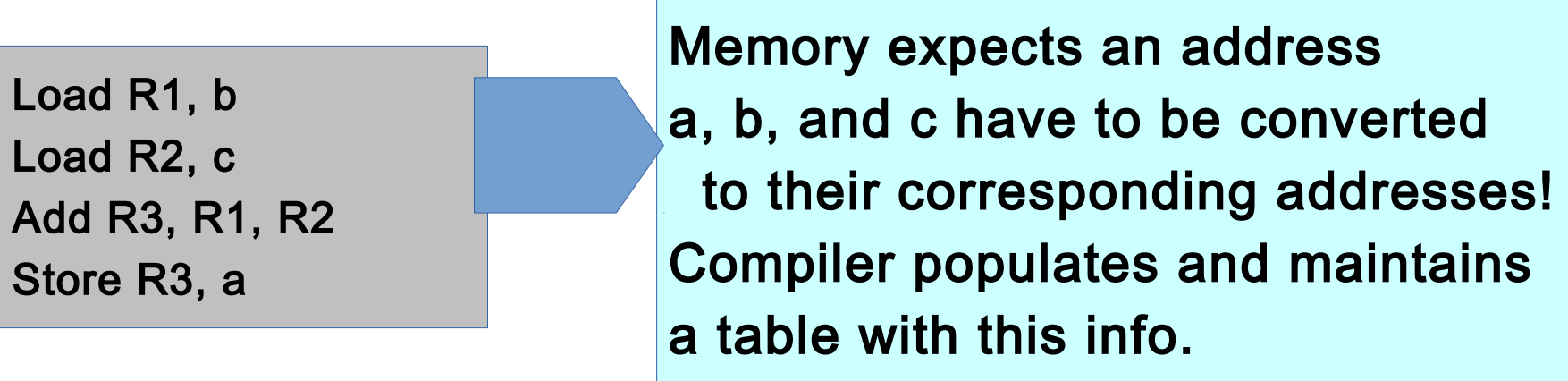
# Assembly Code revisited

Load R1, b  
Load R2, c  
Add R3, R1, R2  
Store R3, a



**Memory expects an address  
a, b, and c have to be converted  
to their corresponding addresses!  
Compiler populates and maintains  
a table with this info.**

# Assembly Code revisited

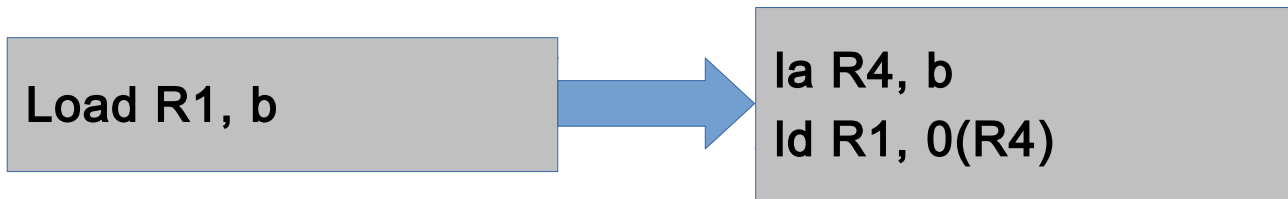


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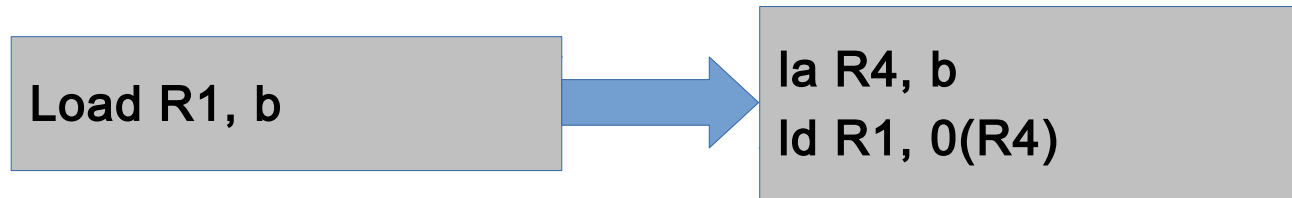
Memory expects an address  
a, b, and c have to be converted  
to their corresponding addresses!  
Compiler populates and maintains  
a table with this info.

- Address calculation and maintenance is one of the jobs of the Compiler

# Correct Code

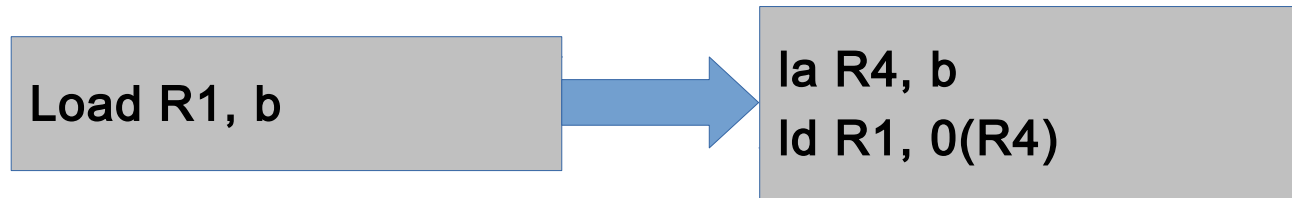


# Correct Code



- R4 contains the Address of variable 'b'

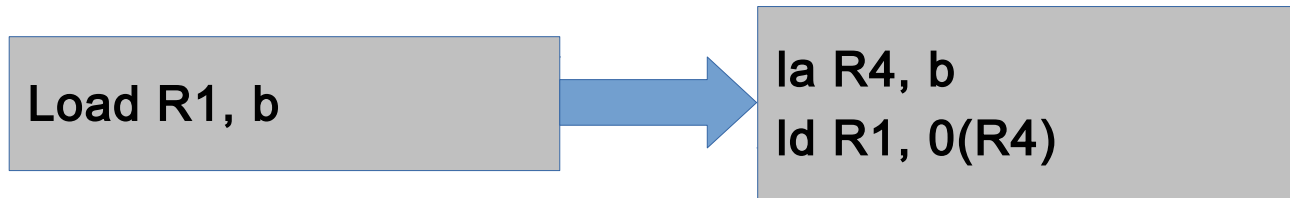
# Correct Code



- R4 contains the Address of variable 'b'
- 0(R4): Address =  $[R4 + 0]$



# Correct Code



- Would these instructions work?
  - ld R1, R4
  - ld R1, (R4)

# MIPS ISA & Assembly Language

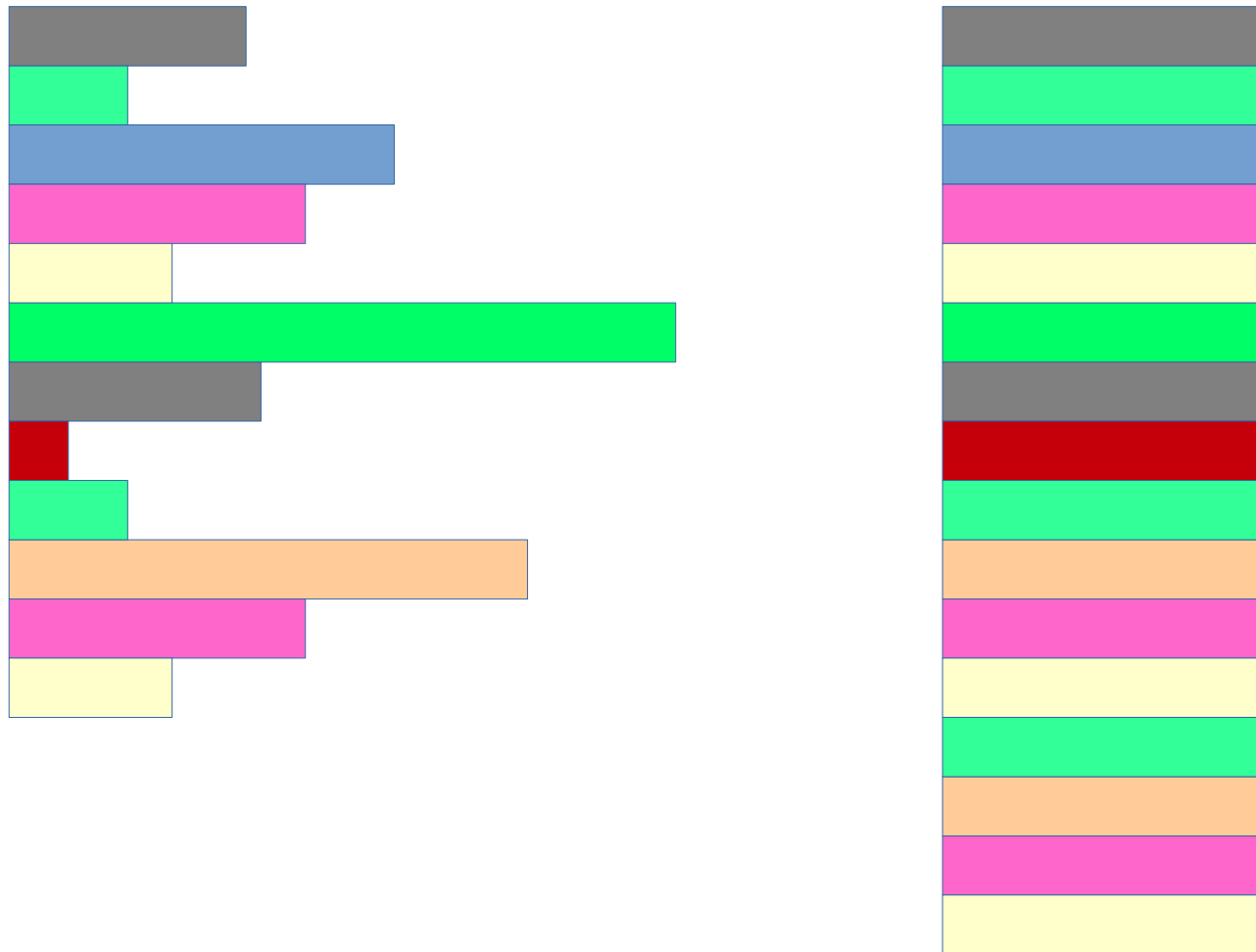
- Simple and elegant ISA

# MIPS ISA & Assembly Language

- Simple and elegant ISA
- One of the first RISC ISAs

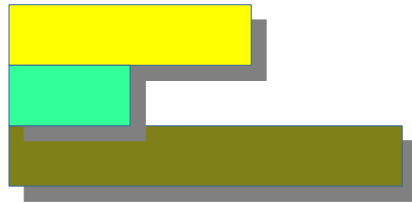
# CISC vs. RISC

- Instruction Sizes



# CISC vs. RISC

**ADD R3, R1, (R2)**



**ADD R3, R1, R2**



# Simple Architecture (1980s)

- IBM 801, Berkely RISC Processor, and Stanford MIPS
- Simple load-store architecture
- Fixed-format 32-bit instructions
- Efficient pipelining
- **Reduced Instruction Set Computers (RISC)**

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# MIPS ISA & Assembly Language

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- Entire ISA at the back of the textbook
- Use the simulator SPIM (xspim, qtspim) for simulating MIPS assembly programs

# Accurate Code


Load R1, b  
Load R2, c  
Add R3, R1, R2  
Store R3, a



la R4, b  
la R5, c  
la R6, a  
ld R1, 0(R4)  
ld R2, 0(R5)  
add R3, R1, R2  
st R3, 0(R6)

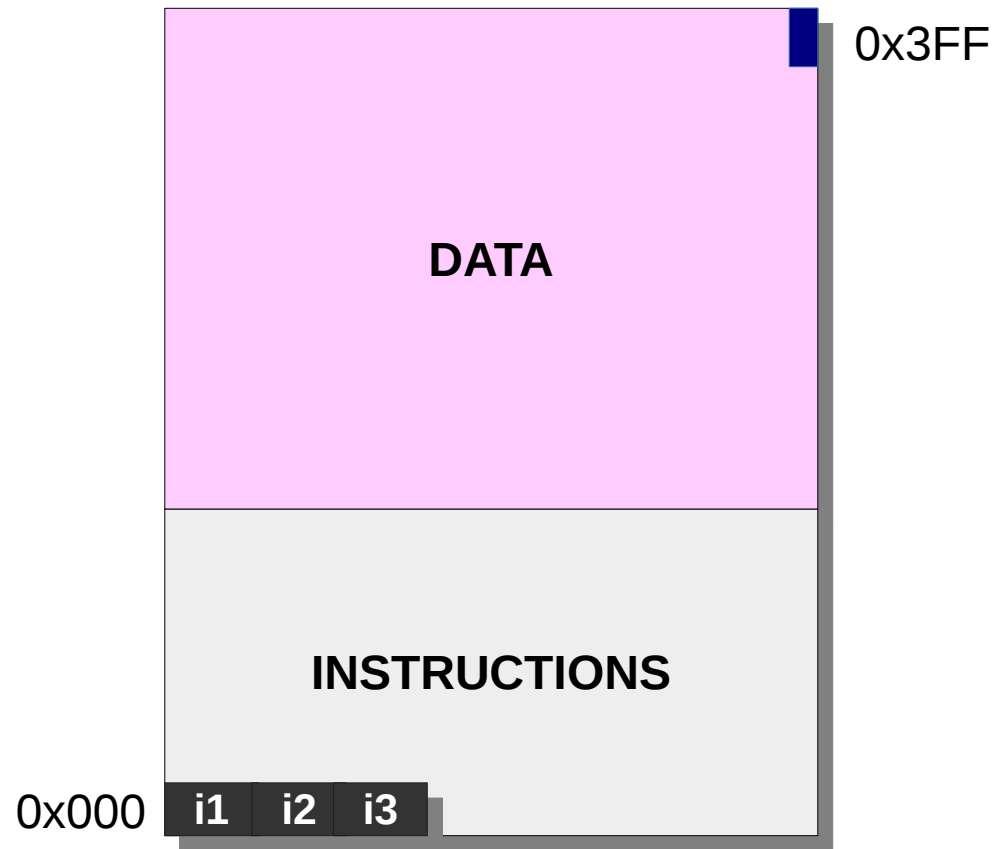
# Accurate MIPS Code

Load R1, b  
Load R2, c  
Add R3, R1, R2  
Store R3, a



```
la $t0, b
la $t1, c
la $t2, a
ld $t3, 0($t0)
ld $t4, 0($t1)
add $t5, $t3, $t4
st $t5, 0($t2)
```

# Instruction Memory



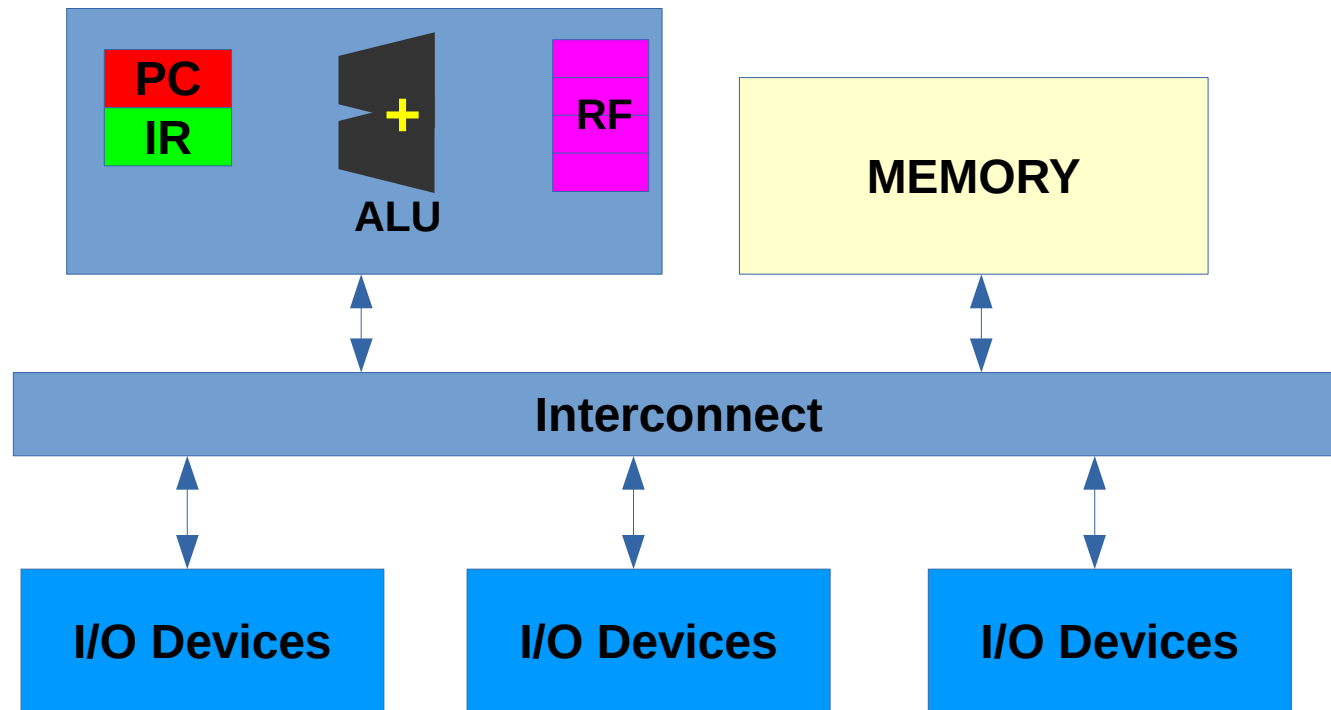
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- The instruction to be executed should be present inside the processor
  - Instruction Register

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- Program Counter keeps track of the next instruction to be executed

# The Computer System



# Datapath and Control Unit

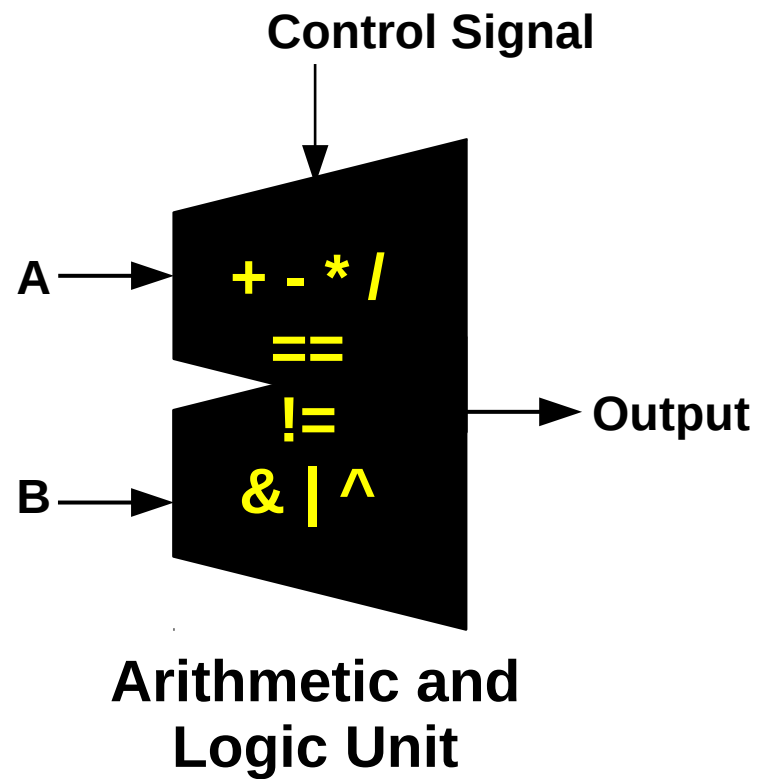
- Datapath: Components in which instructions and data are handled in a processor
  - Register file, ALU, Special registers, ...



# Datapath and Control Unit

- Datapath: Components in which instructions and data are handled in a processor
  - Register file, ALU, Special registers, ...
- Control Unit: Manages these components
  - Ensures correct execution of the instruction

# Control Unit – Example Use



# Computer System

