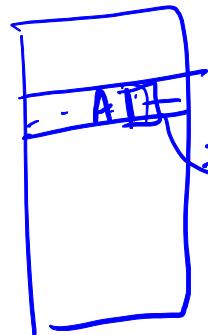


# M2 – Memory Systems

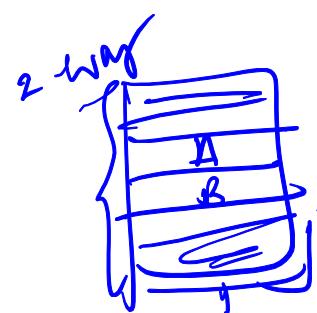
# M2 – Outline

- Memory Hierarchy
- Cache Blocking – Cache Aware Programming
  - config of cache
  - mem accesses
  - cold start, conflict, capacity

reduce DRAM access
- SRAM, DRAM
- Virtual Memory
- Virtual Machines
- Non-volatile Memory, Persistent NVM



load A, load B

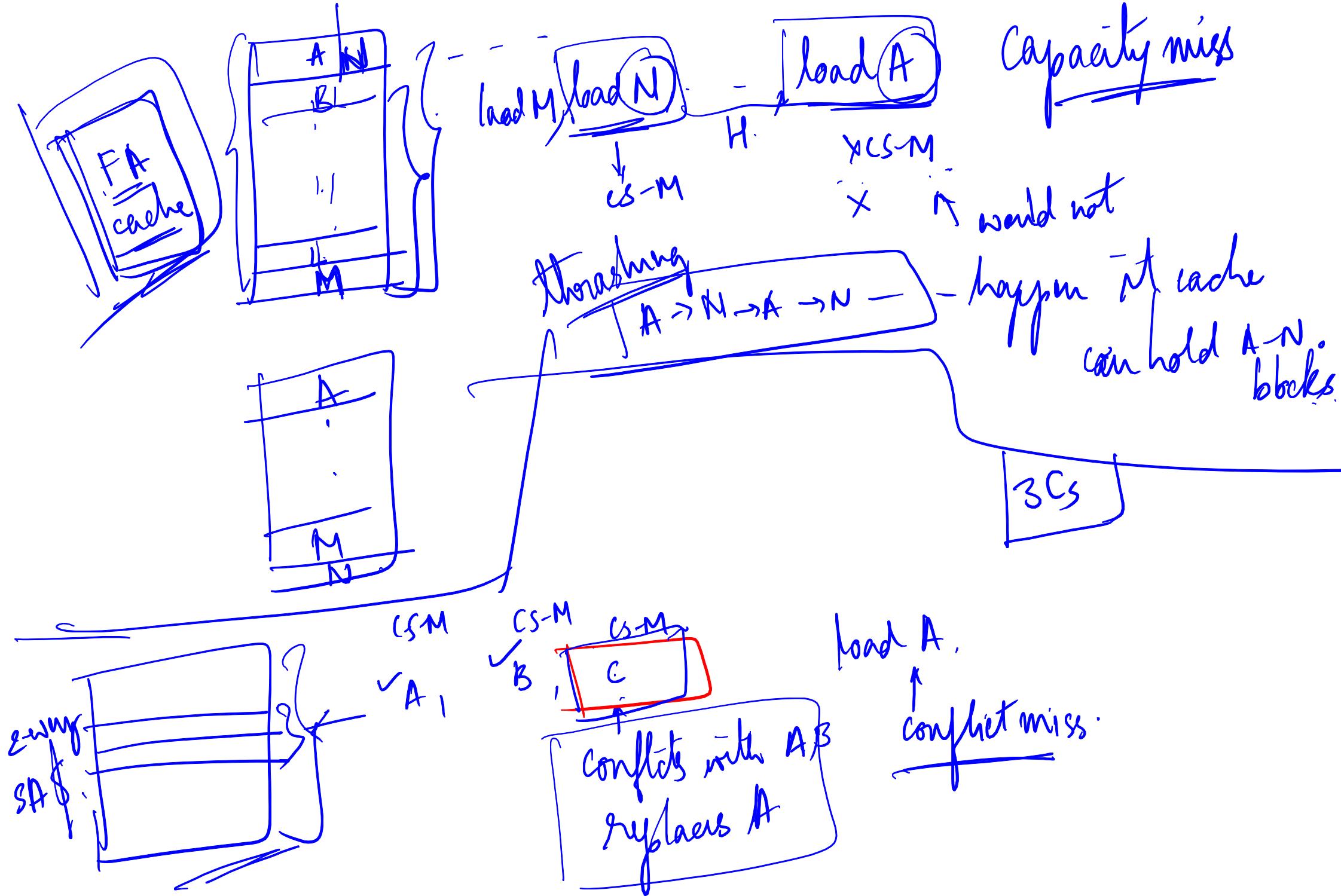


conflict miss

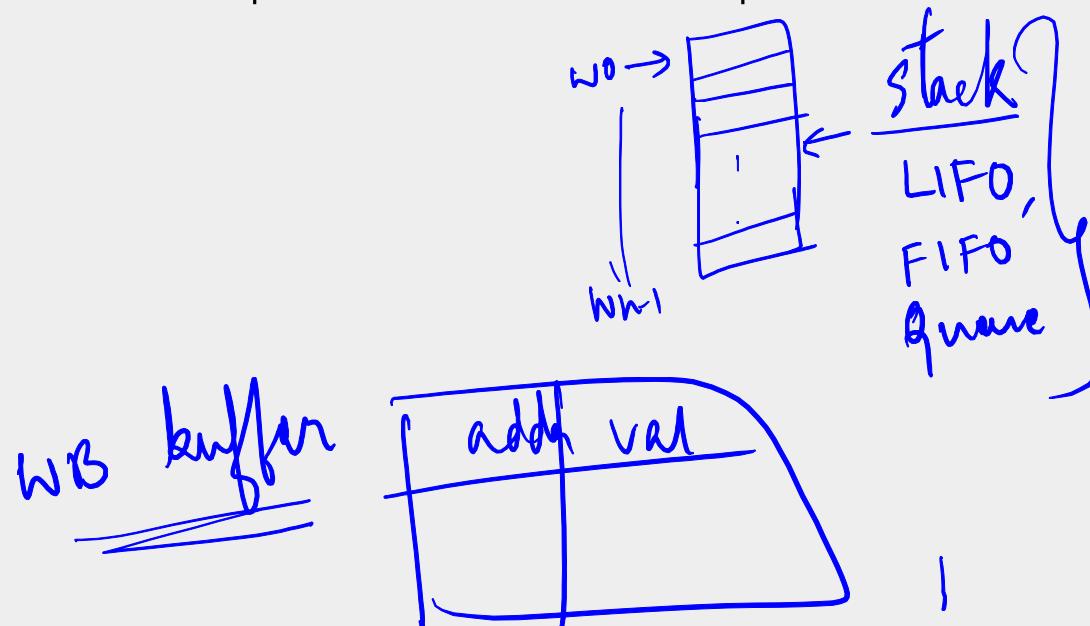
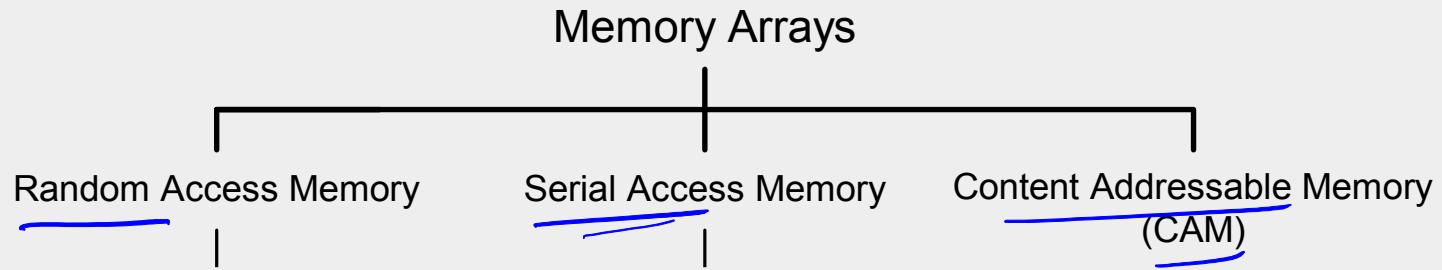
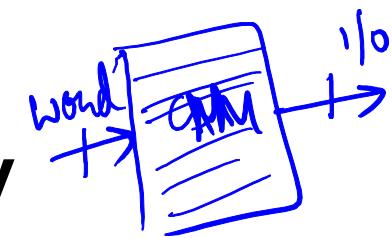
conf. miss  
4-way

FA cache

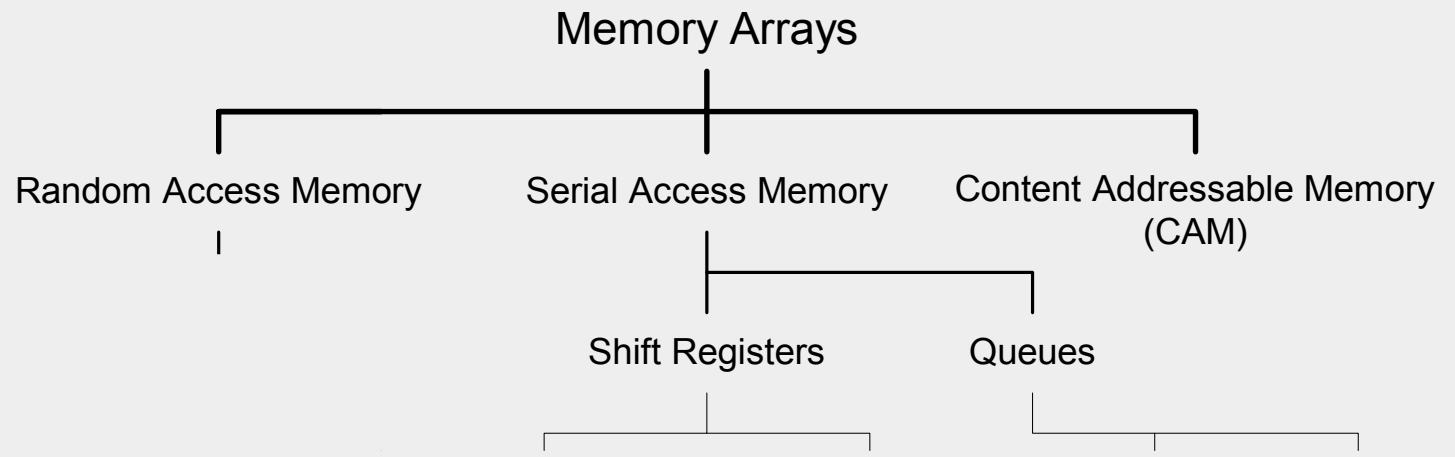
mem access  
(addr errors)



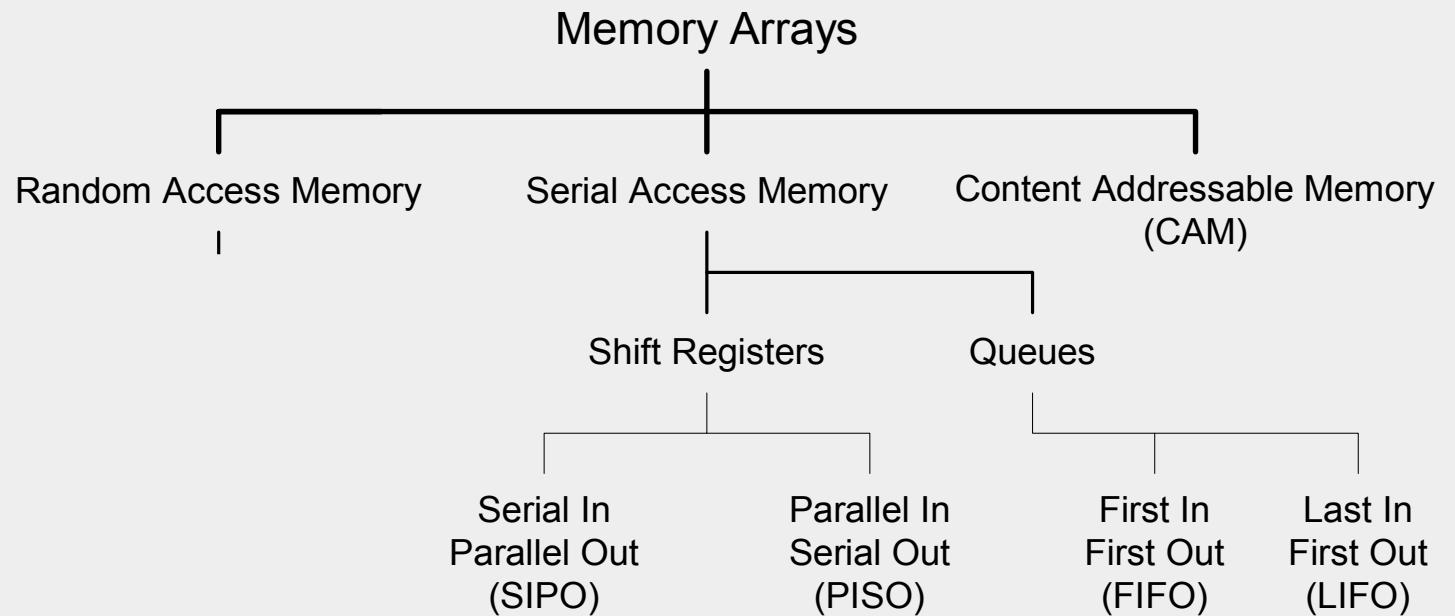
# Memory Technology



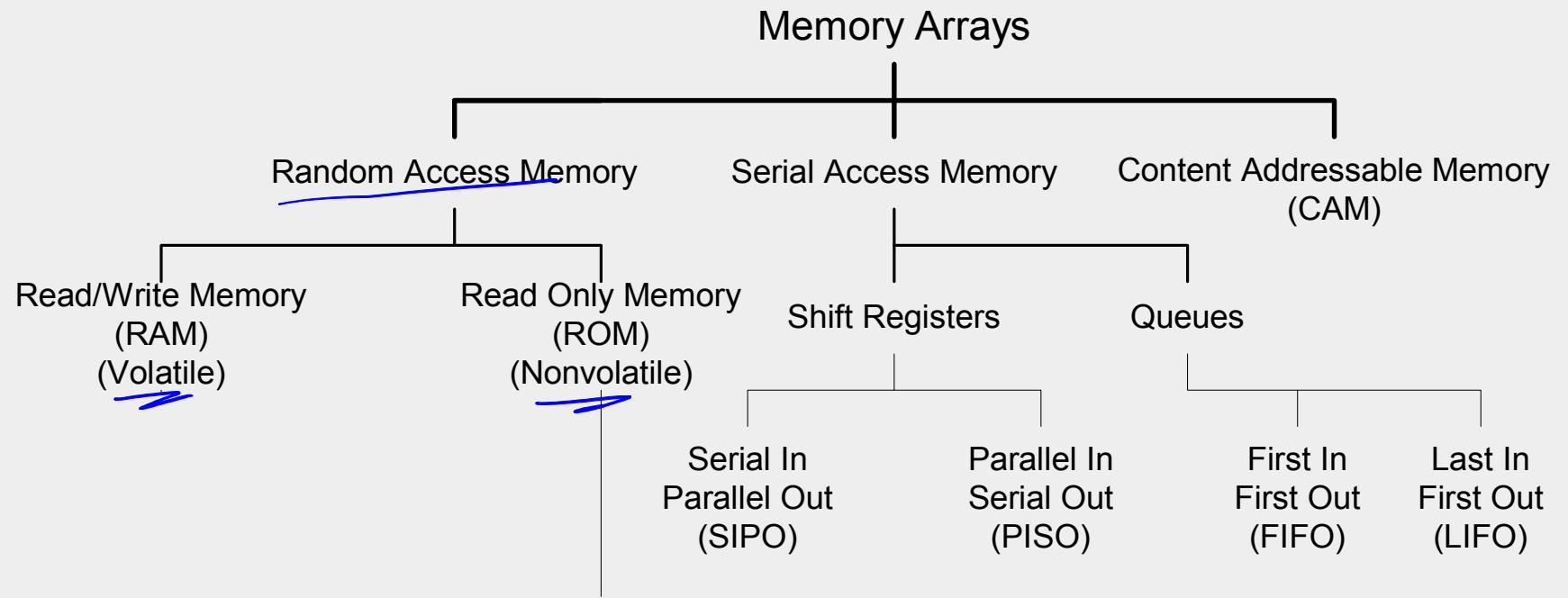
# Memory Technology



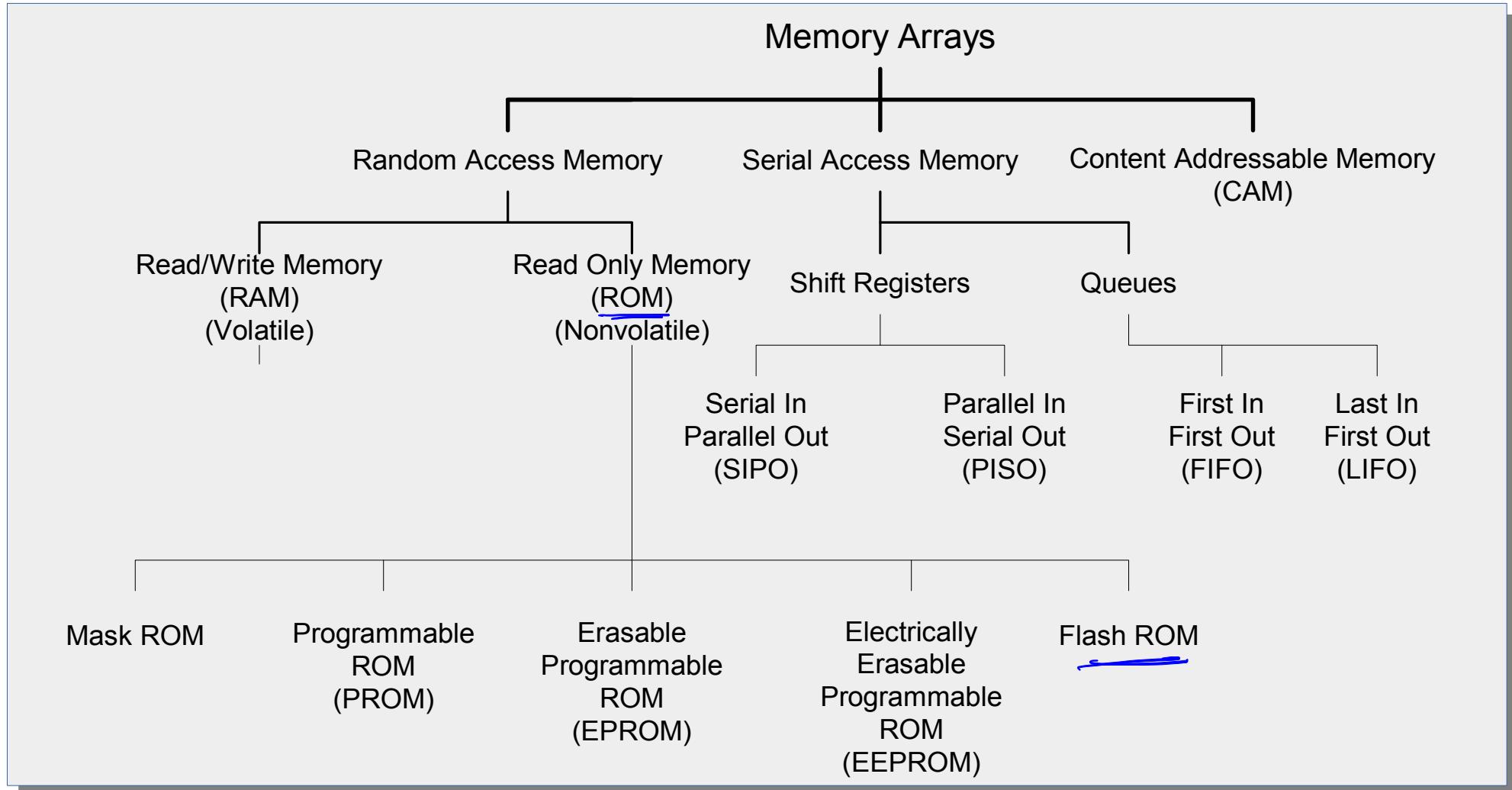
# Memory Technology



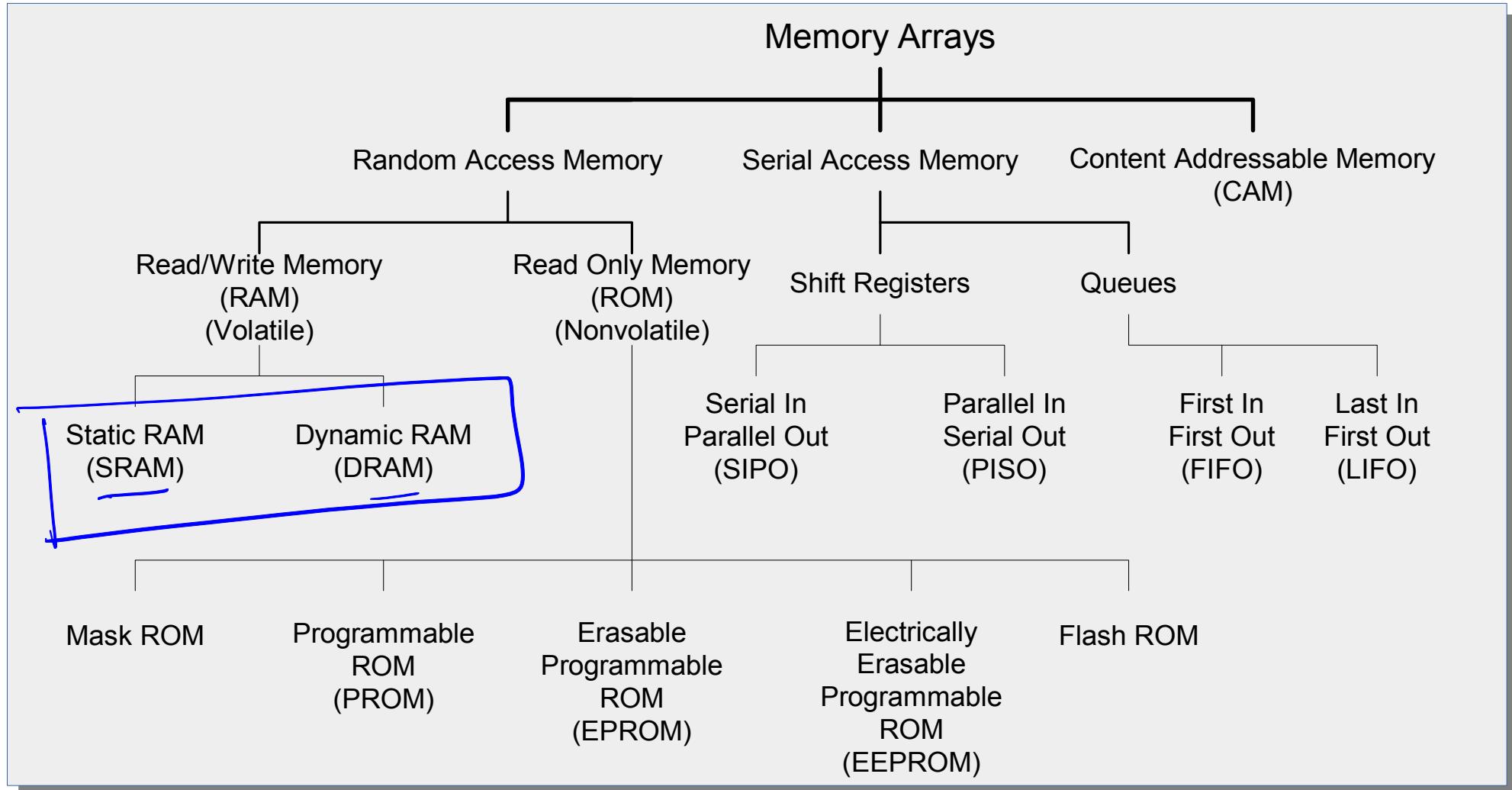
# Memory Technology



# Memory Technology



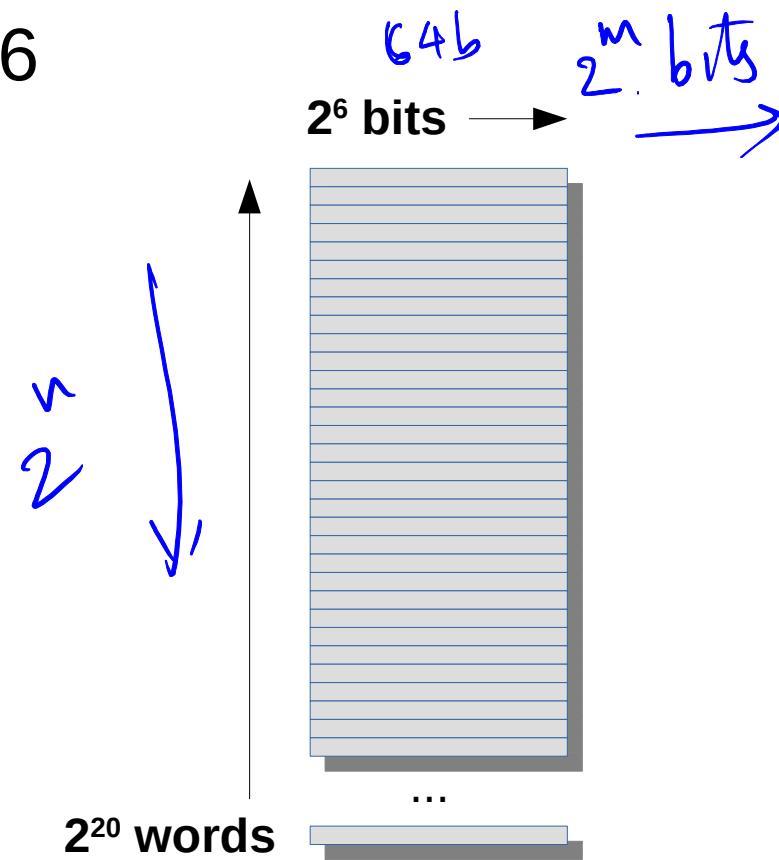
# Memory Technology



# Memory Array

(rows)                    (words)

- Organized as  $2^n$  words of  $2^m$  bits each
  - Usually  $n \gg m$  (1M vs. 64)
  - $n = 20; m = 6$

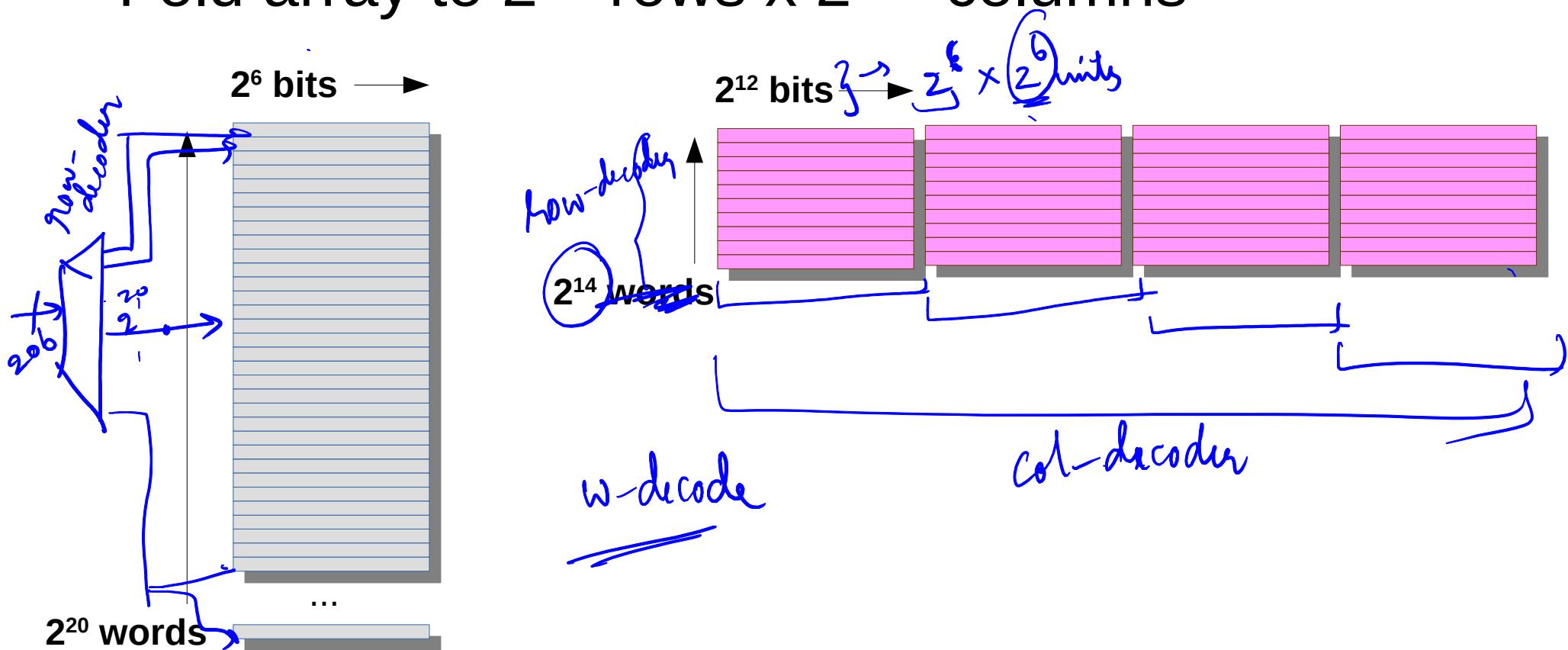


# Memory Array

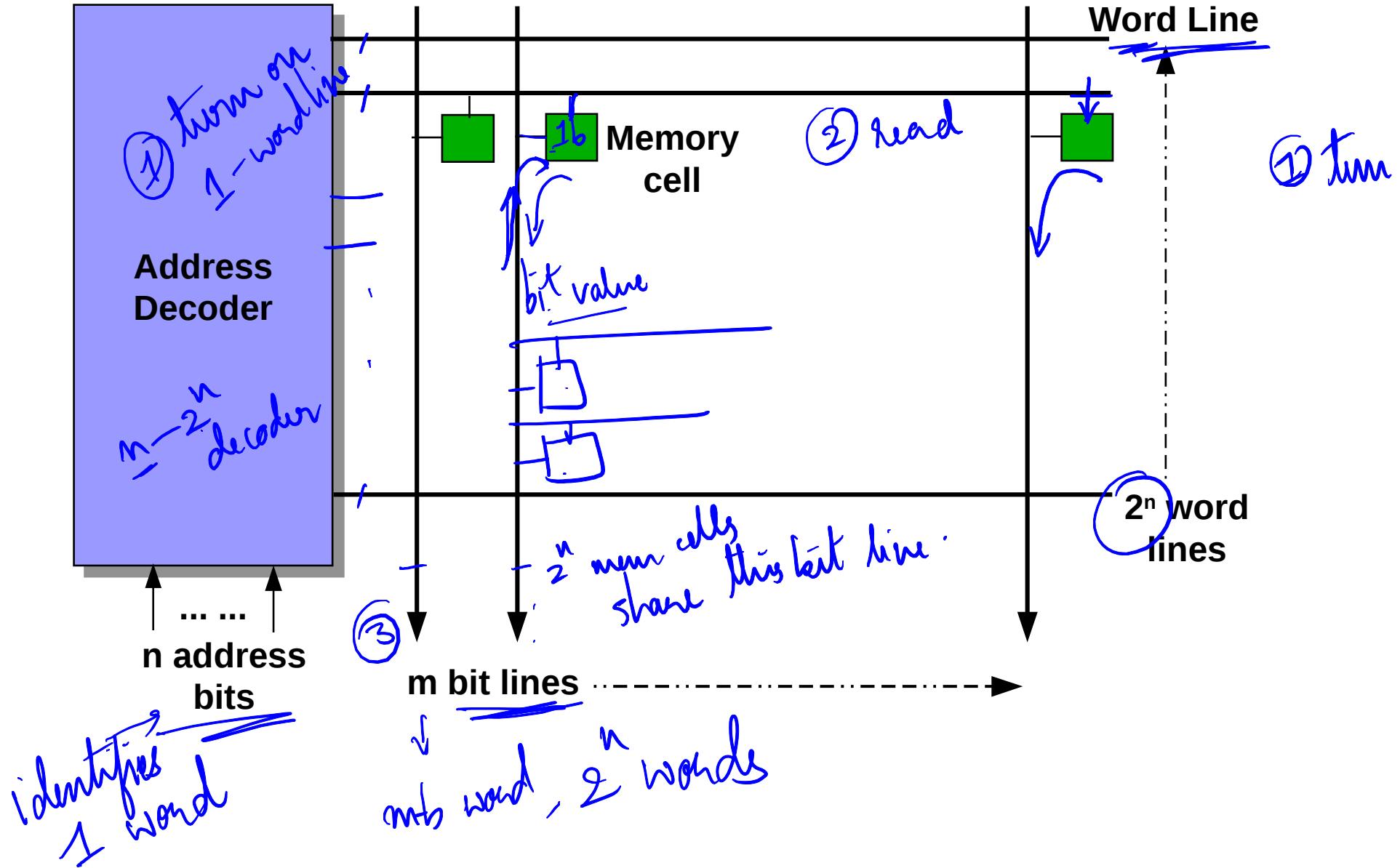
- Organized as  $2^n$  words of  $2^m$  bits each
  - Usually  $n \gg m$  (1M vs. 64)
  -

# Memory Array

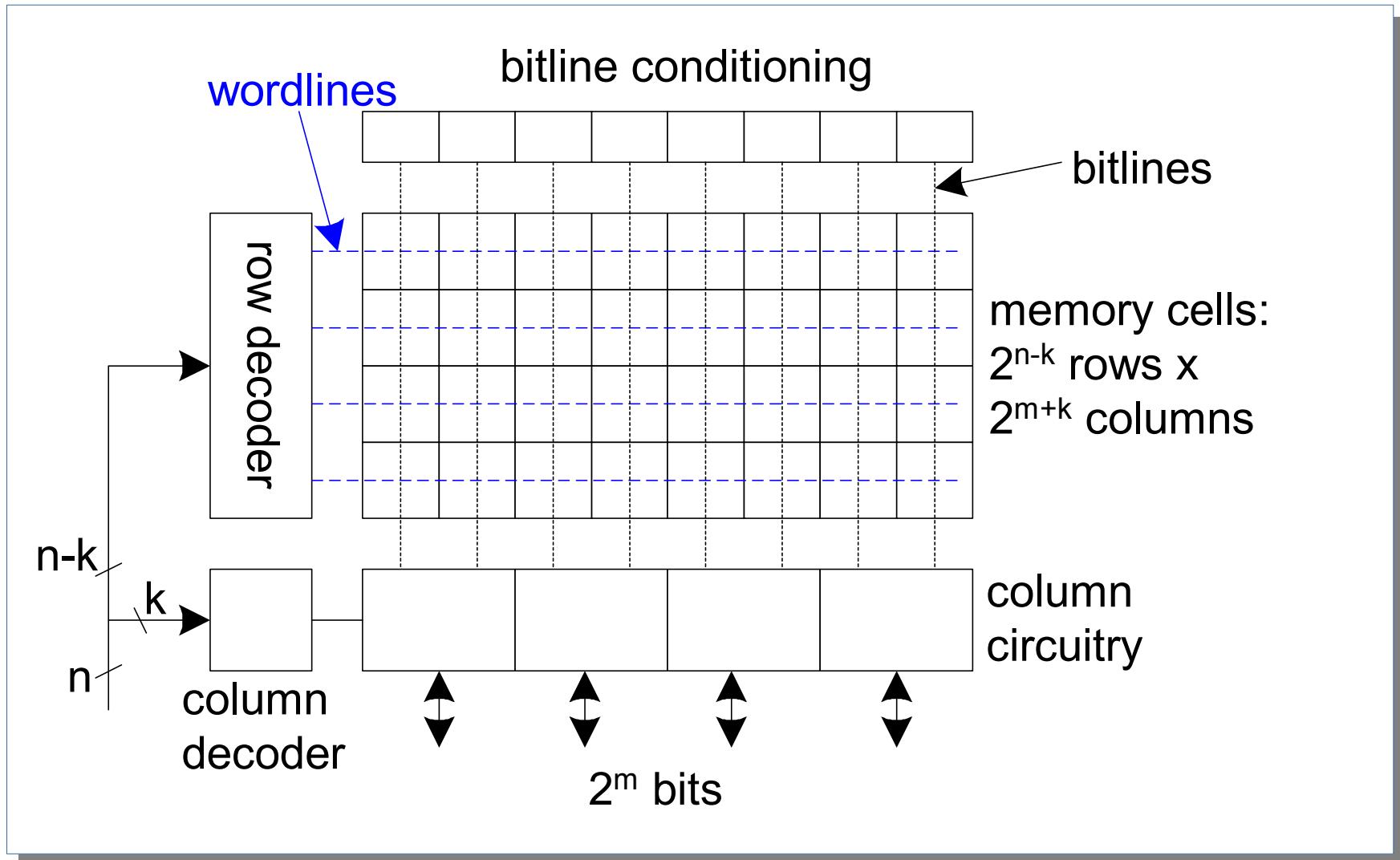
- Organized as  $2^n$  words of  $2^m$  bits each
  - Usually  $n \gg m$  (1M vs. 64)
- Fold array to  $2^{n-k}$  rows x  $2^{m+k}$  columns

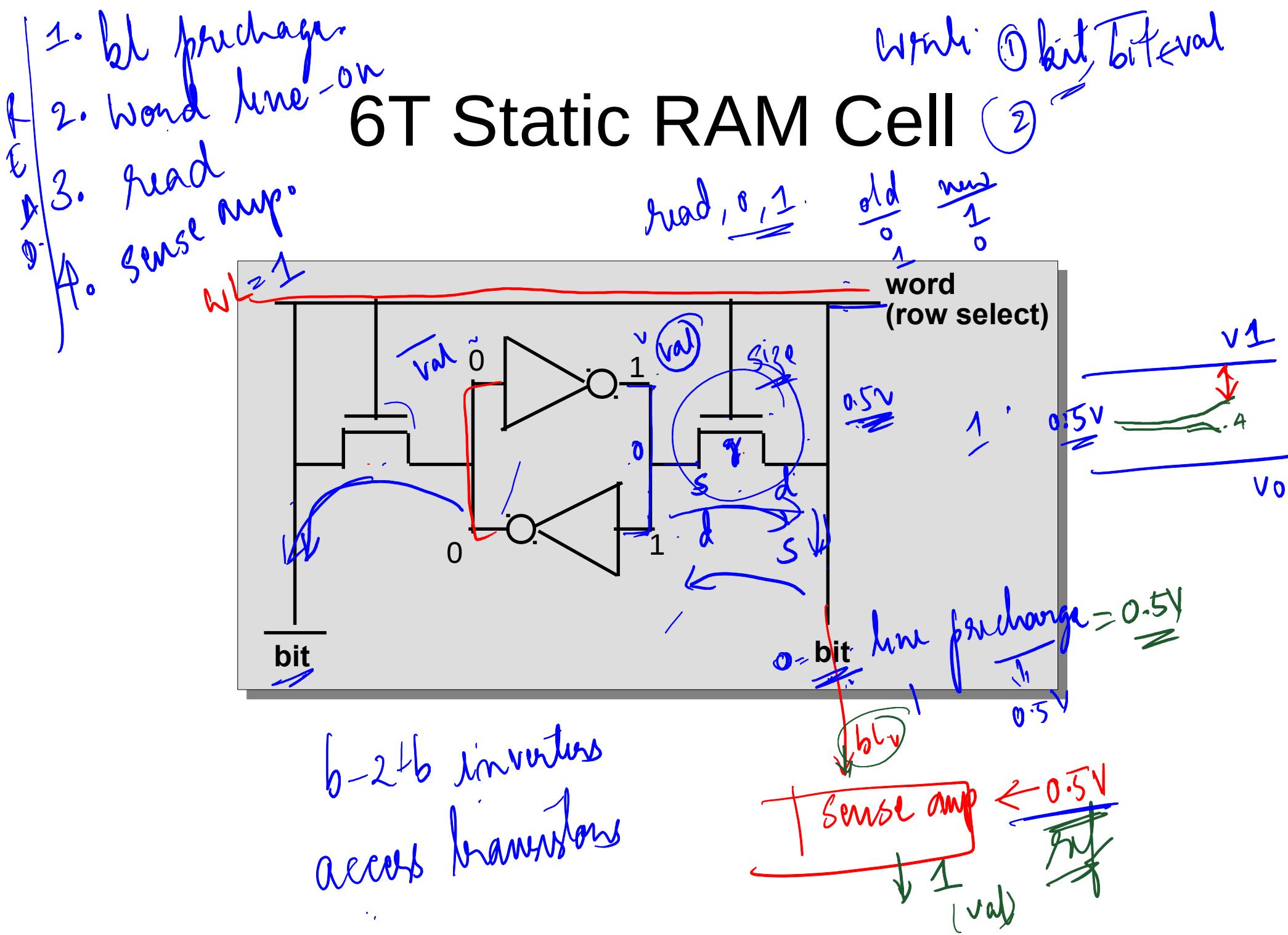


# Memory Array



# Memory Array





# 6T SRAM Cell Operation

- Read:
  - Precharge bit, `bit_b`
  - Raise wordline
  - Cell puts value into bit and its complement in `bit_b`
  - Sense amplifiers sense difference between bit and `bit_b`

# 6T SRAM Cell Operation

- Write:
  - Drive data onto bit, `bit_b`
  - Raise wordline
  - Access transistors set the cell to new state