CO200 – COA. Tutorial 9. Duration: 60 minutes. Max: 3 – Nov – 2016

1. Assume the miss rate of an instruction cache is 2% and the miss rate of the data cache is 4%. If a processor has a CPI of 2 without any memory stalls and the miss penalty is 100 cycles for all misses, determine how much faster a processor would run with a perfect cache that never missed. Assume the frequency of all loads and stores is 36%.

The number of memory miss cycles for instructions in terms of the Instruction count (I) is

$$\text{Instruction miss cycles} = I \times 2\% \times 100 = 2.00 \times I$$

As the frequency of all loads and stores is 36%, we can find the number of memory miss cycles for data references:

$$\text{Data miss cycles} = I \times 36\% \times 4\% \times 100 = 1.44 \times I$$

The total number of memory-stall cycles is 2.00 I + 1.44 I = 3.44 I. This is more than three cycles of memory stall per instruction. Accordingly, the total CPI including memory stalls is 2 + 3.44 = 5.44. Since there is no change in instruction count or clock rate, the ratio of the CPU execution times is

$$\frac{\text{CPU time with stalls}}{\text{CPU time with perfect cache}} = \frac{I \times \text{CPI}_{\text{stall}} \times \text{Clock cycle}}{I \times \text{CPI}_{\text{perfect}} \times \text{Clock cycle}}$$

$$= \frac{\text{CPI}_{\text{stall}}}{\text{CPI}_{\text{perfect}}} = \frac{5.44}{2}$$

The performance with the perfect cache is better by $\frac{5.44}{2} = 2.72$

2. For a DM cache design with a 32-bit address, the following bits of the address are used to access the cache.

Tag	Index	Offset
31-10	9-5	4-0

   a. What is the cache block size (in words)?

Cache Block size = $2^{\text{offset bits}}$
= 2^5 bytes
= 2^3 words
= 8 words

   b. How many entries does the cache have?

Entries = $2^{\text{index bits}} = 2^5 = 32$

   c. What is the ratio between total bits required for such a cache implementation over the data storage bits?

Tag: 22bits
Flag: 3 bits
Bookkeeping bits = $2^5 \times (22 + 3)$ bits
= 25×32 b
Data bits = $2^5 \times 32 \times 8$ b

$$\text{Ratio} = \frac{32 \times (2^5 \times 8 + 25)}{2^5 \times 32 \times 8}$$

Starting from power on, the following byte-addressed cache references are recorded.

Address											
0	4	16	132	232	160	1024	30	140	3100	180	2180

d. How many blocks are replaced?

Four blocks are replaced.

Address	**Hit or Miss**
0	Miss
4	Hit
16	Hit
132	Miss
232	Miss
160	Miss
1024	Miss (Replace)
30	Miss (Replace)
140	Hit
3100	Miss (Replace)
180	Hit
2180	Miss (Replace)

e. What is the hit ratio?

Hit ratio = 4/12 = 0.33

3. Cache access time is proportional to capacity. Assume that main memory accesses take 70ns and that memory accesses are 36% of all instructions. The table shows data for L1 caches attached to 2 processors, P1 and P2.

	L1 Size	L1 Miss Rate	L1 Hit Time
P1	2 KiB	8.0%	0.66ns
P2	4 KiB	6.0%	0.9ns

a. Assuming that the L1 hit time determines the cycle times for P1 and P2, what are their respective clock rates?

Clock rate = $\frac{1}{\text{L1 Hit Time}}$

P1: $\frac{1}{0.66\ \text{ns}} = 1.5152\text{GHz}$

P2: $\frac{1}{0.9\ \text{ns}} = 1.1111\text{GHz}$

b. What is the Average Memory Access Time for P1 and P2?

AMAT = L1 Hit Time + L1 Miss Rate × L1 Miss Penalty

For P1, AMAT = 0.66ns+0.08× 70ns = 6.26 ns

For P2, AMAT = 0.9ns+0.06× 70ns = 5.1 ns

c. Assuming a base CPI of 1.0 without any memory stalls, what is the total CPI for P1 and P2? Which processor is faster?

Number of memory accesses / instruction = 0.36

For P1, L1 miss penalty in cycles is $\frac{70}{0.66}$ = 106.06

For P2, L1 miss penalty in cycles is $\frac{70}{0.9}$ = 77.77

Average memory-stall cycles = Number of memory accesses / instruction×L1 miss rate× L1 miss penalty in cycles

CPI = CPI_{ideal} + average memory-stall cycles

For P1, CPI = 1+0.36× $\frac{8}{100} \times 106.06 = 4.05$ clock cycles
CPU time = IC× CPI × CC = 4.05× $0.66 \times \text{IC} = 2.673 \times \text{IC}$

For P2, CPI = 1+0.36× $\frac{6}{100} \times 77.77 = 2.67$ clock cycles
CPU time = 2.67× 0.9× IC = $2.403 \times$ IC

P2 is faster

Consider the addition of an L2 cache to P1 to presumably make up for its limited L1 cache capacity. Use the L1 cache capacities and hit times from the previous table when solving these problems. The L2 miss rate indicated is local miss rate.

L2 Size	L2 Miss rate	L2 Hit Time
1 MiB	95%	5.62ns

d. What is the AMAT for P1 with the addition of an L2 cache? Is the AMAT better or worse with the L2 cache?

AMAT = L1 Hit Time + L1 Miss Rate× L1 Miss Penalty
L1 Miss Penalty = L2 Hit Time + L2 Miss Rate × L2 Miss Penalty
For P1 with the L2 cache,
AMAT = 0.66 ns + 0.08×(5.62 ns + 0.95 × 70 ns) = 6.42 ns

AMAT is worse with the L2 cache.

e.Assume a base CPI of 1.0 without any memory stalls, what is the total CPI for P1 with the addition of an L2 cache?

CPI = $1 + 0.36 \times 0.08 \times (\frac{5.62}{0.66} + 0.95 \times \frac{70}{0.66})$

CPI = 4.14 clock cycles

f.Which processor is faster, now that P1 has an L2 cache? If P1 is faster, what miss rate would P2 need in its L1 cache to match P1’s performance? If P2 is faster, what miss rate would P1 need in its L1 cache to match P2’s performance?