CO200 – COA. Tutorial 1. 2 – Aug – 2017

1. Against each of the following design tasks, state whether the task is an Organizational challenge or an Architectural task. (Write “A” or “O” against the task). (3)

Design Decision/Task/Challenge	*O/A*
Support for the XNOR instruction in the processor.	
Completing a cache access under 2.0 ns.	
Design a new processor to support the IA-32 ISA.	
Support for the base-index addressing mode.	
The next generation processor should use a special register - “Accumulator” to store the result of every ALU operation.	
Decision to build a 64 bit adder using 2 32bit adders or using 4 16 bit adders.	

2. Write the equivalent assembly code for the following two high level language statements. Bear in mind that the ALU can only receive two inputs and produce one output. (2)
a = b + c;
d = b + c + a;

3. The size of an address to a word-addressable memory is 16 bits. The size of the memory is _____ Bytes . (1)

4. A system has 1 GB of memory. During a program execution, the first 2/5 portion of the memory is used to hold the instructions and the rest to hold the data. (3)
(a) The address range for Instructions is :

(b) The address range for Data is :

(c) Your program declares an array of double precision floating point numbers (double A[100];). The address of the A[12] is:

6. A processor executes one instruction in 3 clock cycles. A program containing 1.5 Million instructions completes in 1.8 ms. What is the processor's operating frequency (2)?

7. Identify the input and the output operands in the following instructions: (3)

Instruction	Input Operands	Output operands
ADD R1, R2, R3		
LOAD R4, 0(R5)		
STORE R6, 0(R7)		

8. Base addres of the integer array A is present in $s2. Contents of the variable h is in $s3. Write the MIPS equivalent code for: A[12] = h + A[8];

9. Convert 16 bit binary versions of +2 and -2 into 32 bit 2s complement binary numbers.

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Rough Work