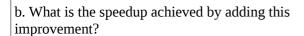
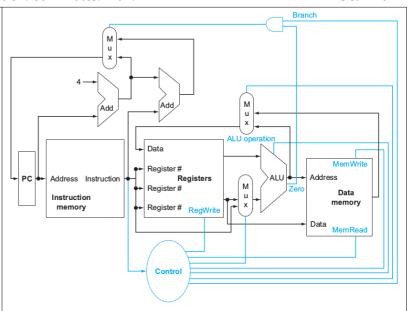
- 1. When processor designers consider a possible improvement to the processor datapath, the decision usually depends on the cost/performance trade-off. Assume that we are starting with a datapath from the following Figure, where I-Mem, Add, Mux, ALU, Regs, D-Mem, and Control blocks have latencies of 400 ps, 100 ps, 30 ps, 120 ps, 200 ps, 350 ps, and 100 ps, respectively, and costs of 1000, 30, 10, 100, 200, 2000, and 500, respectively. Consider the addition of a multiplier to the ALU. This addition will add 300 ps to the latency of the ALU and will add a cost of 600 to the ALU. The result will be 5% fewer instructions executed since we will no longer need to emulate the MUL instruction.
- a. What is the clock cycle time with and without this improvement?





c. Compare the cost/performance ratio with and without this improvement.

2. Problems in this exercise assume that logic blocks needed to implement a processor's datapath have the following latencies:

I-Mem	Add	Mux	ALU	Regs	D-Mem	Sign-Extend	Shift-Left-2
200ps	70ps	20ps	90ps	90ps	250ps	15ps	10ps

- a. If the only thing we need to do in a processor is fetch consecutive instructions, what would the cycle time be?
- b. Consider a datapath similar to the one built in the class, but for a processor that only has one type of instruction: conditional PC-relative branches. What would the cycle time be for this datapath?
- c. Which kinds of instructions require Shift left -2?

3. The breakdown of executed instructions is as follows:

a	ld	addi	not	beq	lw	sw
20)%	20%	0%	25%	25%	10%

a. In what fraction of all cycles is the data memory used?

b. In what fraction of all cycles is the input of the sign-extend circuit needed? What is this circuit doing in cycles in which its input is not needed?

- 4. Assume that individual stages of the datapath have the following latencies: Assume that instructions executed by the processor are broken down as follows:
- a. What is the clock cycle time of the datapath?

IF .	ID	EX	MEM	WB
250ps	350ps	150ps	300ps	200ps

alu	beq	lw	sw
45%	20%	20%	15%

b. What is the total latency of an LW instruction in the processor datapath?

5. Complete the multiplication steps as seen in a standard multiplier.

Iteration	ete the multiplication steps as seen in Step	Multiplier	Multiplicand	Product
0	Initial values	0110	10010010	
1	1a: $1 \Rightarrow \text{Prod} = \text{Prod} + \text{Mcand}$			
	2: Shift left Multiplicand			
	3: Shift right Multiplier			
2				
3				
4				

6. In this exercise we examine in detail how an instruction is executed in a single-cycle datapath. Problems in this exercise refer to a clock cycle in which the processor fetches the following instruction word: 10101100011000100000000000010100.

Assume that data memory is all zeros and that the processor's registers have the following values at the beginning of the cycle in which the above instruction word is fetched:

R0	R1	R2	R3	R4	R5	R6	R8	R12	R31
0	-1	2	-3	-4	10	6	8	2	-16

R0	R1	R2	R3	R4	R5	R6	R8	R12	R31
0	-1	2	-3	-4	10	6	8	2	-16
a. What are	the outputs o	of the sign-ex	ktend and the	e jump "Shif	t left 2" unit	for this inst	ruction word	!?	
b. What are	the values o	f the ALU co	ontrol unit's	inputs for thi	is instruction	n?			
c. What is th	e new PC ac	ldress after t	his instructio	on is execute	d?				
d. For each l	Mux, show t	he values of	its data outp	out during the	e execution o	of this instru	ction and the	ese register v	alues.
e. For the Al	LU and the t	wo add units	s, what are th	neir data inpu	ut values?				
f. What are t	he values of	all inputs fo	or the "Regis	ters" unit?					