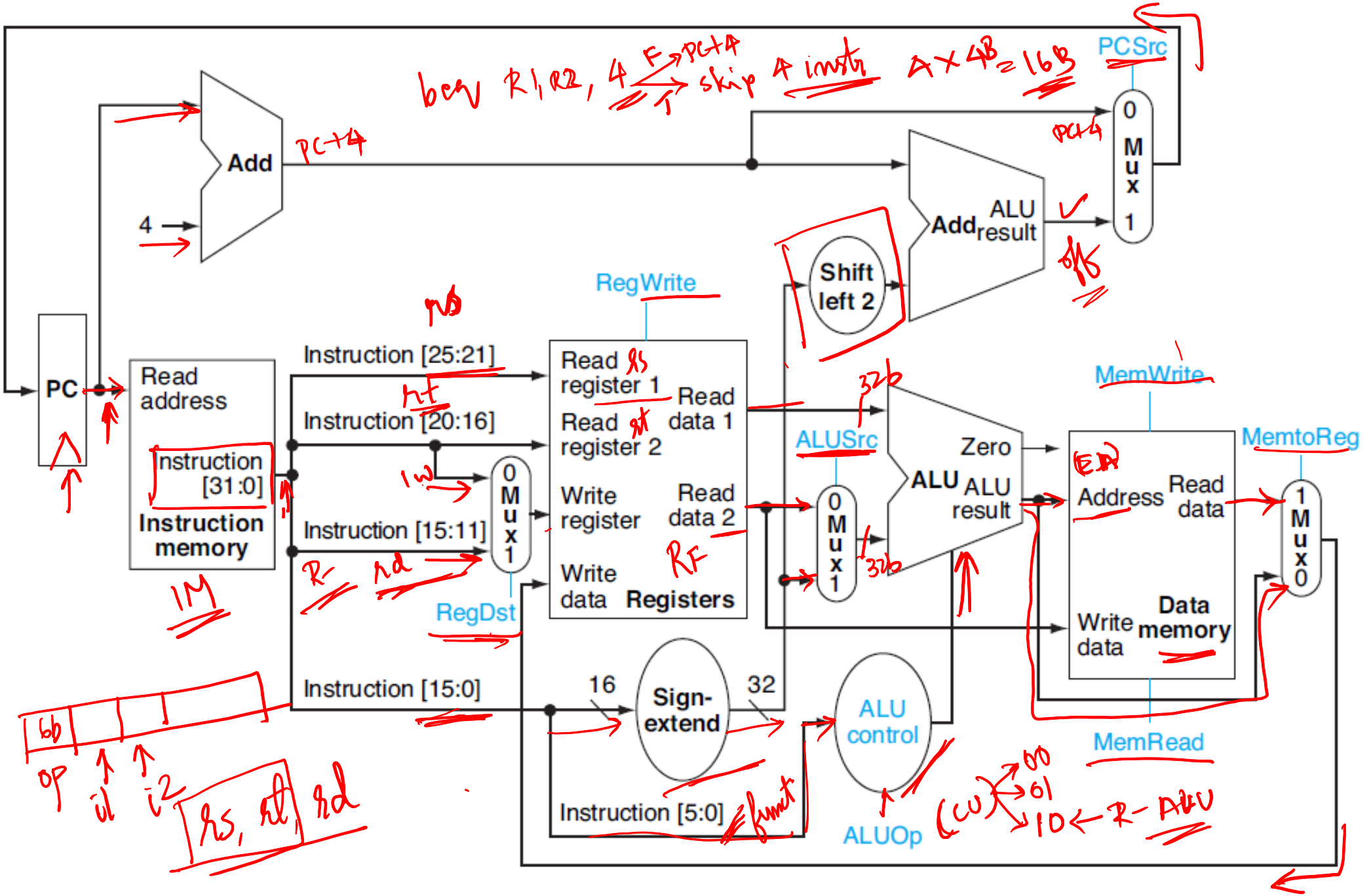
The MIPS Processor Datapath

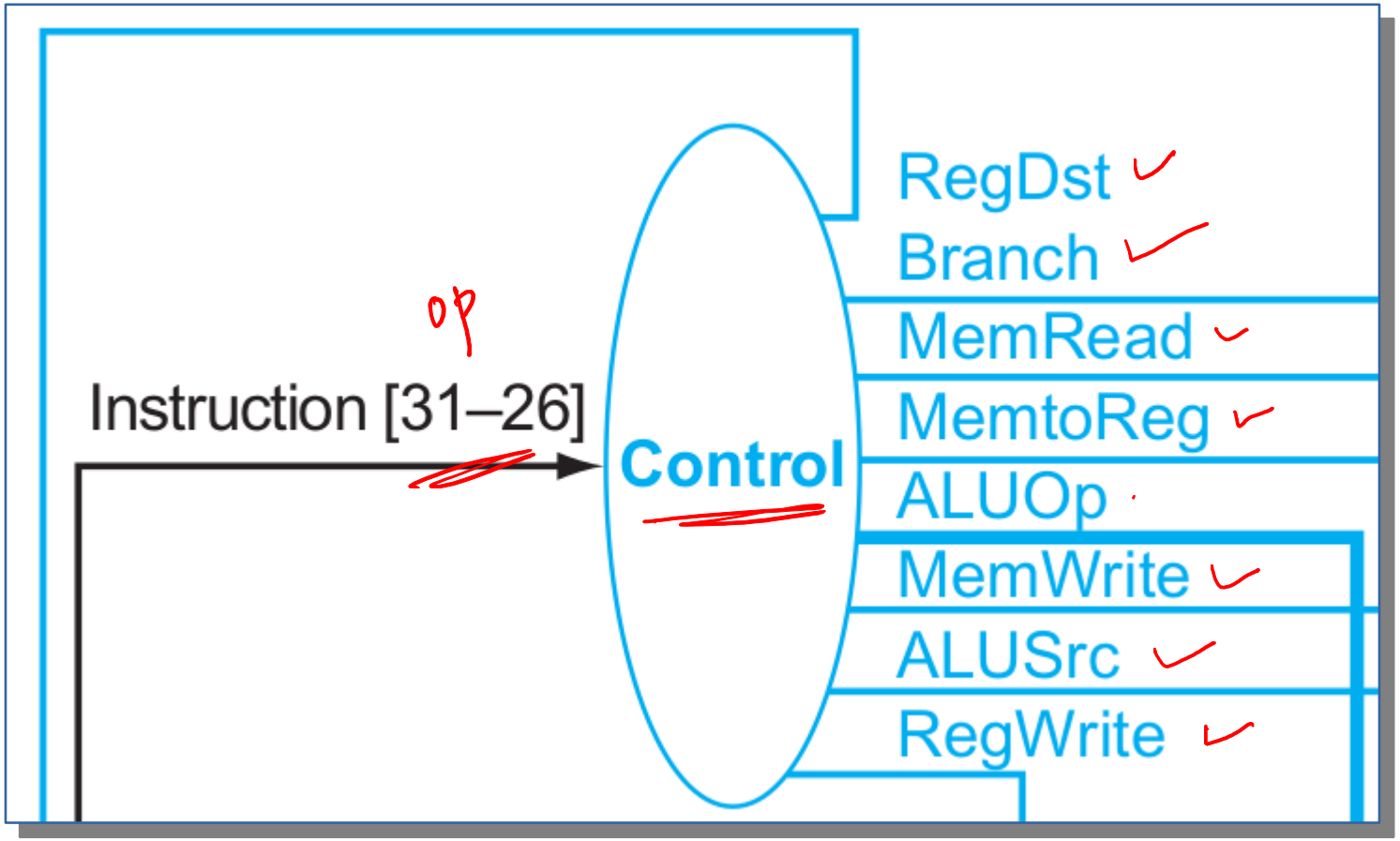
Module Outline

- MIPS datapath implementation
  - Register File, Instruction memory, Data memory
- Instruction interpretation and execution.
- Combinational control
- Assignment: Datapath design and Control Unit design using SystemC.

MIPS Datapath and Control Lines

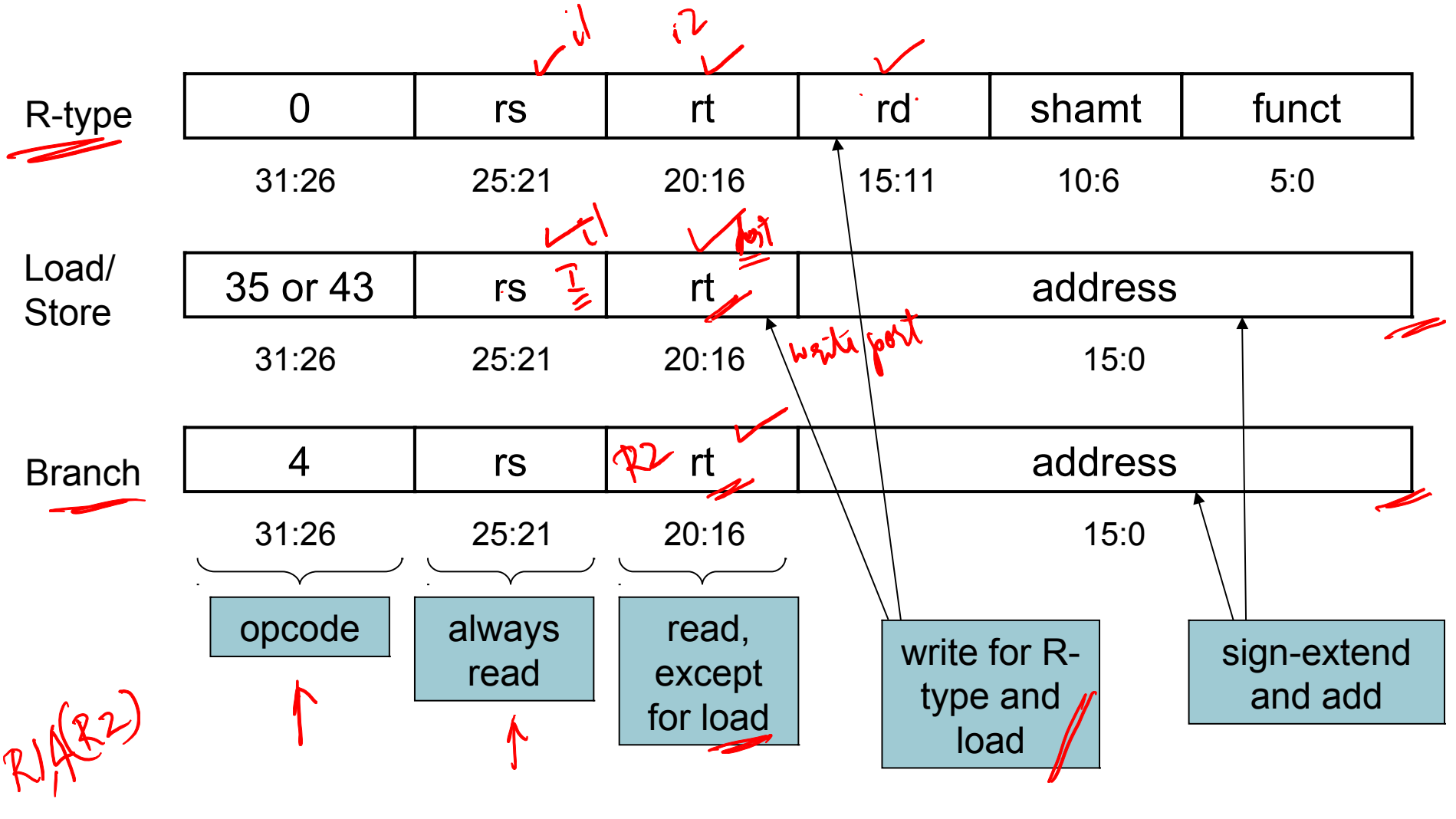


Control Unit

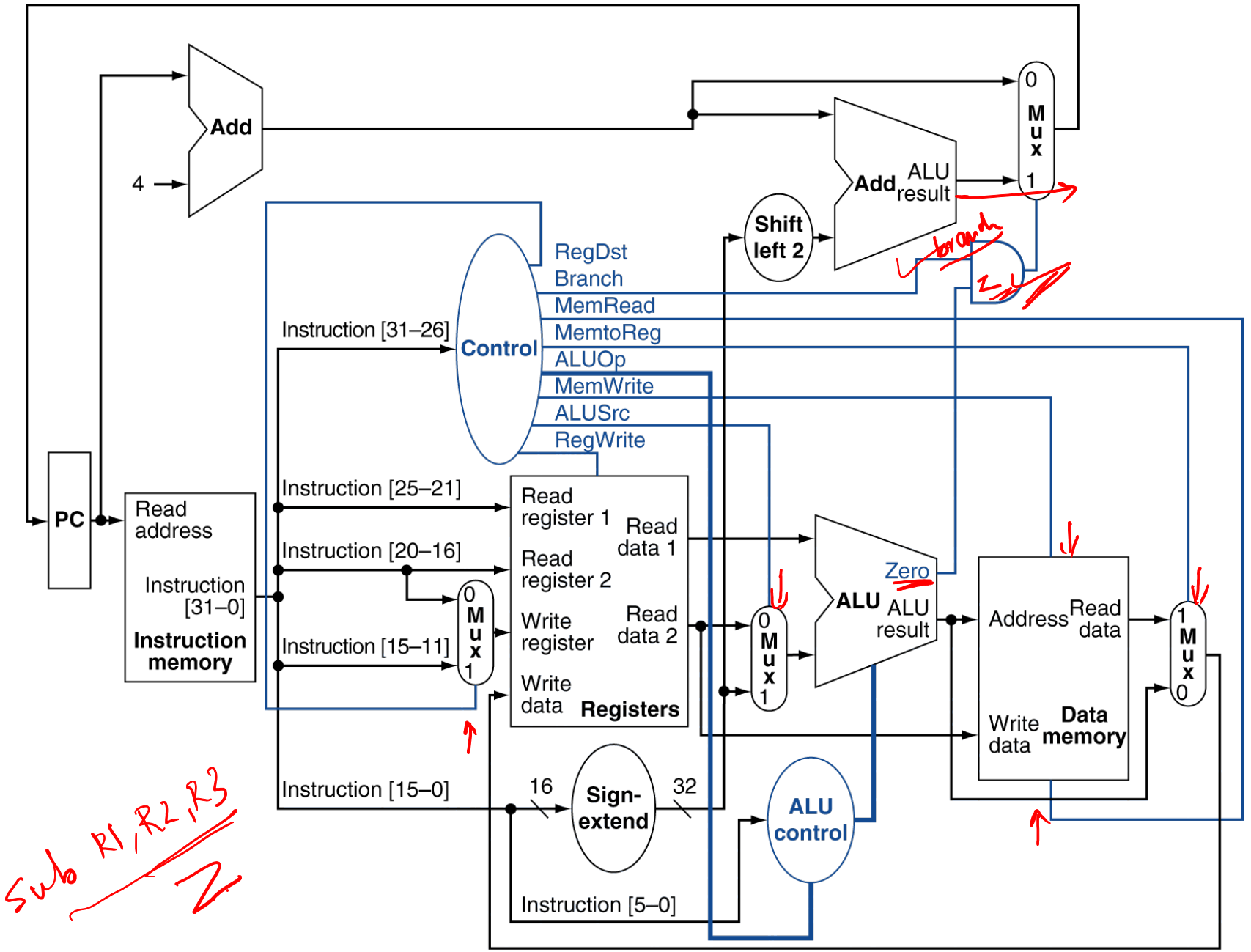


The Main Control Unit

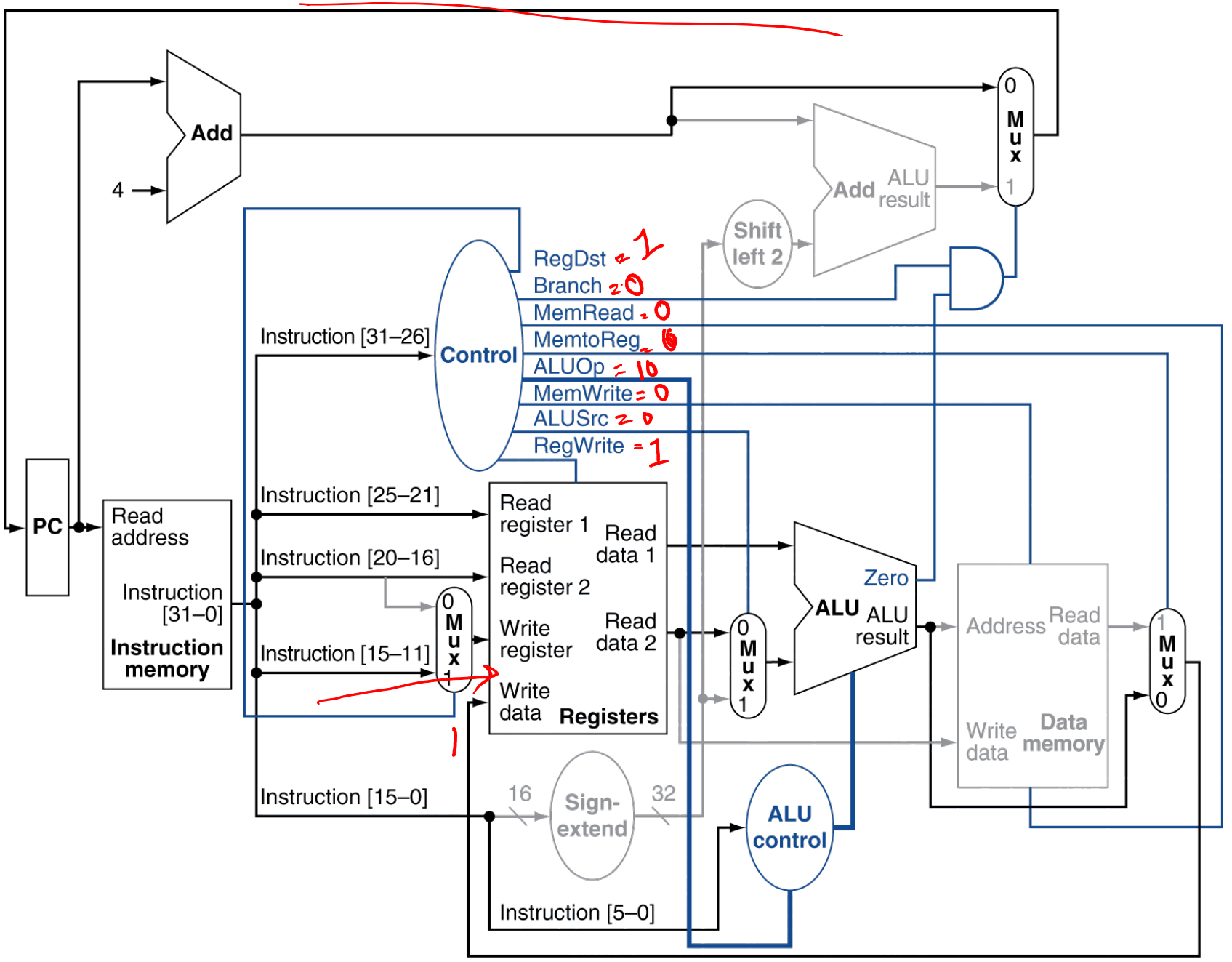
- Control signals derived from instruction



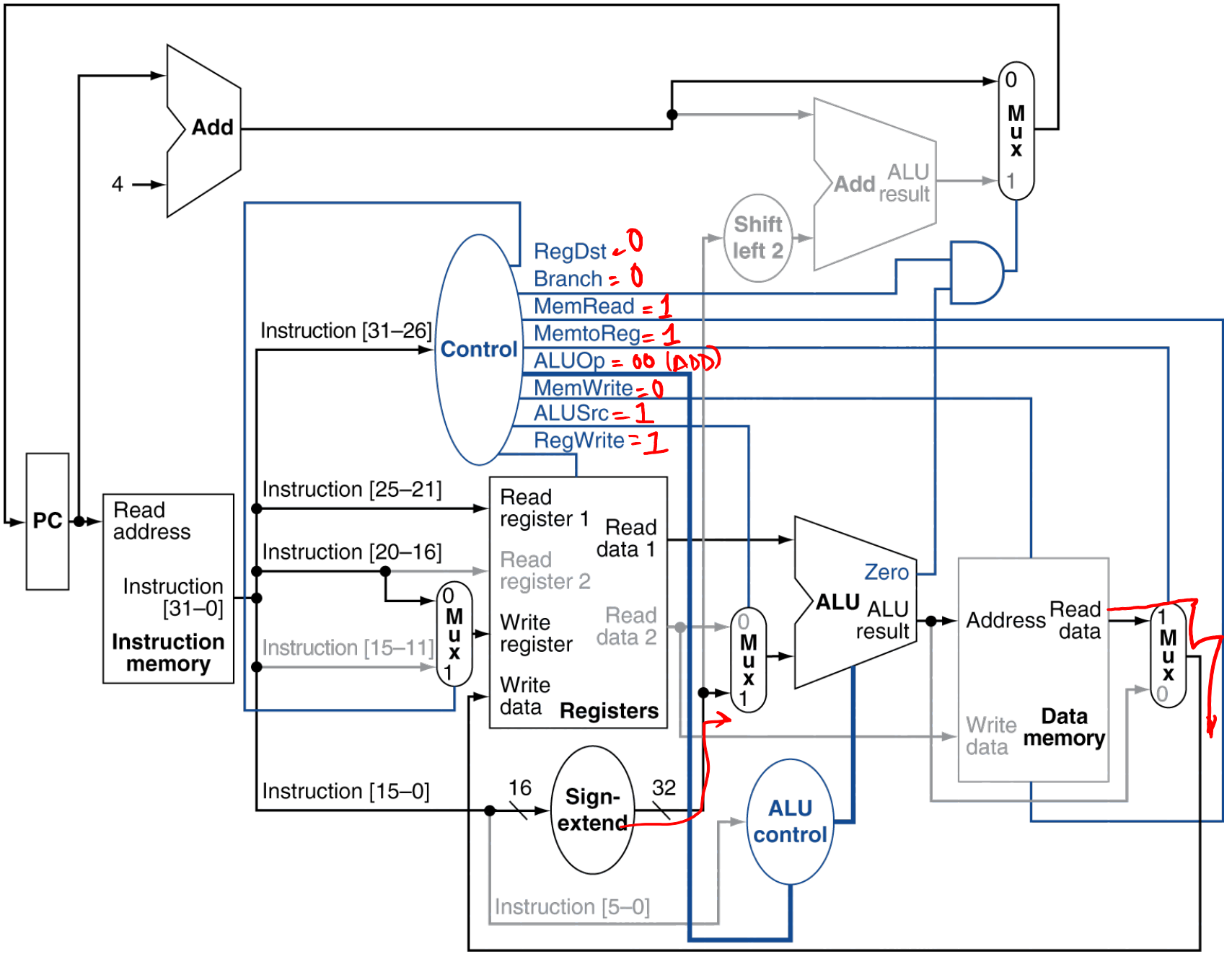
Datapath With Control



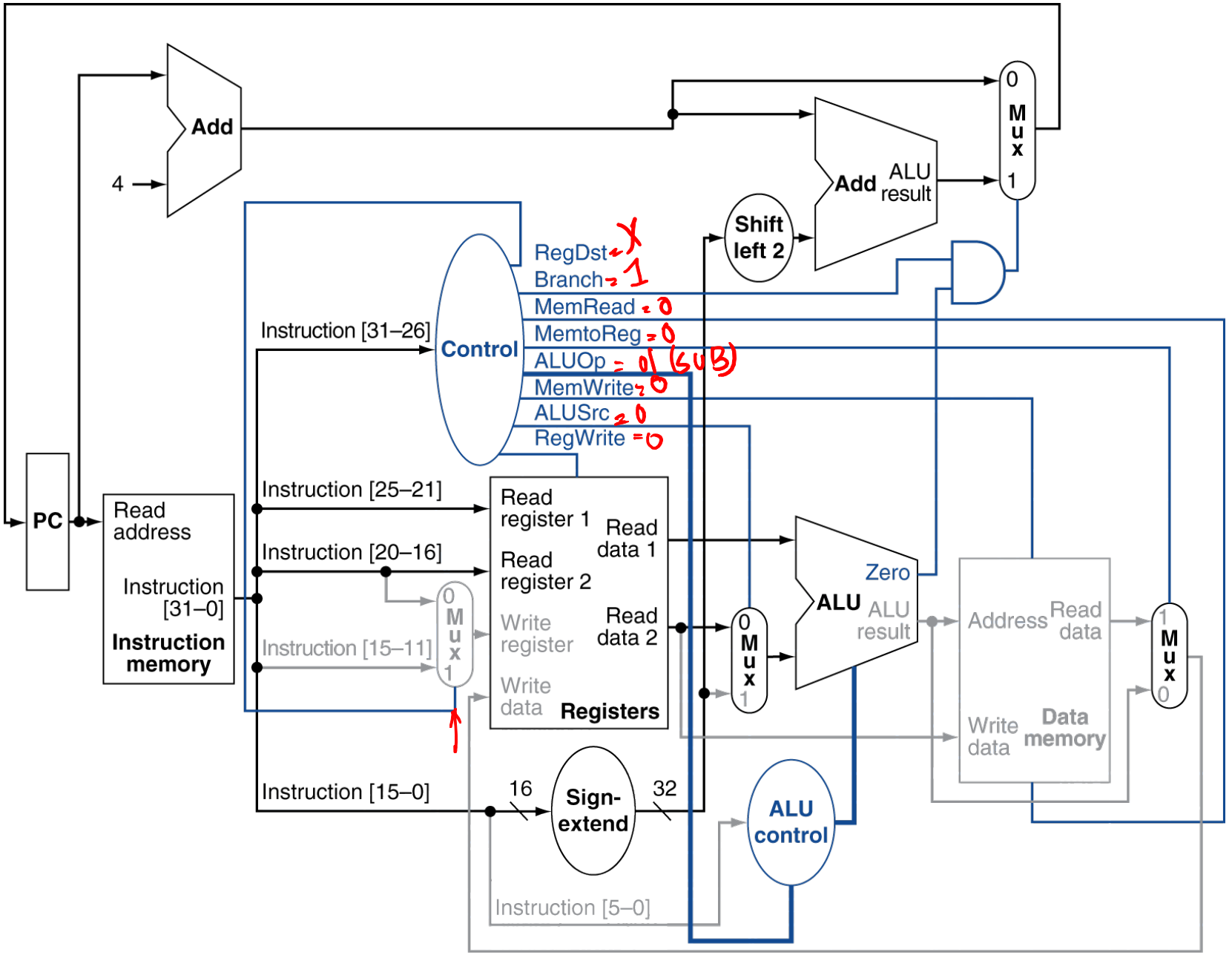
R-Type Instruction



Load Instruction



Branch-on-Equal Instruction



I Type – Control Signals

I-type ALU Instructions

RegWrite=1; ALUSrc=1; ALUoperation=ALUOp;
MemRead=X;MemWrite=X; MemToReg=0;

Load Instructions

RegWrite=1; ALUSrc=1; ALUoperation=ADD;
MemRead=1;MemWrite=0; MemToReg=1;

Store Instructions

RegWrite=0; ALUSrc=1; ALUoperation=ADD;
MemRead=0;MemWrite=1; MemToReg=X;

Control Signals

R-type, ALU Op Control Signals

RegWrite=1; ALUSrc=0; ALUoperation=Funct bits; MemRead=X;MemWrite=X; MemToReg=0;

BEQ – Control Signals

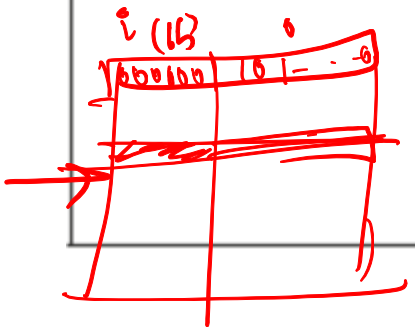
RegWrite=0; ALUSrc=0; ALUoperation=SUB; MemRead=X; MemWrite=X; MemToReg=X; PCSrc=Condition

Control Signals

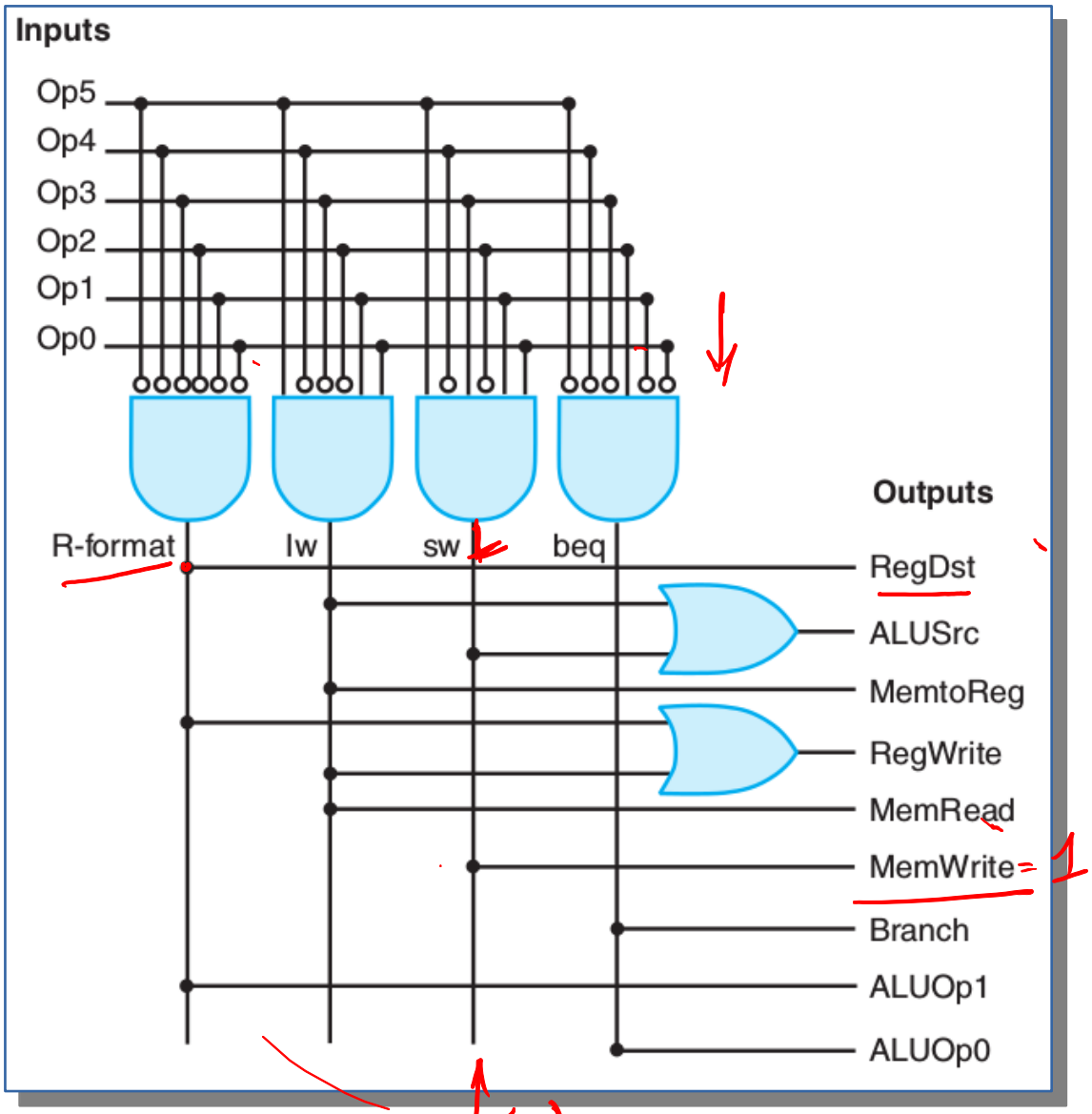
Instruction	RegDst	ALUSrc	Memto-Reg	Reg-Write	Mem-Read	Mem-Write	Branch	ALUOp1	ALUOp0
R-format	1	0	0	1	0	0	0	1	0
lw	0	1	1	1	1	0	0	0	0
sw	X	1	X	0	0	1	0	0	0
beq	X	0	X	0	0	0	1	0	1

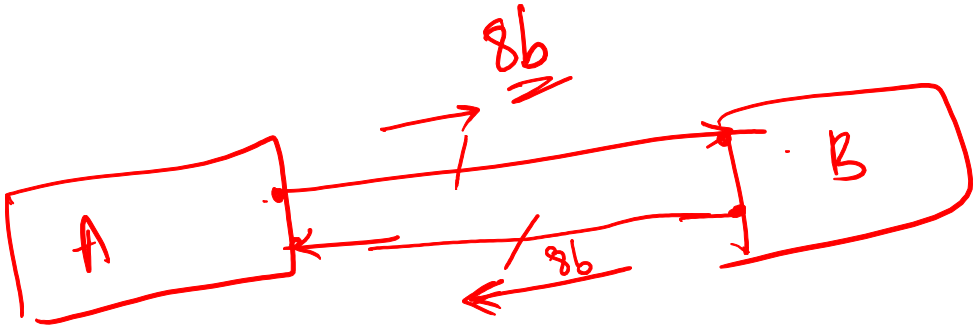
Control Signals

Input or output	Signal name	R-format	lw	sw	beq
Inputs	Op5	0	1	1	0
	Op4	0	0	0	0
	Op3	0	0	1	0
	Op2	0	0	0	1
	Op1	0	1	1	0
	Op0	0	1	1	0
Outputs	RegDst	1	0	X	X
	ALUSrc	0	1	1	0
	MemtoReg	0	1	X	X
	RegWrite	1	1	0	0
	MemRead	0	1	0	0
	MemWrite	0	0	1	0
	Branch	0	0	0	1
	ALUOp1	1	0	0	0
	ALUOp0	0	0	0	1



Control Unit Circuit



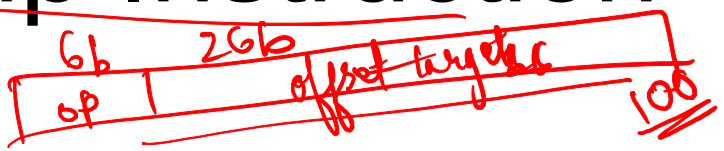


ASIC

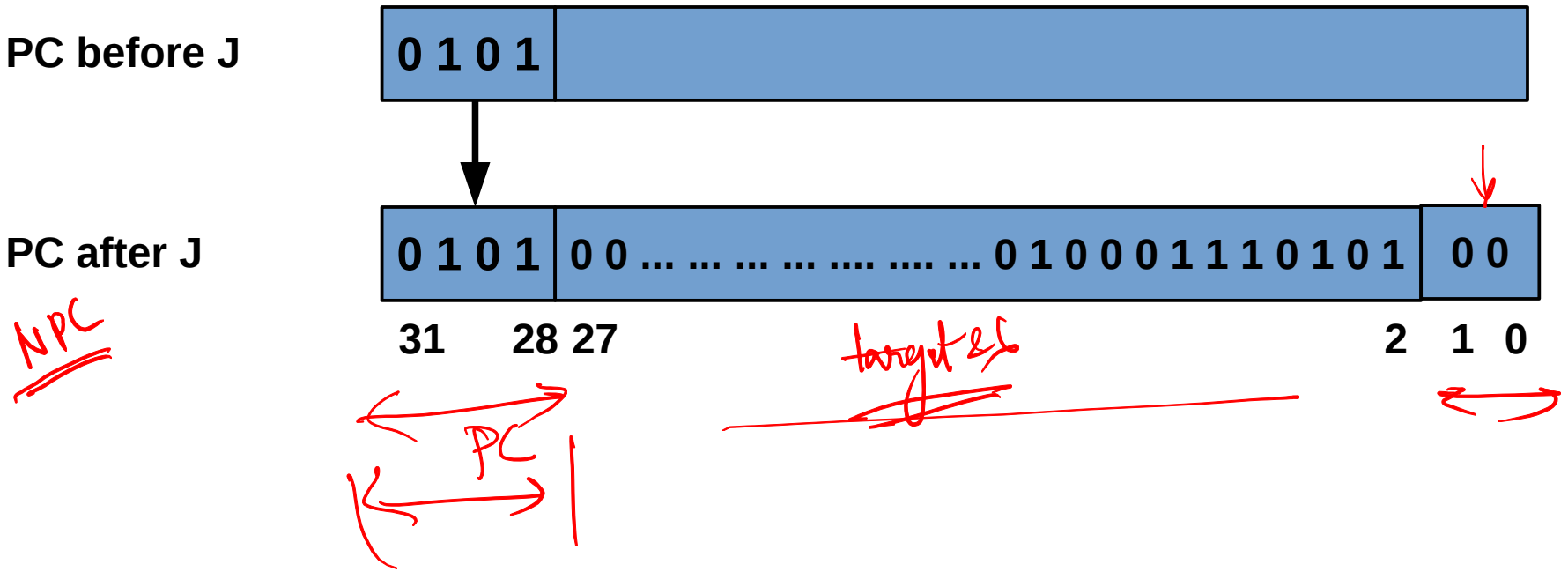
FPGA

programmable

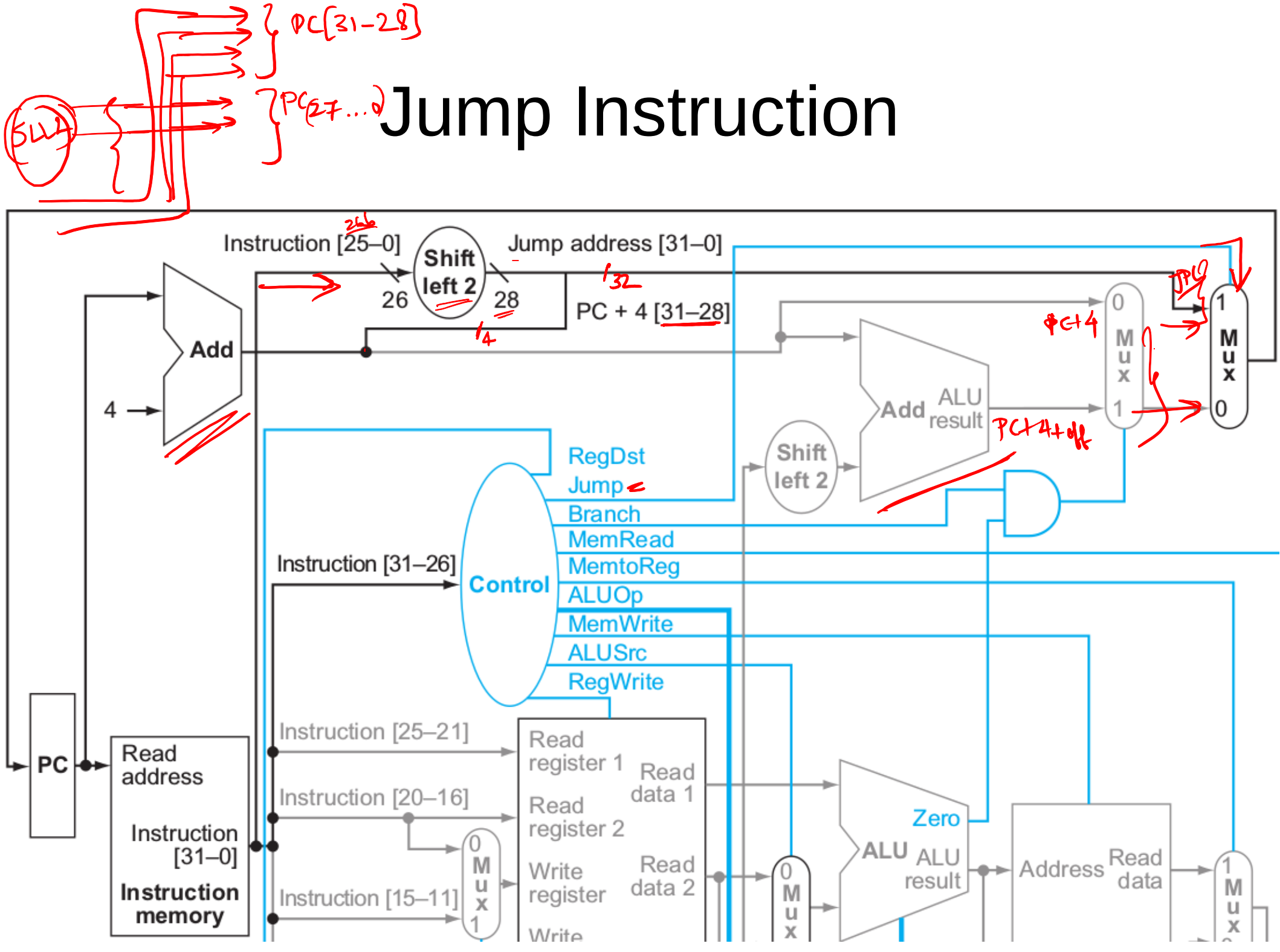
MIPS-I Jump Instruction



	Mnemonics	Example	Meaning
Jump	J, JR	J $target_{26}$ **J 0x475**	PC ← $PC_{31\text{-}28}$ || $target_{26}$ || 00



Jump Instruction



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- Control Unit design using SystemC.