A Survey of Storage Class Memory: Principles, Problems, and Possibilities

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Abstract—Storage Class Memory (SCM) is a class of memory technology which has recently become viable for use. Their name arises from the fact that they exhibit non-volatility of data, similar to secondary storage while also having latencies comparable to primary memory and byte-addressibility. In this area, Phase Change Memory (PCM), Spin-Transfer-Torque Random Access Memory (STT-RAM), and Resistive RAM (ReRAM) have emerged as the major contenders for commercial and industrial use. In this paper, we describe how these memory types function. We then discuss the ongoing research being done in these fields, highlighting a few of the major works that have been undertaken.

Index Terms—storage class memory, classification, non-volatile memory

1 Introduction

Non-Volatile Memory (NVM) is a special class of memory that exhibits persistence, similar to that of secondary memory, while providing access speeds at least two magnitudes faster. NVM can potentially replace or augment any of the current existing memory layers, like that of the cache or primary memory. Storage Class Memory (SCM) is a subset of NVM whereby the device exhibits the feature of data persistence, while offering performance comparable to or better than that of primary memory along with byte-addressibility [1], [2], [3].

The current technology used for designing caches and primary memory face many problems that SCM could potentially solve. Static RAM (SRAM), the technology typically used in caches, suffers from low density making it more and more difficult to pack together in order to meet the increasing demands of speed [4]. Dynamic RAM (DRAM) used in primary memory has a better density, but suffers from slower access times, and requires constant power to refresh memory [5].

Three emerging SCM technologies are Phase Change Memory (PCM), Spin-Transfer-Torque Random Access Memory (STT-RAM), and Resistive Random Access Memory (ReRAM). As Table 1 and Table 2 indicate, their main advantages are that they exhibit low leakage power dissipation, since they do not need to be refreshed constantly. They also have the ability to be packed close together leading to higher data storage for the same given volume. This is since the cell size of STT-RAM and ReRAM, considered as possible replacements for SRAM, are nearly one-tenth the size of SRAM. Another important feature that these memory devices exhibit is their ability to function as Multi-Level Cells (MLCs) [6], this is where a single memory cell is capable of storing more than one bit. As the resistance of the memory element can be varied based on current supplied for SCM technology, MLC is achieved by assigning different resistance levels different bit values.

While these all seem like promising reasons to adopt SCM technology, they also face some severe drawbacks. PCM and STT-RAM both suffer from high write latencies [7], nearly ten times that of DRAM for PCM, and ten times SRAM for STT-RAM, and high write energy. PCM and ReRAM also suffer from a limit on write endurance before a hard error occurs. Unlike soft errors, a hard error is when a memory element gets permanently stuck at a certain value and cannot be changed [8]. These are major issues that needs to be tackled before SCM can be widely adopted.

In this paper, we give a brief overview of how the different types of SCM function. We then identify the key areas of focus, classifying the research being done in these fields.

Section 2 covers the details of how the three SCM based memories PCM, STT-RAM, and ReRAM function. Section 3 covers all the recent research trends that have been ongoing in this field. Section 4 gives a brief introduction of popular simulators oriented towards studying properties of SCM memory. Section 5 gives an overview of possibilities that may emerge in future.

2 SCM Characteristics

2.1 Phase Change Memory (PCM)

Figure 1 shows the basic view of a PCM cell, along with the requirements for programming the cell. The phase change material is a chalcogenide typically consisting of Ge-Sb-Te (GST) [9]. GST can exist in two states, amorphous and crystalline. In the amorphous state, the device exhibits higher resistance than the crystalline state. These two states can be used to store data, where high resistance is assigned a value of 0, and low resistance is assigned a 1. PCM can also be used to store multiple states as a Multi-Level Cell (MLC).

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This is by assigning data values to intermediate resistances. In order to SET the cell, it must reach a temperature below melting point, but above crystallization temperature. The cell needs time to change into crystalline state, which is why the pulse lasts much longer. For RESET, the cell temperature must be rapidly increased to melting point, then quickly cooled so that the material sets into amorphous state [10], [11].

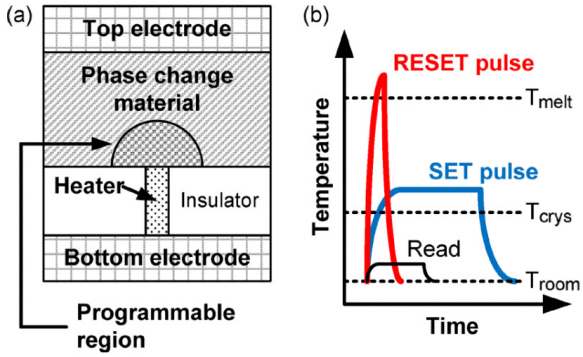

Fig. 1. (a) Cross-section of PCM cell. (b) Temperature and time required to program or read PCM cell. [12]

2.2 Spin-Transfer Torque Random Access Memory (STT-RAM)

STT-RAM represents bits of data by relying on differences in magnetic directions. There are two ferromagnetic layers in an STT-RAM separated by a dielectric. One layer is referred to as the reference layer, as it has a fixed magnetization direction. The other layer is referred to as free layer, whose magnetization direction can be controlled by passing current. Based on the relative directions of the two layers, the resistance of the magnetic tunnel junction (MTJ), will differ. In the case where the magnetization direction of the two layers are aligned, the resistance at the MTJ will be low, indicating a state of 1. If the two layers have opposing directions, the resistance becomes high, indicating a state of 0 [13]. Figure 2 shows the arrangement of the cell for the two states.

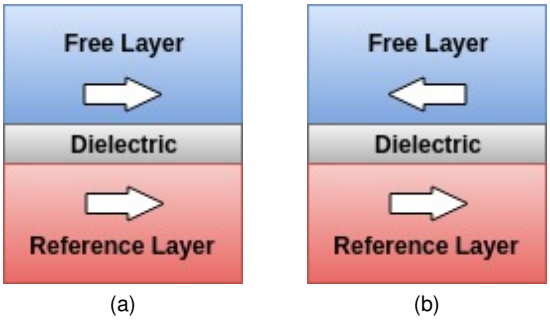

Fig. 2. (a) STT-RAM cell in SET (1) state. (b) STT-RAM cell in RESET (0) state.

2.3 Resistive Random Access Memory (ReRAM)

Resistive RAM experiences resistance changes due to electrochemical effects. The ReRAM cell consists of two metal electrodes, separated by a metal oxide layer. The behaviour of this system is dependent on the concentration of the oxygen vacancy in the metal oxide layer. By applying current to the cell, the state the cell is in can be switched. In the case of a bipolar ReRAM cell, the SET operation is undertaken when a negative bias is applied, while the RESET operation is undertaken when a positive bias is applied. An example of a ReRAM cell is a titanium oxide layer sandwiched between two platinum electrodes [14].

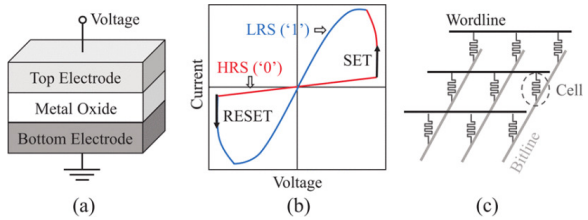

Fig. 3. (a) Structure of ReRAM cell. (b) Bias and current for write operations. [12]

3 Current Research Areas

As mentioned before, since the majority of SCM is still in the experimental stage, there is a lot of ongoing research on possible outcomes of these memory devices. Below is listed several research areas which are currently popular in this field. Table 3 lists all the areas along with the relevant papers. Some of these topics have relations where an impact in one topic may end up causing an impact in another topic. Thus, certain papers end up accomplishing multiple objectives and have been repeated multiple times in the table. Figure 4 shows some of the relations between solutions to problems that SCM faces.

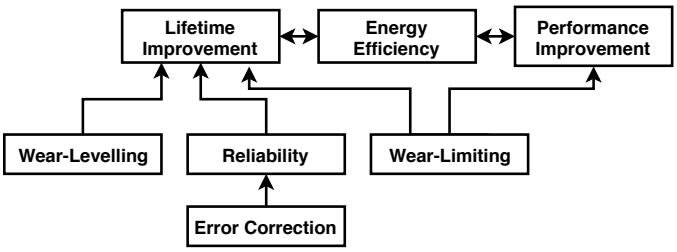

Fig. 4. Relations between different SCM issues. An arrow from one topic to another implies that changes in that field may cause impacts in the other topic.

3.1 Lifetime Improvement

While PCM has many advantages over DRAM memory, including non-volatility, low standby power, and high density, a major cause of concern is the endurance [10]. PCM and ReRAM technologies have a write endurance that are magnitudes less than those of memory technologies currently in use. Due to this, the lifetime of these memories is severely hindered.

TABLE 1
Comparison of Device Properties of Memory Technologies [7]

	Cell size (F^2)	Access Granularity	Read Latency	Write Latency	Erase Latency	Endurance	Standby Power
HDD	N/A	512B	5 ms	5 ms	N/A	$\geq 10^{15}$	1 W
SLC Flash	4 - 6	4KB	$25\mu s$	$500\mu s$	2 ms	$10^4 - 10^5$	0
DRAM	6 - 10	64B	50 ns	50 ns	N/A	$\geq 10^{15}$	Refresh Power
PCM	4 - 12	64B	50 ns	500 ns	N/A	$10^8 - 10^9$	0
STT-RAM	6 - 50	64B	10 ns	50 ns	N/A	$\geq 10^{15}$	0
ReRAM	4 - 10	64B	10 ns	50 ns	N/A	10^{11}	0

TABLE 2
Comparison of Cache Memory Technologies [15]

	SRAM	DRAM	STT-RAM	PCM
Cell Size (F^2)	120 - 200	4 - 6	6 - 50	4 - 12
Multi-level cell	No	No	Yes	Yes
Read speed	Very fast	Slow	Fast	Slow
Write speed	Very fast	Slow	Slow	Very slow
Read energy	Low	Medium	Low	Medium
Write energy	Low	Medium	High	High
Leakage	High	Medium	Low	Low
Throughput	Very high	Medium	High	Low
Write Endurance	10^{16}	10^{16}	$\geq 10^{12}$	$10^8 - 10^9$
Soft Error	Low	High	No	No

3.1.1 Wear-leveling

These are techniques which attempt to distribute writes evenly over all cells, by continuously trying to change the cell that write operations take place. Wear-leveling techniques already exist [16], [17] and are used for NAND Flash based SSDs. These involve creating a logical to physical mapping of addresses, storing the number of writes a line experiences in a table and using that data to periodically change the mapping. A shortcoming of this is that it requires a high overhead for the tables, and increases latencies due to reading and resolving of mappings. Moinuddin K. Qureshi et al. [18] proposed an alternative system which uses address space randomization to provide a low overhead wear-leveling approach.

Caches are optimised in order to maximise the temporal locality of the data in order to improve performance. This can lead to a disproportionate amount of writes being directed to certain cache lines. Endurance problems can thus arise when these caches consist of SCM. When the lifetime of the cache is estimated, the assumption is that writes are distributed evenly across the cache. Due to the disproportionate writes, certain cache lines may start to fail much before the estimated lifetime. Wear-leveling techniques are thus required in order to avoid this situation. Two simple types of wear leveling schemes can arise for caches. The first is intra-set wear-leveling, where an attempt is made to distribute writes evenly within a cache set. The second scheme is inter-set wear-leveling, where an attempt is made to avoid one cache set from receving more writes than the other sets. In this way the writes are distributed across the entire cache. For the most part, both of these schemes can operate independently, allowing for one inter-set and one intra-set wear-leveling methodology to coexist in the same cache.

One inter-set wear-leveling scheme involves set remapping [19] which has been proposed to try to tackle this problem. In this proposal, a register is maintained, and after a certain amount of time the value of the register is changed. The register is used to determine which set to write to. This method requires that tags maintain a set index, increasing the memory overhead. Jue Wang et al. [20] tried to introduce inter-set and intra-set wear-leveling using two methods. For inter-set leveling, the number of writes are measured, and after a threshold is reached, two sets are swapped. Data that was present in the sets before the swap are then invalidated. Since only two sets are swapped at a time, the performance does not take a severe toll. For intra-set leveling, the number of write hits is kept track of using a global counter. When the counter saturates, the cache line last written is flushed from the cache. This can cause a decrease in performance, and does not guarantee that the cache line that was flushed was actually frequently used.

Another proposal [21] breaks a cache set into multiple modules. The amount of writes each module receives is noted, and if the variation reaches a certain threshold, data in the most written module is moved to the least written module, and the most written module is temporarily disabled. In this way intra-set wear-leveling is achieved. A limitation is that this requires complicated computational circuitry when calculating the variation. Similar to this, Sukarn Agarwal et al. [22] proposed partitioning the cache into multiple windows. For each window, the number of writes received is noted. At regular intervals, the window with the most writes is set to read-only, and the counter for that window is reset achieveing intra-set wear-leveling. Sparsh Mittal et al. [23] proposed a intra-set wear-leveling mechanism which required maintaining a counter for each cache line. Comparisons are made between the counters of the same set, and when the difference between the largest and smallest value crosses a threshold, their data is swapped, and their counters are reset. The larger the associativity of the cache, the better the performance.

3.1.2 Wear-limiting

These are techniques which attempt to reduce the overall number of writes required for functioning. Data Comparison Write [24] schemes achieve this by first issuing a read on a cell, and then only writing to the cell if the written value differs from the stored value. Flip-N-Write [25] is another technique which builds on this, to reduce the number of writes. This is done by allocating an extra bit per block. When a write is issued to a block, the number of bit write operations needed is checked. If it is greater than half the size of the block, the extra bit is set, and each bit of the

data is complemented, then stored. Otherwise a normal data comparison write takes place. This method guarantees that a block write will require at maximum, bit writes equal to half the size of the block.

While wear-leveling and wear-limiting techniques help reduce the impact of writes, they do not have any effect on the limit on the number of writes that a cell can experience. An analytical model [26] found that there was a tradeoff between endurance and write speed. Lunkai Zhang et al. [27] built on this, proposing a wear-limiting methodology to reduce the wear that a single write operation causes by performing slow writes. Three different mechanisms have been discussed, in order to slow writes without adversely affecting the performance. Results show that this could potentially result in the lifetime doubling.

3.2 Error-Correction

Recent research [28], [29] has shown that a common cause of system crashing is due to memory failures. While many methods have arisen that attempt to reduce the effect of writes on cells and thus increase the lifetime of SCM, hard errors may still occur in the memory. By improving the error correction capabilities of SCM, the lifetime of the memory will improve, as the system will be able to last even after errors start occurring. Due to this, some procedures have to be developed in order to overcome these errors when they arise. Error-Correcting Codes (ECCs) [30], [31] have existed to mitigate effects of soft errors that occur in DRAM and SRAM. However, these approaches cannot be applied directly for SCM, as they have a high memory overhead. New methods for error mitigation have to be explored.

Error-Correcting Pointers (ECPs) [8] were suggested as an alternative for ECCs in SCM. An ECP is a pointer to a failed cell, which also stores the correct value for that cell. The suggestion given was to provide 6 ECPs for every 512-bit memory block. This enables each 512 bit block to recover from at most 6 hard errors. One limitation is that uniform allocation is not optimal. Certain rows may be more likely to experience hard failures, while others may be less likely. Once a 512 bit block fails beyond recovery, the entire page has to be discarded. As we can see from Figure 5 the vast majority of rows do not even reach four errors when the failure point of the page is reached. To counter this, proposals [32], [33] have been made to improve usage of ECPs, at the cost of additional latency and hardware. Other methods [34], [35] rely on the operating system for providing support.

Use of Error-Correcting Strings (ECSs) [36] is another proposal, in which variable-length offsets are used instead of fixed-length pointers. This allows for larger tolerance of hard errors until failure occurs. This is combined with a page-level error correction, which provides ECSs to blocks on demand. To reduce the wastage of pages caused by failures, Mohammad Khavari Tavana et al. [37] suggest utilizing Aegis [38] alongside ECP for error correction, and suggesting a method of block cooperation where the unused metadata space of one block is shared with other nearby blocks in order to reduce the chance of failure of the entire page.

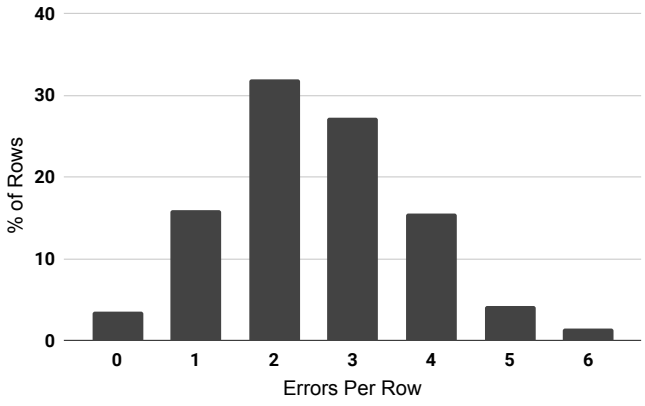

Fig. 5. Distribution of number of errors in a row when a page reaches failure point. [36]

3.3 Performance and Parallelism

The previously mentioned technique, Flip-N-Write [25], was a major milestone in the improvement of write performance. It provided a strict upper-bound on the time that would be required to complete a write operation on a block of data. It also reduced the worst-case number of write operations in half. Recent works are looking at further improving the write performance of SCM by writing multiple cells in parallel. For clarity, a *bit write* refers to a single bit whose value is changing, while a *write operation* refers to a single write issued to the controller which may consist of multiple bit writes.

Many techniques try to improve write parallelism by taking advantage of the asymmetries that exist in PCM. Writing a 0 (RESET) in PCM takes more current, but requires less time compared to writing a 1 (SET). Moinuddin K. Qureshi et al. [39] proposed a PreSET mechanism where all the cells of a PCM main memory line are preemptively SET when the respective cache line becomes dirty. In this way, when a writeback request is sent to main memory, only the faster RESET operations need to take place. This mechanism incurs a large lifetime penalty, as many unnecessary SET operations are required. Another method referred to as two-stage-write [40] exploits the write asymmetries by breaking a write operation into two stages. In the first stage, bits that are 0 are written at an accelerated rate. This is followed by the second stage, where bits that are 1 are written into in parallel to the extent that the power constraints allow. While this method improves write performance, it requires significant write asymmetries to give viable improvements. In addition, due to the separate stages, extra control circuitry is required. Zheng Li et al. [41] made an approach where the number of 1s and 0s to be written is measured. Following this, a schedule is created keeping in mind the asymmetries of power and time. In this way, concurrent bit writes are arranged without violating the power requirements. An alternative proposal called MaxPB [42] involves estimating the power requirements of each write operation that needs to be undertaken. Based on this, and the power budget given, the write operations are packaged together in order to obtain the minimum number of write operations required.

The write operations in a single package are then executed in parallel, allowing for an improvement in speed. Figure 7 compares the time taken for a few of the previously mentioned schemes.

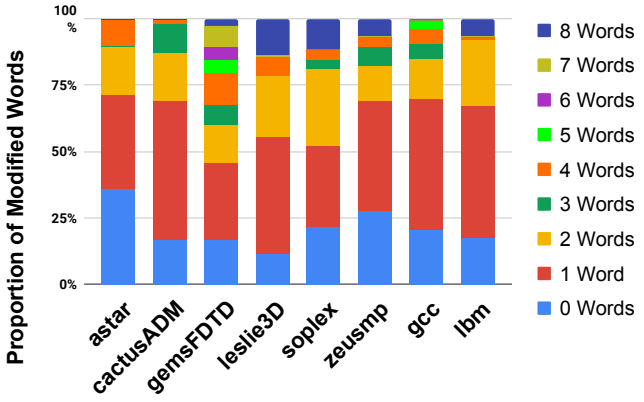

Fig. 6. Percentage of cache lines writes with given number of modified words, assuming a cache line is 64 bytes and a word is 8 bytes. [43]

An issue faced by writes on PCM memory is that write operations are handled at a cache line granularity. However, the entire cache line may not have been modified, or the write may in fact be a Silent Store [44]. Figure 6 shows the percentage of cache lines with the number of modified words for a subset of the SPEC CPU 2006 [45] benchmark suite. 0 words modified means that the write was a Silent Store [44], while 8 means that the entire cache line was modified. It can be clearly seen that in the majority of cases, only a small part of the cache line has actually been modified. Another problem arising is that while the write is being handled, the unmodified chips within a rank will remain idle. A proposal [46] was made to coalesce writes that effect the same rank into a single write operation. In this way, multiple write operations that target the same rank can be sent as a single operation, reducing the latencies and energy requirements that the multiple operations would have consumed. Similarily, MaxPB addressed this issue in order to reduce the time that write operations took. Since read operations are on the critical path, writes that are issued are put into a buffer until a certain threshold is reached. Once this threshold is reached, write operations that are required are undertaken until a lower threshold is reached. In this way, reads and writes occur in bursts. PCM also has a smaller write bandwidth than DRAM [47], [48]. Due to this, while write operations are undertaken, read operations are forced to wait, increasing their overall latency. One proposal [49] made to address this, was to cancel or pause writes when read operations were necessary. Mohammad Arjomand et al. [43] proposed several mechanisms involving utilizing error correction codes and rotating data mappings to allow for parallel read and write operations for chips that are currently being written into.

3.4 Multi-Level Cell

The resistance range of the cells in PCM are fairly large, due to the resistance gap between the amorphous and crystalline states. By manipulating the temperature and duration of a write operation to PCM, it is found that resistance values intermediate to the two states can be achieved. This allows for the possibility of a single cell to hold multiple bits by using intermediate resistance values for different states. These cells are thus referred to as Multi-Level Cells (MLCs). By using MLC instead of the previous Single-Level Cell (SLC), the density of PCM is greatly increased. In addition, the extra storage that is gained can help in tolerating failures.

However, MLCs comes with their own set of problems. Due to smaller gaps in resistance between bit levels, the write operation is more complicated and must be more precise. It is performed by applying multiple iterations of Program and Verify (P&V) [50], [51]. The operation takes place because the exact parameters (current/temperature) with which to issue the write to achieve a certain resistance varies between cells. Thus, an estimation is made and a write operation is undertaken. The value is then read, and if the resistance is not within the desired range, the process is repeated. This results in latencies almost 4 to 8 times higher than in SLC [49]. In addition the write energy consumption is also increased. MLCs also experience problems from resistance drift [52], [53]. Resistance drift is a phenomenon where the resistance of PCM cells increase with time. In SLC, since the resistance gap was so large this issue did not cause any problems, but in MLC the gaps are smaller and resistance drift can cause an unwanted change in state of the cell. This causes soft errors to pop up in PCM cells, and reduces the reliability of the device.

To resolve issues with reliability, the concept of guardbands are used [50]. In this, a band of resistance is kept between consecutive states. When a P&V operation takes place, it is ensured that the final value does not lie within the guardband range. The size of the guardband determines the amount of resistance drift that can be endured. A larger guardband means that data is retained longer as a larger resistance drift can be endured, at the cost of a larger number of iterations of P&V. A smaller guardband means that writes are less costly in terms of latency and energy, but the data will not be retained as long. There is thus a clear latency/retention time tradeoff involved [54]. It has been shown that the number of P&V iterations undertaken have no effect on the endurance of the cell [55], because RESET pulses determine endurance more than SET. To take advantage of all of these functionalities, Mingzhe Zhang et al. [56] proposed that two types of write operations exist. One, a long latency, high retention write, and the second a low latency, low retention write. They proposed a region retention monitor, to guess the required type of write when write operations are issued. Based on this guess, the appropriate write operation takes place. In this way, latencies can be improved for data that does not require high retention time.

Another method [57] proposed to overcome the reliability problems was to reduce the number of possible states that each cell of MLC has from 4 to 3, combining the two states with small resistance gap into a single state. Saeed Rashidi et al. [58] combined this with utilising the extra storage reserved for hard error correction to further alleviate the issue of reliability. This extra storage typically remains under-utilized for a long time, until hard errors start to

	Block 0 (B0)	Block 1 (B1)	Block 2 (B2)	Block 3 (B3)	Block 4 (B4)	Block 5 (B5)	Block 6 (B6)	Block 7 (B7)
Bit Changes (Inverted)	3 (3)	10 (6)	1 (1)	2 (2)	13 (3)	3 (3)	8 (8)	14 (2)

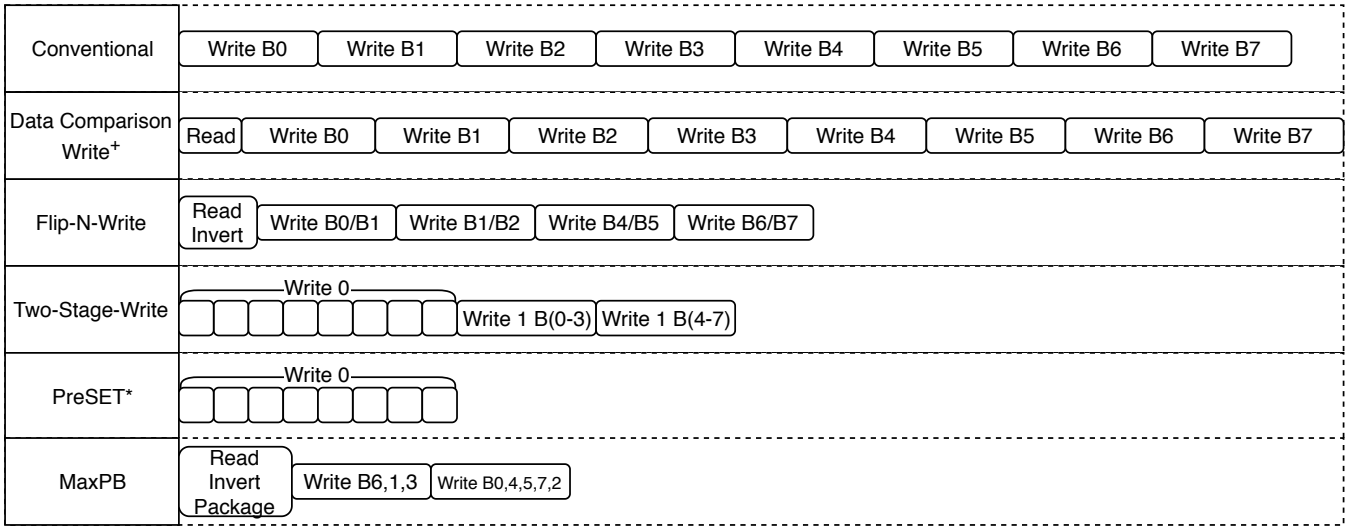

Fig. 7. Rough comparison of time taken for Conventional, Data Comparison Write [24], Flip-N-Write [25], Two-Stage-Write [40], PreSET [39], and MaxPB [42] write schemes, assuming blocks of 16 bits are written at a time. ($^+$) While Data Comparison Write has the overall highest latency, it saves both energy and endurance over the Conventional scheme, by first reading the cell. (*) While PreSET has the overall least latency, it reduces the lifetime of the memory, due to writing SET regardless of whether it's required.

occur. M-Metric [59] alongside this extra error-correction metadata is used with a tri-level PCM to improve the latencies and energy consumption as well as increase the overall IPC.

Compression techniques have been proposed as a method of reducing the impact on energy, lifetime, and latencies of MLC SCMs. A few techniques [60], [61] leverage compression to try to reduce the number of individual write operations required. However, these methods have a high overhead in terms of memory and computation. Another method is CompEx [62] coding, which attempts to provide a low overhead solution to classical methods of compression by combing statistical compression with expansion coding. Building on this, CompEx++ [63] integrates custom expansion codes and variable compressibility. These methods reduce the total energy consumption of the memory system by almost half, along with providing improvements in IPC and bandwidth.

Along with the other issues that MLC cells face, another key issue is the high read latency. In most of the common architectures [64], [65], [66], reading the values of an MLC cell works in an iterative fashion, where the values of the MSB are detected, as the resistance values differ by a large amount. Following this, the further bits are detected, with smaller consecutive resistance gaps. This method resembles a binary search across the possible resistance values of the states. A solution [67] presented to reduce the required iterations for reads is by striping multiple lines and grouping them on a single array. This method improves the read latency and IPC, at a small cost of lifetime.

3.5 Accelerators

Research has shown that PCM [68], STT-RAM [69], [70], and ReRAM [71], [72] are capable of performing operations and computations in addition to their capability of storing data. This method of having a device store data as well as perform computations allows for building in-memory accelerators which can quickly compute basic functions without requiring CPU intervention. Out of these ReRAM exhibits a crossbar array structure that is beneficial for in-memory processing of matrixvector multiplication. Due to this, many accelerators exploiting the structure of ReRAM have arisen [73], [74], [75].

Ping Chi et al. [76] used the structure in order to accelerate neural network computations. Ali Shafiee et al. [77] focussed on applying ReRAM for Convolutional Neural Network (CNN) applications. However, both of these methodologies did not work well with training and weight updations for CNNs. In an attempt to rectify this, Linghao Song et al. [78] built on these works, taking advantage of intra-layer parallelism to create an architecture that greatly boosts speed during both the training and inference phase of CNNs.

Besides focusing on neural network computations, Mahdi Nazm Bojnordi et al. [79] explored the usage of ReRAM in developing an accelerator for Boltzmann machine, resulting in a large improvement in performance along with reduced energy consumption when compared with a multicore implementation. Linghao Song et al. [80] proposed a structure to speed graph processing of graph algorithms that can be expressed as sparse matrix vector multiplication. S. Mittal compiled a survey [81] which explains neural network and processing in-memory accelerators that utilize ReRAM in more detail.

TABLE 3
Classification of Research Work

Field of Work	Papers
Lifetime Improvement	[18], [19], [20], [21], [22], [23], [27], [60], [62], [63], [82], [83], [84], [85]
Error-Correction	[8], [32], [33], [34], [35], [36], [37], [38], [86], [87], [88]
Performance and Parallelism	[39], [40], [41], [42], [43], [46], [49], [89], [90], [91], [92], [93]
Multi-Level Cells	[49], [50], [51], [52], [53], [54], [56], [57], [58], [65], [66], [67], [94], [95], [96], [97], [98], [99]
Accelerators	[68], [69], [70], [71], [72], [73], [74], [75], [76], [77], [78], [79], [80], [100], [101], [102], [103], [104], [105], [106], [107], [108], [109], [110], [111], [112], [113], [114]
SCM Type	**Papers**
ReRAM	
STT-RAM	
PCM	

4 Simulators

While several options for system simulation exist, the most popular simulators for SCM are GEM5 [115], NVSim [116] and NVMain [117], [118].

GEM5 is a simulator commonly used in computer architecture and system research. It can simulate system-level and processor microarchitecture. Provisions exist for full-system capabilities of Alpha, ARM, SPARC, and x86 simulations. The CPU model being simulated can be interchanged between a simple, an inorder, or a full-scale out-of-order CPU. For out-of-order CPU, traces can be run to obtain detailed results on the performance of the memory system.

NVSim is a circuit-level modelling tool, which provides estimations for the performance, energy, and area values for a given design specification. It supports the commonly used NVM memories, such as PCM, STT-RAM, ReRAM, as well as NAND based Flash memory. The intent of the tool is to help in creating optimized designs for the metrics mentioned, before fabricating the physical chip. NVSim is based off of the existing analytical model, CACTI [119], [120].

NVMain is a main memory simulator targeted for use with NVM-based memories. NVMain provides a cycle-accurate simulator which can estimate energy consumption at the system level. NVMain supports main memories of DRAM, PCM, STT-RAM, and ReRAM, as well as hybrid versions of these memories. NVMain has the option to be used in conjunction with GEM5 in order to evaluate full system simulation.

5 Future Outlook

Due to the many shortcomings of a pure SCM-based memory system, the majority of research now deals with hybrid memory. This gives the benefit of scalability, while allowing the shortcomings of SCM to be offset by a DRAM/SRAM component. With the release of Intel's 3D-XPoint memory [121] the use of this memory has gone from being hypothetical to practical, with claims that it performs 1000 times faster than NAND SSDs, with 1000 times the endurance. Instead of replacing existing layers of memory as was previously expected, current NVM memory is trying to bridge the gap between long latency NAND-based secondary memory, and primary memory, providing a large capacity of storage in doing so. In this way, NVM is seeking to change the memory hierarchy from a set of discrete memory layers to a spectrum of different memory possibilities.

Another aspect of SCM being actively looked at is its unique capability of supporting MLC. As mentioned previously, the use of MLC comes a new range of problems that have to be overcome before widespread use becomes practical. The International Technology Roadmap for Semiconductors (ITRS) [122], [123] predicts that densities of 3-bit and 4-bit MLCs may become possible in the near future. This increase in density may further exacerbate the existing problems that are being experienced.

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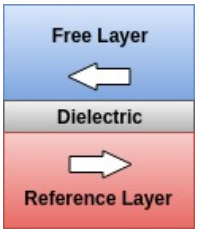

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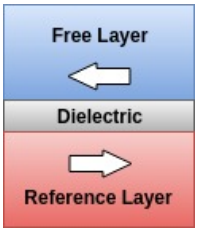

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