Energy Efficient Memory Technologies

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***Abstract*— This article aims to discuss several emerging memory technologies from an energy efficiency point of view. Three relatively new non-volatile memory technologies will be reviewed: Phase Change Memory, Resistive Switching Devices and Spin Torque Transfer Random Access Memory (STT-RAM). We will focus on their reading/writing power efficiency, area efficiency or scalability, information retaining efficiency and endurance, as well as their opportunities and limitations. Circuit and system level considerations aiming to reserve power and extend device lifetime will also be discussed.**

Keywords— Non-volatile memory, Low power memory

I. INTRODUCTION

With growing popularity of mobile handheld devices in recent decade, such as smart phone, tablets and ultra thin computers, the demand for more condensed and energy efficient information storage solutions increases rapidly. This is because these mobile devices are usually battery powered, therefore, with limited energy resource. Moreover, the demand for lighter devices and faster processing time requires fast access to more condensed memory arrays.

With increasing computation power of modern CPU core, the overall processing speed is actually bottlenecked by the how fast CPU can access cache and/or main memory. The traditional Random Access Memory solution, such as DRAM, shows benefit of fast accessing speed, however, it requires power to retain the data. For battery powered devices, the power consumed for refreshing data in DRAM may be crucial in determining the device's standby time. Non-volatile memory, on the other hand, is an ideal solution because they require no additional power to retain the data. The obstacles preventing random accessibility of non-volatile memories are mainly their long writing time and limited lifetime. However, some recently emerged technologies showed potentials to overcome these obstacles, which could be the next breakthrough in computing technologies.

In this article, we will discuss three relatively new non-volatile memory technologies, i.e. Phase change random access memory, resistive switching devices and Spin Torque Transfer random access memory (STT-RAM). We will focus on device attributes as well as circuit/system level considerations from an energy efficiency point of view. We will also discuss limitations of these technologies and methods to mitigate them. This paper is organized as follows: section II introduces the operational basics of these devices; section III discusses their energy efficiency, endurance and scalability, with comparison to traditional random access memory; section IV discusses some emerging circuit and system level considerations aiming to improve energy efficiency and to extend device lifetime; section V gives our concluding remarks.

II. OPERATION BASICS

A. Phase Change Memory

The structure of a basic phase change memory cell is illustrated in Fig. 1. The active layer of phase change memory is called phase change material, the most commonly used material is Ge-Sb-Te (GST). This type of material displays an easy tendency to be amorphized when melted then quenched quickly. Amorphous state usually displays higher resistance than crystalline state. Therefore, to SET the phase change memory, the cell needs to be heated by a charging current to a temperature below melting point, but above crystalline temperature. This allows the lattice structure of phase change memory to relax and organized into crystal structure. To RESET, a higher charging current is needed to melt the phase change grain, followed by removing the heat quickly to quench the grain into amorphous state. The SET pulse is usually longer than the RESET pulse because the lattice needs time to relax into crystalline state. Phase change memory is a single polar device, as illustrated in right panel of Fig. 1.

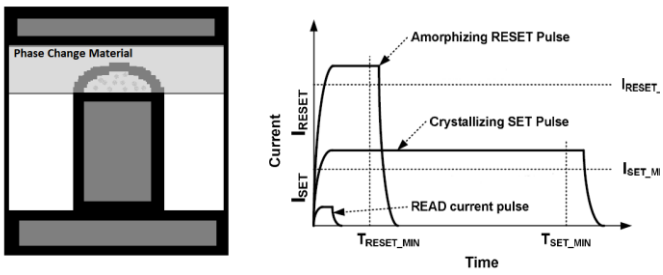

Fig. 1. Device structure of phase change memory cell and its read/write operation. [24]

B. Resistive Switching Devices

A resistive switching device, also shared the name of Memristor, is a relatively new non-volatile memory device. There are majorly two types of resistive switching devices. One is based on solid state electrolyte, in which an electrochemical effect is triggered by a positive voltage bias. As a result, a conduction link is formed between active electrode and bottom electrode, as shown in left panel of Fig. 2. The active electrode

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is made of the metal element contained in the solid state electrode. For example, if the solid state electrolyte is silver based, i.e. Ag-Ge-S, the active layer needs to be Ag [42]. When a conduction link is formed, the cell display a low resistance state, i.e. SET. The conduction link can be removed by reversely biasing the cell, i.e. RESET. This type of resistive switching device is also known as programmable metallization cell, which is a bipolar device, as illustrated in the right panel of Fig. 2, therefore a reading/writing circuit that could reverse the polarity of the memory cell is needed [43-44]. Another type of resistive switching device is based on metal oxide layer, the structure is similar to programmable metallization cell, but the active layer is a metal oxide, e.g TiO_x or TaO_x. The top lay for oxide based resistive switching device does not have to contain the active metal element. Oxide based resistive switching device is also bipolar, which needs a positive bias to SET and a negative voltage to RESET.

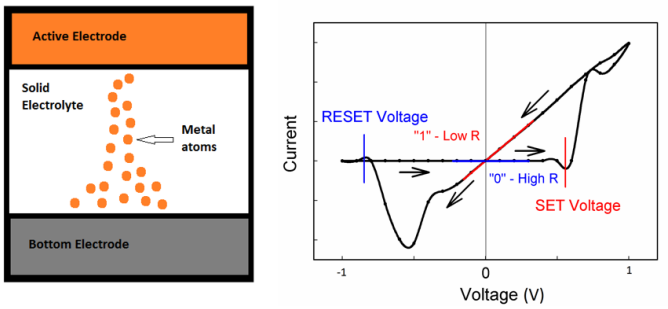

Fig. 2. Device structure of a resistive switching device based on solid state electrolyte, also known as programmable metallization cell and its SET/RESET operation.

C. Spin Torque Transfer Random Access Memory (STT-RAM)

The basic structure of a spin torque transfer random access memory cell (STT-RAM) is illustrated in Fig. 3. The device contains two ferromagnetic layers, separated by a thin dielectric, forming a magnetic tunneling junction. One of the ferromagnetic layers has fixed magnetization direction, which is call a "pinned" layer, the other layer is called "free" layer, whose magnetization directions can be switched by applying voltage across the magnetic tunneling junction. If the magnetization direction of "pinned" layer and "free" layers are aligned, the resistance of the junction is low, R_p, i.e. SET; otherwise, the resistance is high, R_{AP}, i.e. RESET [27]. As shown in right panel of Fig. 3, the STT-RAM is also a bipolar device.

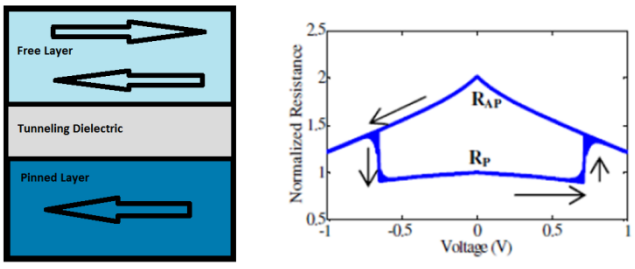

Fig. 3. Device structure of STT-RAM and its SET/RESET operation. Rp is low resistance state corresponding to aligned magnetic direction, RAP is high resistance state corresponding to opposite magnetic direction in free and pinned layers. [27]

III. Device Performance Review

A. Energy Efficiency

In order to discuss the energy efficiency of memory devices, both reading/writing current (and/or voltage) and reading/writing time need be considered, especially for non-volatile memory devices, where majority portion of energy consumption happens during write process.

As discussed above, phase change memory operates from thermal effect by melting/quenching or heating/crystallizing the active material. This usually requires high writing power, and long writing time. Some early phase change memory devices require SET time to be around 50ns, while RESET time is much longer, around 100ns. However, benefited from deep submicron technology in modern foundry, phase change grain can now be fabricated in several tens of the nano meters, which significantly reduced the required writing power, therefore, improved the energy efficiency. Moreover, recent research in material science also contributed to an improved phase changing speed, for example, using SiC dope GST materials [1-2], or fabricating GST in super lattice structure [3], [21]. The phase change behavior could be induced in as fast as 20 ns and the writing energy as low as 0.03 nJ/bit. Another articles reported even better phase change speed, for less than 6ns [19]. If optimized pulse shaped is utilized to induce phase change, even sub-ns switching could be possible [20]. Research is also going on aiming to replace GST as phase change layer. S. Song et al. [40] recently reported the potential of a low power phase change application using Sb2Te3-Ta2O5, which displays better Joule heating due to its reduced thermal conductivity compared to GST materials.

TABLE I. Basic Device Attributes Comparision

	Memory Technologies			
	DRAM	***PCRAM***	***Resistive Switching Device***	***STT-RAM***
Write Time	50ns	20-100ns	<10ns	<20ns
Read Time	30-50ns	20-50ns	<10ns	<20ns
Writing Energy	0.1 nJ/bit	> 10 pJ/bit	~fJ /bit	~pJ/bit
Reading Energy	0.1 nJ/bit	<< 0.1nJ/bit	~ fJ/bit	~pJ/bit
Lifetime	No limit	10^9	$>10^{12}$	$\sim 10^{15}$
Data Retention	Require Power	No Power Required	No Power Required	No Power Required

The application of resistive switching devices as non-volatile memory only emerged in recent decades, but the research in this field develops rapidly because of their promising characteristics, mainly fast switching time. The switching time for early resistive switching devices were reported to be less than 30ns [17-18], already much faster than flash memory or phase change memory. Recent research shows that the switching time of

resistive switching memory could easily reach 10ns or less [4]. Torrenzan et al. even reported a sub-nano second switching device, with a switching time as low as 0.3ns [5]. The energy needed to perform resistive switching is also low, because the electrochemical effect in active layer could be induced by very low electric field. Switching energy as low as several fJ/bit has been reported for electro-chemical based devices [4].

The writing/erasing time for STT-RAM is a lot better than phase change memory, but usually worse than the resistant switching devices. The writing/erasing time is reported to be less than 20ns [13]. Recent study also reports writing/erasing energy could be as low as 1 pJ/bit [12, 15]. Table I summarized the device performance for phase change memory, resistive switching devices and STT-RAM, with comparison to DRAM technology.

B. Device Lifetime

In order to serve as random access memory for modern computing instruments, the memory cells need to sustain intensive writing/erasing cycles. As a matter of fact, DRAM is an excellent candidate from lifetime perspective, because DRAM does not show any hard limit on number of cycles it could endure. On the other hand, the non-volatile memory technologies discussed above, i.e. phase change memory, resistive switching devices and STT-RAM, all show limited writing/reading cycles. Nevertheless, their lifetimes are still considerably higher than flash memory (~10^5 cycles [37]), which is currently dominating non-volatile memory market.

The writing/erasing operation of phase change memory intrinsically induces heat stress in memory cell, which limits the lifetime of the device. Typically, a phase change memory cell could endure 10^9-10^{10} cycles of writing/erasing [8]. There does exist an optimal current to RESET a given phase change memory cell, as over charging a cell will result in shorter lifetime. Study shows that doubling the writing energy to phase change memory reduces the lifetime by 50 times [9]. Therefore, a careful system level control could be used to extend the lifetime of phase change memory.

The lifetime of electro-chemical based resistive switching devices have not been tested extensively yet, most reported endurance tests range from hundreds of cycles to thousands of cycles [6]. However, there is no sign of solid electrolyte based devices reaching their endurance limits yet. For oxide based resistance switching devices, Lee et al. reported over 10^{12} switching cycles [7], also there is no sign of oxide based devices reaching endurance limits yet.

Tests on STT-RAM show that this type of device could sustain at least 10^{12} writing/erasing cycles, with an estimated lifetime of 10^{15} cycles [10-11]. Moreover, as a bonus, STT-RAM has the benefit of anti-radiation, which is ideal for aerospace applications.

C. Scalability

Scalability is another important consideration for handheld mobile devices. Phase change memory usually requires charge pumps to boost write voltage, therefore, requires larger peripheral circuits than traditional DRAM. However, with current fabrication technology, phase change cell could be fabricated in very small volume, which considerably decreased the required writing voltage, thus, the overall memory size. Phase change memory cell has shown compatibility with current CMOS technology in terms of scalability, with 22nm technology and beyond [13]. Samsung reported a phase change memory chip using 58 nm process technologies in 2011 [14]. As a result, the overall scalability of phase change memory is considered to be comparable to DRAM (~10 F^2), but significantly better than SRAM (~100 F^2). Resistive switching devices also display excellent scalability due to their simple structure and less requirement on writing/erasing energy. The overall scalability could be as low as 1 F^2 [13]. STT-RAM also displays comparable scalability to DRAM [13], [16]. Therefore, from scalability point of view, there is no obstacle for above discussed non-volatile memory technology to serve as alternative to DRAM.

In additional to their excellent fabrication scalability, multi-level cell is also possible for phase change memory, resistive switching devices as well as STT-RAM. Multi-level cell means more than one bit of data could be stored in a single memory cell. For example, the cell needs to have 2 resistive states to store one bit of data, i.e. high resistance and low resistance. In order to store n bit of data, a multi-level cell needs to have 2^n resistance states. Multi-level cell technology can significantly improve memory density and power efficiency. For phase change memory, mulit-level resistance could be realized by introducing intermediate states between amorphous and crystalline states. Y. Gu et al. [38] recently reported that by adjusting the composition of Ge-Sb-Te, one can achieve 3 distinct resistance levels by carefully controlling the SET current. The reliability in regards to controlling the resistance and distinguishing them when accessing the cell was a major concern, but recent research has reported reliable 2-bit phase change cell [23]. Y. Yin and S. Hosaka [39] also reported multi-level storage using SbTeN materials.

Multi-level resistive switching device also has been reported in [24-26], realized by controlling the programming current compliance during the Set process and voltage compliance during the Reset process. Russo et. al. [25] reported that by limiting the current compliance, the knetics of the conductive filament's formation can be controlled. The resistance of the cell can be tuned to 4 distinguished resistance states; therefore, a 2-bit cell is possible.

Lou [22] reported a 2-bit multi-level STT-RAM that has 4 resistive states. The free magnetic layer contains two domains; one can be switched by a small current, while the other can only be switched by a large current.

IV. Circuit and System Level Considerations

The overall energy efficiency of memory could be considered as product of accessing energy to individual cell and number of access to the cell. We already discussed several device level considerations aiming to reduce accessing energy to individual cells in previous section. Reducing overall accessing traffic to non-volatile memory cells could be realized through improving memory architecture and smart assessing

control [37]. Statistical study on CPU memory shows that a significant portion of memory cell stays unchanged [35] during most of processing. This gives the idea of differential writing, in which the memory control circuit first read out the data stored in the cell, compare it with the data to be written. If the data are the same, no writing is needed. This way, the writing is only performed when necessary. This significantly reduced the writing traffic, which is the most time and energy consuming task, for all three types of non-volatile memory devices discussed above.

Using non-volatile memory cell to replace computer's main memory, even cache memory may seem to be a direct approach for ultimate energy saving. However, one has to overcome the lifetime issue, because the accessing traffic in CPU memory, especially cache, may quickly wear out non-volatile memory cells. Therefore, a more feasible approach is to combine existing DRAM and the new non-volatile memory technology, i.e. hybrid memory. There are mainly two different ways to integrate non-volatile memory into CPU memory. One approach is to using non-volatile memory as backup to a DRAM buffer. Qureshi et al. showed that including a small portion of DRAM buffer will significantly improve energy consumption and overall lifetime of the memory [34]. Another approach is to integrate non-volatile memory horizontally with DRAM. CPU needs to perform statistical analysis on pages of data to be written, store data that needs high write traffic to DRAM, but write data with relatively low traffic to non-volatile memory [32-33].

While lifetime is the major concern for all non-volatile memory devices, several approaches have been reported to mitigate this drawback. One approach is to divide the memory into segments and tracks the traffic to each segment [35]. Periodically, it swaps hot and cold segments. Another approach aims to randomize the memory access by randomizing the mapping between device physical address and memory address [36]. Yoon et al. and Schechter et al. aim to introduce error correction pointer, which requires smaller memory redundancy than traditional error correction codes [28-29]. A failure in non-volatile cell could then be quickly detected and corrected.

In additional to the energy consumed by memory device itself, considerable amount of energy is actually consumed by interconnectors between computing core and memory arrays, such as metal lines. The further away the memory is from computing core, the larger the accessing energy and accessing time is needed. Therefore, an intuitive approach in conserving energy in memory is to bring memory closer to the computing core [13, 30]. The non-volatile memory cell displays excellent potential to be integrated monolithically into a 3-Dimensinal chip [41]. This means very short interconnection Vias are available to access data, which significantly reduced the distance of moving data back and forth between computing core and main memory. Therefore, overall energy efficiency is improved as a result.

V. Concluding remarks

We reviewed the phase change memory, resistive switching device and STT-RAM in terms of their energy efficiency, scalability and lifetime. On device level, non-volatile memory displays clear advantages in terms of energy efficiency and scalability. However, the lifetime limitation needs to be mitigated in order to utilize non-volatile memory as main memory. Circuit and system level strategies, such as differential writing, DRAM buffering, random accessing and error correction could be used for that purpose. Energy efficiency could be further improved by shortening the interconnectors between computing core and main memory by 3-D integration.

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