SURIYA B

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Summary

Organized and dependable candidate skilled in efficiently managing multiple priorities with a positive attitude. Willing to take on added responsibilities to effectively meet team goals while ensuring accuracy in handling multiple projects.

Internship Experience

Yellow Raft Kinetics | Design Engineer Intern June 2024 to May 2025

The automated juicer system maintains consistent juice levels across multiple cups while tracking sealed cups and total dispensed juice. Real-time data is displayed on a screen and synced to the cloud daily, ensuring accuracy and minimizing wastage.

Intel Unnathi | Embedded Systems Intern May 2024 to July 2024

The vehicle cut-in detection system improves driving safety by identifying nearby vehicles cutting in too closely and providing real-time alerts. It processes image data to detect sudden lane changes, preventing collisions in advanced driver-assistance systems.

Education

SSLC | Vijay Vikas International Senior School, Erode with 80.6 percentage. 2019-2020
HSC | Vijay Vikas International Senior School, Erode with 84.4 percentage. 2021-2022
B.E | Kongu Engineering College, Perundurai with CGPA 8.22 2022-2026

Language

• Tamil (Fluent) • English (Fluent) • Hindi (Fluent) • Japanese (Basics)

Projects

Implemented a Cyclic Redundancy Check :(CRC) algorithm on FPGA for real-time error detection in digital communication. Designed and verified the CRC module using Verilog/VHDL, optimizing for speed and resource efficiency. Deployed the design on FPGA hardware, ensuring reliable data integrity with a selected CRC polynomial.

RTL Design & Synthesis of a Pipelined RISC Processor : Designed and implemented a custom 8-bit RISC-V processor with an ALU, registers, and memory. Completed full ASIC RTL to GDSII flow using Cadence Genus and Innovus. Achieved clean timing closure and DRC, generating a fabrication-ready GDSII.

UART Protocol Verification Using UVM : This project focuses on verifying the UART communication protocol using the Universal Verification Methodology (UVM). A complete UVM testbench is developed, including sequence, driver, monitor, agent, and scoreboard components.

Technical Skills

Programming: C, Python, Java ,Verilog, System Verilog
Tools & Software: ModelSim, Cadence (Virtuso ,Genus ,Innovus), Xilinx Vivado ,proteus,ANSYS
Communication Protocols: UART, I2C,SPI, CAN
AI ,& ML Tools: TensorFlow, OpenCV

Leadership & Responsibilities

Student Assessment Coordinator – Managed student evaluations and performance tracking.
ISTE Coordinating Member – Assisted in organizing technical events and seminars.

Interests

• Digital Electronics • VLSI