Code: 9A05406

SS

B.Tech II Year II Semester (R09) Supplementary Examinations December/January 2015/2016

COMPUTER ORGANIZATION

(Electrical & Electronics Engineering)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

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1 With the help of an example, explain about:
   (a) Signed magnitude representation.
   (b) Signed 1's complement representation.
   (c) Signed 2's complement representation.

2 (a) Explain interrupt cycle with flow chart.
   (b) Describe general branch and call / return instructions.

3 (a) What are the design goals for a designer while deciding a hardwired or microprogrammed CU for a CPU?
   (b) Explain special bits, branch logic, mapping and subroutine register.

4 (a) Design an array multiplier that multiplies two 4 bit numbers. Use AND gates and binary adders.
   (b) Divide 101111100011 with 1001.

5 (a) Draw and explain the virtual memory organization.
   (b) Explain how data is organized and formatted on the magnetic disk.

6 (a) What is the need for controlling device requests? What are the mechanisms used to control device request?
   (b) What are exceptions? Explain different types of exceptions.

7 (a) Explain the hardware organization for four stage instruction pipeline.
   (b) What is data hazard?

8 (a) Explain the Inter processor communication using shared variables.
   (b) What is cache coherence protocol?

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