

B.Tech II Year II Semester (R13) Supplementary Examinations December/January 2015/2016
COMPUTER ORGANIZATION & ARCHITECTURE
(Common to CSE and IT)

Time: 3 hours

Max. Marks: 70

PART – A
(Compulsory Question)

- 1 Answer the following: (10 X 02 = 20 Marks)
- (a) Describe basic function of assembler and compiler.
 - (b) What is an interrupt driven I/O?
 - (c) Define the terms guard bits and rounding with respect to floating point operations.
 - (d) Design an adder to add two 4 bit numbers.
 - (e) Write micro operations for ADD R₁, R₂
 - (f) What is the function of control memory?
 - (g) Explain asynchronous bus in input operation with timing diagram.
 - (h) Explain significance of memory hierarchy.
 - (i) What is the role of bus controller in multiprocessor system?
 - (j) Explain 'Write after Read data hazard' in instruction pipeline.

PART – B
(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

- 2 Draw and explain Von Neumann Architecture.
- OR**
- 3 Describe following instructions with suitable examples:
- (a) RAR.
 - (b) ADC.
 - (c) JZ.
 - (d) PUSH.
 - (e) SHL.

UNIT – II

- 4 Multiply 7 and 3 using Booth's algorithm.
- OR**
- 5 Perform division of 1000 and 0011 using restoring division algorithm.

UNIT – III

- 6 Write control sequence for fetching a word from memory with neat diagram.
- OR**
- 7 Describe micro instruction sequencing with neat block diagram.

UNIT – IV

- 8 Explain address translation in virtual memory with neat block diagram and state the significance of TLB.
- OR**
- 9 What is DMA? Explain three modes of DMA operations.

UNIT – V

- 10 Draw and explain arithmetic pipeline for floating point multiplication.
- OR**
- 11 Explain instruction pipeline with neat timing diagram.
