**Code: 15A04511**

**R15**

B.Tech III Year I Semester (R15) Regular Examinations November/December 2017

**COMPUTER ORGANIZATION**

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 70

**PART – A**

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) List the role of registers involved in instruction execution.
(b) What is the difference between linker and loader?
(c) Draw the diagram of one stage Arithmetic Logic Shift Unit.
(d) Draw the timing diagram for Register Transfer Language.
(e) Convert the binary number $100101_2$ to decimal.
(f) What is the difference between hardwired and micro-programmed control?
(g) Define HIT and MISS ratio in memory.
(h) Differentiate virtual address from logical address.
(i) What is Bus arbitration?
(j) What are the advantages of vector processor?

**PART – B**

(Answer all five units, 5 X 10 = 50 Marks)

**UNIT – I**

2 Explain different functional units of a digital computer with neat sketch.

**OR**

3 State and explain different types of addressing modes.

**UNIT – II**

4 (a) Explain shift micro operations and draw 4 bit combinational circuit shifter.
(b) Draw and explain logic micro operation in detail.

**OR**

5 Explain in detail about data transfer and data manipulation instruction.

**UNIT – III**

6 Write the Booth multiplication algorithm. Draw the flowchart and explain with an example.

**OR**

7 What is micro-programmed control? Explain in detail.

**UNIT – IV**

8 (a) Discuss the function of TLB with neat sketch.
(b) Explain in detail Direct Memory Access (DMA).

**OR**

9 Explain the basic concepts of virtual and cache memory techniques.

**UNIT – V**

10 What is pipelining? Explain instruction and RISC pipeline in detail.

**OR**

11 Discuss the following
(a) Inter-Process Communication.
(b) Synchronization.

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