Code: 13A05401

R13

B.Tech III Year I Semester (R13) Supplementary Examinations November/December 2017

COMPUTER ORGANIZATION & ARCHITECTURE

(Common to ECE and EIE)

Time: 3 hours Max. Marks: 70

PART – A

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) Describe functional units of computer.
(b) Compare RISC and CISC architectures.
(c) What are the phases of instruction cycle?
(d) Represent 1259.125 in double precision format.
(e) Differentiate between hardwired and microprogrammed control unit.
(f) What is RTL? Explain with suitable example.
(g) What is set associative mapped cache?
(h) Compare programmed and interrupt driven I/O.
(i) Explain two types of adders used in arithmetic pipeline.
(j) What is polling and daisy chaining in inter processor arbitration?

PART – B

(Answer all five units, 5 X 10 = 50 Marks)

UNIT – I

2 Draw and explain structure of IAS machine.

OR

3 What are interconnection structures? Draw interconnection structures for memory, I/O and CPU module.

UNIT – II

4 Write Booth's algorithm for signed number multiplication. Multiply (5 X - 4) using same.

OR

5 Draw flowchart for non-restoring division algorithm. Divide 1100 by 0011 using the above algorithm.

UNIT – III

6 Draw and explain single bus organization. Write control sequence for executing the instruction Add (R_3), R_1 using single bus organization.

OR

7 Explain execution of complete instruction with suitable example.

UNIT – IV

8 Explain Asynchronous data transfer with neat timing diagram.

OR

9 What is virtual memory? How logical address is translated in physical address in virtual memory system?

UNIT – V

10 Describe inter processor communication and synchronization.

OR

11 Describe the following terms with respect to pipeline:

(a) Speed up.
(b) Efficiency.
(c) Throughput.

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