Code: R7220504

R07

B.Tech II Year II Semester (R07) Supplementary Examinations December/January 2015/2016

COMPUTER ORGANIZATION

(Common to CSE, IT, CSS & ECC)

(For 2008 Regular admitted batch only)

Time: 3 hours Max. Marks: 80

Answer any FIVE questions

All questions carry equal marks

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1 (a) What is hardware, software and computer?
(b) Differentiate between single bus and two-bus structures.
(c) Explain in brief about floating point representation.

2 (a) Explain various addressing modes with example.
(b) What are standard logic gates? Describe the functionality of each logic gate along with its symbol.
(c) Explain the synthesis of NAND and NOR gates.

3 (a) Explain control transfer in hardwired control unit with suitable diagram.
(b) Explain vectored interrupts.
(c) Explain control memory.

4 (a) Describe Booth's multiplication algorithm.
(b) Explain the signed-operand multiplication and integer division.

5 (a) Explain memory hierarchy.
(b) Define different types of ROM.
(c) Explain the concept of virtual memory and its implementation.

6 (a) Explain the design issues and data transfer in D.M.A with suitable diagram.
(b) What is interrupt? Explain the all types of interrupts in the complete execution of instruction.

7 (a) With a neat diagram, explain the instruction pipeline processing in RISC architecture.
(b) What are data path considerations? Explain.
(c) What is the use of fast multipliers? Write array multipliers.

8 (a) What do you mean by cache coherence? Mention the conditions for cache-coherence. Explain how cache coherence problem can be resolved by a snoopy.
(b) Describe the architecture of a shared memory multiprocessor.

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