**Code: 13A05401** **R13**

B.Tech II Year II Semester (R13) Supplementary Examinations December 2016

**COMPUTER ORGANIZATION & ARCHITECTURE**

(Common to IT & CSE)

Time: 3 hours Max. Marks: 70

**PART - A**

(Compulsory Question)

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1 Answer the following: (10 X 02 = 20 Marks)

(a) What is bus in computer? Give any two buses name.
(b) What are the categories of instructions in an instruction set?
(c) What are the various type of addressing modes?
(d) How are floating point numbers represented in a computer?
(e) What are the necessaries of shift operation in a computer?
(f) What are the needs of control memory?
(g) What are the purposes of providing cache memory?
(h) What is meant by priority interrupt?
(i) What are the stages of instruction pipelines?
(j) List out the inter process communication mechanisms.

**PART - B**

(Answer all five units, 5 X 10 = 50 Marks)

**UNIT - I**

2 Describe in detail about a CPU organization with a neat block diagram.

**OR**

3 Describe about I/O subsystem organization and interfacing in detail.

**UNIT - II**

4 Discuss about memory reference instructions with brief description of each instruction.

**OR**

5 Write booth multiplication algorithm to multiply signer 2's complement numbers.

**UNIT - III**

6 Explain how to program for arithmetic and logic operation implementations.

**OR**

7 Design and explain a micro program sequencer part of a typical control unit.

**UNIT - IV**

8 Describe in detail virtual memory concept and explain how it expands main memory capacity.

**OR**

9 Describe about direct memory access control with a neat diagram.

**UNIT - V**

10 Explain how to implement instruction cycle in pipeline with seven stages.

**OR**

11 Explain about inter processor parallel and dynamic arbitration logic.

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