Code :9A05406 **1**

II B.Tech II Semester(R09) Regular Examinations, April/May 2011
COMPUTER ORGANIZATION
(Common to Electronics & Computer Engineering, Computer Science & Engineering)
Time: 3 hours **Max Marks: 70**

Answer any FIVE questions
All questions carry equal marks

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1. (a) What are the functional units? Explain each one.
   (b) Explain about different buses in a practical computer system and their implications on accuracy, precision and addressability.
2. Describe commonly employed bit shift operations such as shift left, right and arithmetic shift left/right. Design a circuit for register length of 4 bits using D flip-flops.
3. (a) Explain the variety of techniques available for sequencing of microinstructions based on the format of the address information in the microinstruction.
   (b) Hardwired control unit is faster than micro programmed control unit. Justify this statement.
4. (a) Draw a flowchart to explain how addition and subtraction of two fixed point numbers can be done. Also draw a circuit using full adders for the same.
   (b) Explain Booth's algorithm with its theoretical basis.
5. (a) Explain how the bit cells are organized in a memory chip.
   (b) Compare and contrast direct and associative mapping techniques.
6. (a) Explain bit oriented and character oriented protocols in serial communication.
   (b) What are the different issues behind serial communication? Explain.
7. (a) What is meant by instruction pipeline? Explain four segment instruction pipeline.
   (b) Give the timing diagram of instruction pipeline.
8. (a) Differentiate tightly coupled and loosely coupled multiprocessors according to hardware.
   (b) Explain the functioning of omega switching network with a neat sketch.

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Code :9A05406 **2**

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Time: 3 hours **Max Marks: 70**

Answer any FIVE questions
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1. (a) What are the different performance measures used to represent a computer systems performance?
   (b) What do you mean by a parity bit? Explain with an example how even and odd parity bits are generated. Is it possible to correct errors using parity bits?
2. Mention about full adder circuit functionality with inputs and outputs using a block diagram. Using FA block design combined adder cum subtraction circuit. Assume two numbers are 4-bit numbers.
3. (a) What are the major design considerations in microinstruction sequencing.
   (b) Describe how microinstructions are arranged in control memory and how they are interpreted.
4. (a) Draw a flow chart which explains multiplication of two signed magnitude fixed point numbers.
   (b) Multiply 10111 with 10011 with the above procedure given (a). show all the registers content for each step.
5. Differentiate between paging and segmentation. Explain how the logical address will be translated to physical address in paging.
6. (a) What are the different types of I/O communication techniques? Give brief notes.
   (b) In the above techniques, which is the most efficient? Justify your answer.
7. Explain array processors. Explain SIMD array processor organization in detail.
8. What are the different kinds of Multi stage switching networks? Explain with neat sketch. Compare their functioning.

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Code :9A05406 **3**

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Time: 3 hours **Max Marks: 70**

Answer any FIVE questions
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1. (a) Explain about sign magnitude and 2's complement approaches for representing the fixed point numbers. Why 2's complement is preferable?
   (b) Design a 4-bit odd parity generator and checker. Can parity bit be used for error detection. If so how?
2. (a) Differentiate between RISC and CISC processors? Mention their advantages and disadvantages.
   (b) Which factors decides instruction format? Explain in detail.
3. (a) What are the major design considerations in microinstruction sequencing?
   (b) Explain about microinstruction sequencing techniques, specifically variable format address microinstruction.
4. (a) Explain how we can identify arithmetic overflow has occurred or not while adding/subtracting two signed numbers. Draw the circuit for performing addition/subtraction of two 4 bit numbers that checks the overflow.
   (b) Multiply 10111 with 10011 using booths algorithm.
5. Explain the following:
   (a) Magnetic tape systems
   (b) Optical Disc
   (c) DVD technology
6. (a) Explain bit oriented and character oriented protocols in serial communication.
   (b) What are the different issues behind serial communication? Explain.
7. (a) What is pipeline? Explain space time diagram for pipeline.
   (b) Explain pipeline for floating point addition and subtraction.
8. (a) What is the functioning of cross bar switch network? Explain. With a neat sketch.
   (b) How many switch points are there in a cross bar switch network that connect 'p' Processors to 'm' memory modules.

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Code :9A05406 4

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Time: 3 hours **Max Marks: 70**

Answer any FIVE questions
All questions carry equal marks

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1. (a) Explain about various buses such as internal, external, back plain, I/O, system, address, data, synchronous and asynchronous.
   (b) Explain about daisy chain based bus arbitration.
2. (a) What is an interrupt? Explain about interrupt cycle in detail.
   (b) How do we classify CPU's based on their register organizations. In which organizations zero address instructions are used. Mention few zero address instructions and their actual execution in practice.
3. (a) Explain the terms control word, control memory, control address register and control buffer register.
   (b) Hardwired control unit is faster than micro programmed control unit. Justify this statement.
4. (a) Explain arithmetic overflow and divide overflow with some examples for 2' s complement numbers.
   (b) Explain Booth's algorithm with its theoretical basis.
5. (a) Show the memory hierarchy and give the brief explanation.
   (b) What is virtual Memory? What are the issues behind the usage of this technique?
6. What are the different kinds of I/O communication techniques? What are the relative advantages and disadvantages? Compare and contrast all techniques.
7. Write short notes on the following:
   (a) RISC pipeline
   (b) Vector processing
   (c) Array processors.
8. (a) What is the need of inter processor synchronization? Explain.
   (b) Explain hardware lock mechanism.

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