Code: 9A05406

R09

B.Tech III Year II Semester (R09) Supplementary Examinations May/June 2016

COMPUTER ORGANIZATION

(Common to EIE and E.Con.E)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

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1 (a) Derive the circuits for a 3 bit parity generator and 4 bit parity checker using an even parity bit.
(b) Explain Amdahl's law.

2 (a) Explain the implementation of common bus using tri state buffer.
(b) Draw and explain the block diagram of n-bit parallel adder circuit.
(c) With a neat sketch explain the overflow detector logic circuit.

3 (a) Describe how microinstructions are arranged in control memory and how they are interpreted.
(b) Compare hardwired control unit and microprogrammed control unit.

4 (a) Derive an algorithm in flow chart form for the non restoring method of fixed point binary division.
(b) Divide (-12) by (4) when these numbers are represented in sign magnitude form.

5 Explain in detail the different mapping procedures in the organization of cache memory with necessary diagram.

6 (a) Give a short note on IEEE 1394 Standard.
(b) Write in detail about USB.

7 (a) Explain SIMD processor organization.
(b) Give the applications of Array processors.

8 (a) Explain the Interprocessor Communication.
(b) Write in detail about Interprocessor Arbitration.

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