
STM32
CubeMX

1. Description

1.1. Project

Project Name	Test H743ZI
Board Name	custom
Generated with:	STM32CubeMX 6.2.1
Date	07/05/2021

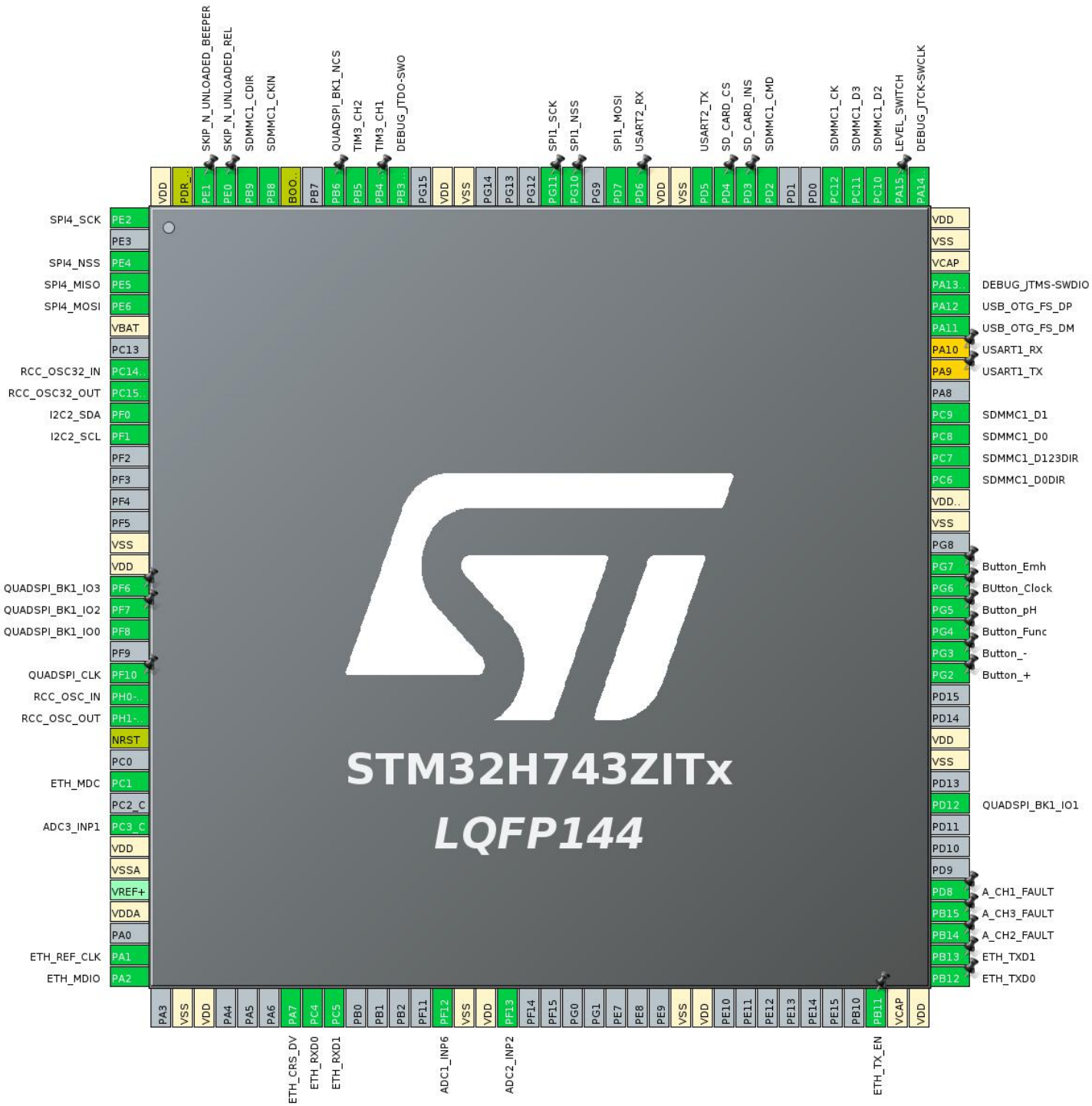
1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H743/753
MCU name	STM32H743ZITx
MCU Package	LQFP144
MCU Pin number	144

1.3. Core(s) information

Core(s)	ARM Cortex-M7

2. Pinout Configuration



3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2	I/O	SPI4_SCK	
3	PE4	I/O	SPI4_NSS	
4	PE5	I/O	SPI4_MISO	
5	PE6	I/O	SPI4_MOSI	
6	VBAT	Power		
8	PC14-OSC32_IN (OSC32_IN)	I/O	RCC_OSC32_IN	
9	PC15-OSC32_OUT (OSC32_OUT)	I/O	RCC_OSC32_OUT	
10	PF0	I/O	I2C2_SDA	
11	PF1	I/O	I2C2_SCL	
16	VSS	Power		
17	VDD	Power		
18	PF6	I/O	QUADSPI_BK1_IO3	
19	PF7	I/O	QUADSPI_BK1_IO2	
20	PF8	I/O	QUADSPI_BK1_IO0	
22	PF10	I/O	QUADSPI_CLK	
23	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	
24	PH1-OSC_OUT (PH1)	I/O	RCC_OSC_OUT	
25	NRST	Reset		
27	PC1	I/O	ETH_MDC	
29	PC3_C	I/O	ADC3_INP1	
30	VDD	Power		
31	VSSA	Power		
33	VDDA	Power		
35	PA1	I/O	ETH_REF_CLK	
36	PA2	I/O	ETH_MDIO	
38	VSS	Power		
39	VDD	Power		
43	PA7	I/O	ETH_CRS_DV	
44	PC4	I/O	ETH_RXD0	
45	PC5	I/O	ETH_RXD1	
50	PF12	I/O	ADC1_INP6	
51	VSS	Power		
52	VDD	Power		
53	PF13	I/O	ADC2_INP2	

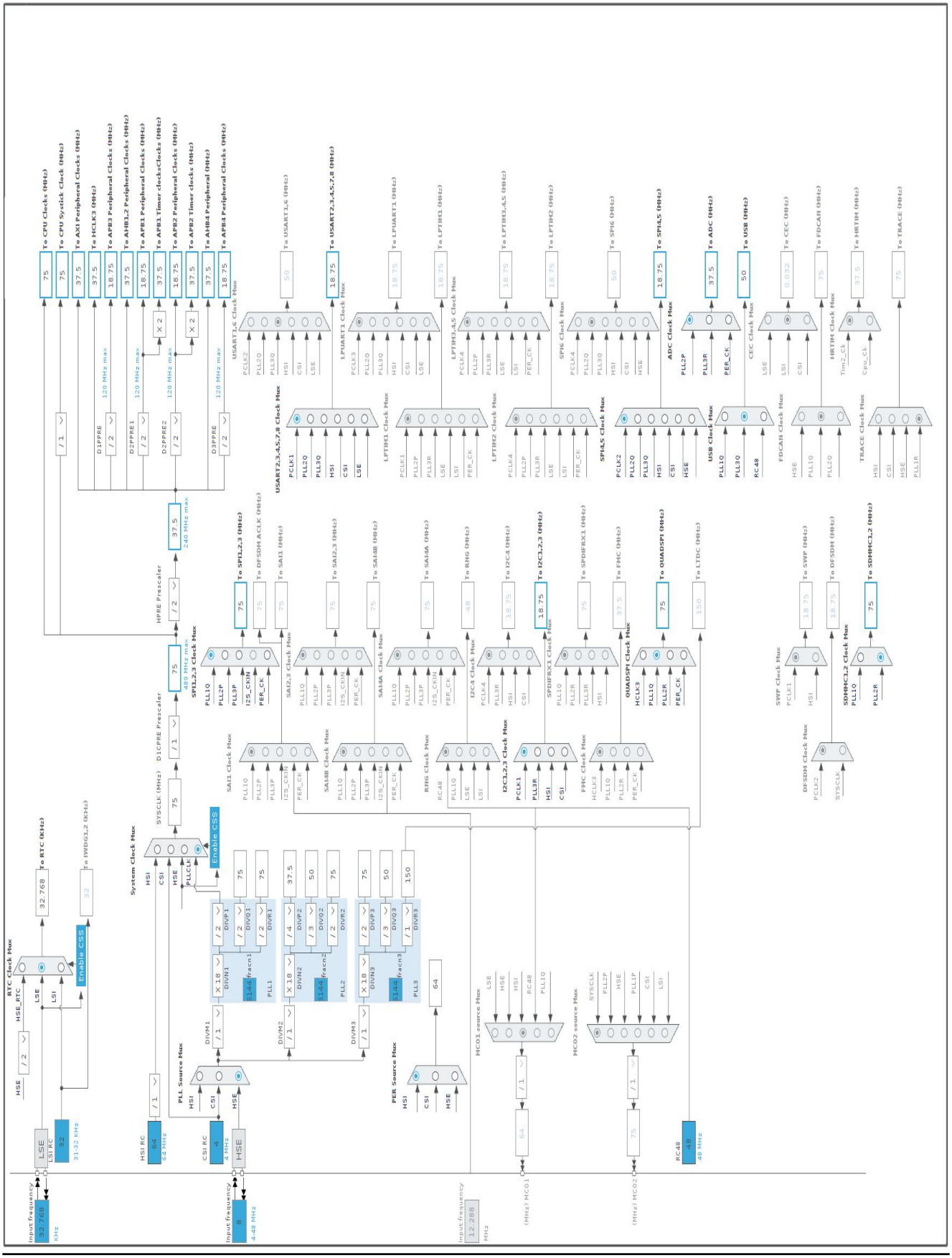
Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
61	VSS	Power		
62	VDD	Power		
70	PB11	I/O	ETH_TX_EN	
71	VCAP	Power		
72	VDD	Power		
73	PB12	I/O	ETH_TXD0	
74	PB13	I/O	ETH_TXD1	
75	PB14 *	I/O	GPIO_Input	A_CH2_FAULT
76	PB15 *	I/O	GPIO_Input	A_CH3_FAULT
77	PD8 *	I/O	GPIO_Input	A_CH1_FAULT
81	PD12	I/O	QUADSPI_BK1_IO1	
83	VSS	Power		
84	VDD	Power		
87	PG2 *	I/O	GPIO_Input	Button_+
88	PG3 *	I/O	GPIO_Input	Button_-
89	PG4 *	I/O	GPIO_Input	Button_Func
90	PG5 *	I/O	GPIO_Input	Button_pH
91	PG6 *	I/O	GPIO_Input	BUtton_Clock
92	PG7 *	I/O	GPIO_Input	Button_Emh
94	VSS	Power		
95	VDD33_USB	Power		
96	PC6	I/O	SDMMC1_D0DIR	
97	PC7	I/O	SDMMC1_D123DIR	
98	PC8	I/O	SDMMC1_D0	
99	PC9	I/O	SDMMC1_D1	
101	PA9 **	I/O	USART1_TX	
102	PA10 **	I/O	USART1_RX	
103	PA11	I/O	USB_OTG_FS_DM	
104	PA12	I/O	USB_OTG_FS_DP	
105	PA13 (JTMS/SWDIO)	I/O	DEBUG_JTMS-SWDIO	
106	VCAP	Power		
107	VSS	Power		
108	VDD	Power		
109	PA14 (JTCK/SWCLK)	I/O	DEBUG_JTCK-SWCLK	
110	PA15 (JTDI) *	I/O	GPIO_Input	LEVEL_SWITCH
111	PC10	I/O	SDMMC1_D2	
112	PC11	I/O	SDMMC1_D3	
113	PC12	I/O	SDMMC1_CK	
116	PD2	I/O	SDMMC1_CMD	

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
117	PD3 *	I/O	GPIO_Output	SD_CARD_INS
118	PD4 *	I/O	GPIO_Input	SD_CARD_CS
119	PD5	I/O	USART2_TX	
120	VSS	Power		
121	VDD	Power		
122	PD6	I/O	USART2_RX	
123	PD7	I/O	SPI1_MOSI	
125	PG10	I/O	SPI1_NSS	
126	PG11	I/O	SPI1_SCK	
130	VSS	Power		
131	VDD	Power		
133	PB3 (JTDO/TRACESWO)	I/O	DEBUG_JTDO-SWO	
134	PB4 (NJTRST)	I/O	TIM3_CH1	
135	PB5	I/O	TIM3_CH2	
136	PB6	I/O	QUADSPI_BK1_NCS	
138	BOOT0	Boot		
139	PB8	I/O	SDMMC1_CKIN	
140	PB9	I/O	SDMMC1_CDIR	
141	PE0 *	I/O	GPIO_Output	SKIP_N_UNLOADED_REL
142	PE1 *	I/O	GPIO_Output	SKIP_N_UNLOADED_BEEPER
143	PDR_ON	Reset		
144	VDD	Power		

* The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	Test H743ZI
Project Folder	/mnt/work/Documents/STM32CubeIDE/MWE/Test H743ZI
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_H7 V1.9.0
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	SystemClock_Config	RCC
3	MX_ADC1_Init	ADC1
4	MX_ADC2_Init	ADC2
5	MX_ETH_Init	ETH
6	MX_QUADSPI_Init	QUADSPI
7	MX_USB_OTG_FS_PCD_Init	USB_OTG_FS
8	MX_RTC_Init	RTC
9	MX_SDMMC1_SD_Init	SDMMC1
10	MX_SPI4_Init	SPI4
11	MX_I2C2_Init	I2C2

Rank	Function Name	Peripheral Instance Name
12	MX_USART2_UART_Init	USART2
13	MX_ADC3_Init	ADC3
14	MX_TIM3_Init	TIM3
15	MX_SPI1_Init	SPI1

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32H7
Line	STM32H743/753
MCU	STM32H743ZITx
Datasheet	DS12110_Rev5

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Alkaline(9V)
Capacity	625.0 mAh
Self Discharge	0.3 %/month
Nominal Voltage	9.0 V
Max Cont Current	200.0 mA
Max Pulse Current	0.0 mA
Cells in series	1
Cells in parallel	1

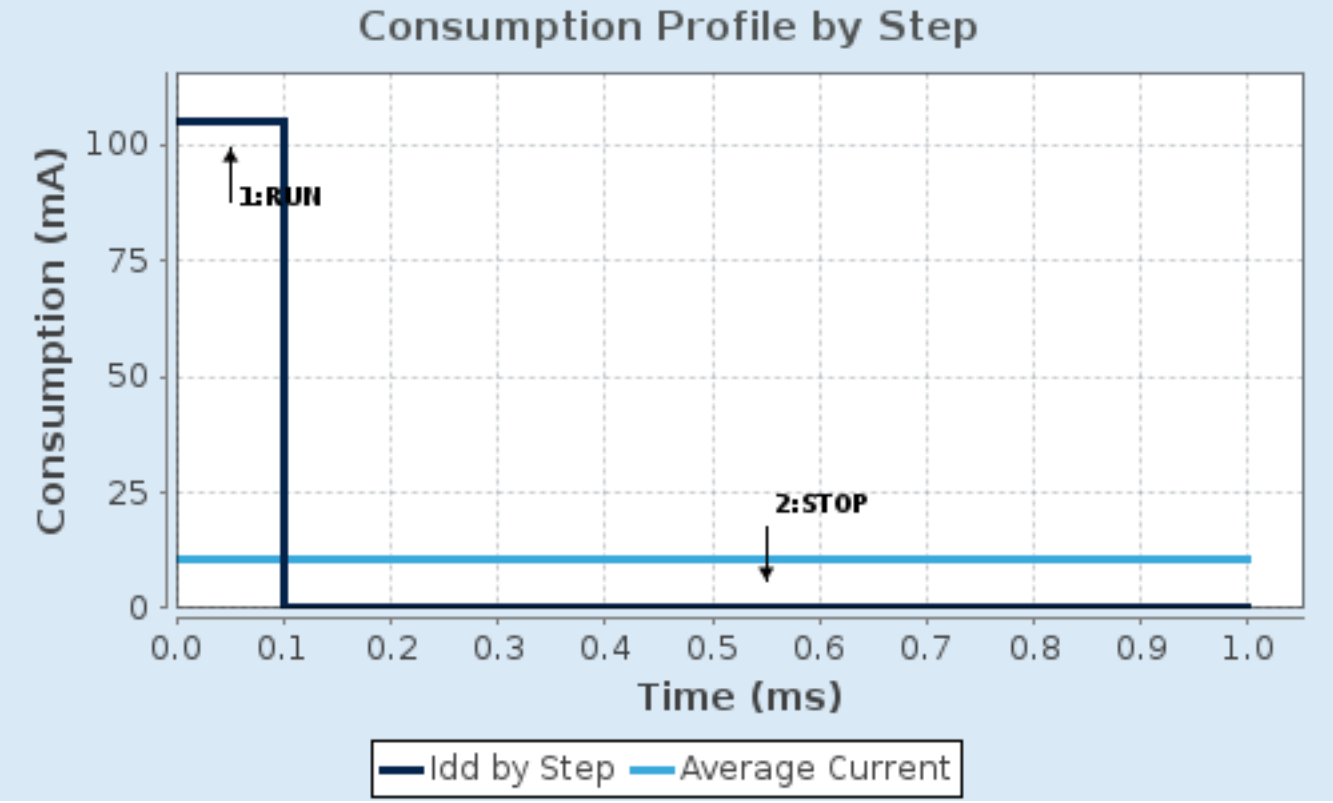
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	VOS1: Scale1-High	SVOS5: System-Scale5
D1 Mode	DRUN/CRUN	DSTANDBY
D2 Mode	DSTANDBY	DSTANDBY
D3 Mode	DRUN	DSTOP
Fetch Type	FLASH_A	NA
CPU Frequency	400 MHz	0 Hz
Clock Configuration	HSE BYP PLL Flash-ON Cache-ON	Flash-LP
Clock Source Frequency	25 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	105 mA	170 µA
Duration	0.1 ms	0.9 ms
DMIPS	856.0	0.0
Ta Max	111.14	124.98
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	10.65 mA
Battery Life	2 days, 10 hours	Average DMIPS	856.00006 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
100
75
50
25
0
1:RUN
2:STOP
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. Peripherals and Middlewares Configuration

7.1. ADC1

mode: IN6

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	Asynchronous clock mode divided by 1
Resolution	ADC 16-bit resolution
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Left Bit Shift	No bit shift
Conversion Data Management Mode	Regular Conversion data stored in DR register only
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 6
Sampling Time	1.5 Cycles
Offset Number	No offset
Offset Signed Saturation	Disable

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.2. ADC2

IN2: IN2 Single-ended

7.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	Asynchronous clock mode divided by 1
Resolution	ADC 16-bit resolution
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Left Bit Shift	No bit shift
Conversion Data Management Mode	Regular Conversion data stored in DR register only
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 2
Sampling Time	1.5 Cycles
Offset Number	No offset
Offset Signed Saturation	Disable

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.3. ADC3

IN1: IN1 Single-ended

7.3.1. Parameter Settings:

ADC_Settings:

Clock Prescaler	Asynchronous clock mode divided by 1
Resolution	ADC 16-bit resolution
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Left Bit Shift	No bit shift
Conversion Data Management Mode	Regular Conversion data stored in DR register only
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 1
Sampling Time	1.5 Cycles
Offset Number	No offset
Offset Signed Saturation	Disable

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.4. DEBUG

Debug: Trace Asynchronous Sw

7.5. ETH

Mode: RMII

7.5.1. Parameter Settings:

General : Ethernet Configuration:

Warning	The ETH can work only when RAM is pointing at 0x24000000
Ethernet MAC Address	00:80:E1:00:00:00
Tx Descriptor Length	4
First Tx Descriptor Address	**0x30040060 ***
Rx Descriptor Length	4
First Rx Descriptor Address	**0x30040000 ***
Rx Buffers Address	**0x30040200 ***
Rx Buffers Length	1524

7.6. I2C2

I2C: I2C

7.6.1. Parameter Settings:

Timing configuration:

Custom Timing	Disabled
I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x0040486C ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.7. QUADSPI

QuadSPI Mode: Bank1 with Quad SPI Lines

7.7.1. Parameter Settings:

General Parameters:

Clock Prescaler	255
Fifo Threshold	1
Sample Shifting	No Sample Shifting
Flash Size	1
Chip Select High Time	1 Cycle
Clock Mode	Low
Flash ID	Flash ID 1
Dual Flash	Disabled

7.8. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.8.1. Parameter Settings:

Power Parameters:

SupplySource	PWR_LDO_SUPPLY
Power Regulator Voltage Scale	Power Regulator Voltage Scale 3

RCC Parameters:

TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000
LSE Drive Capability	LSE oscillator low drive capability
CSI Calibration Value	16
HSI Calibration Value	32

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	0 WS (1 CPU cycle)
Product revision	rev.Y

PLL range Parameters:

PLL1 clock Input range	Between 8 and 16 MHz
PLL2 input frequency range	Between 8 and 16 MHz
PLL3 input frequency range	Between 8 and 16 MHz
PLL1 clock Output range	MEDIUM VCO range
PLL2 clock Output range	MEDIUM VCO range
PLL3 clock Output range	MEDIUM VCO range

7.9. RTC

mode: Activate Clock Source

mode: Activate Calendar

7.9.1. Parameter Settings:

General:

Hour Format	Hourformat 24
Asynchronous Predivider value	127
Synchronous Predivider value	255

Calendar Time:

Data Format	BCD data format
Hours	0
Minutes	0
Seconds	0
Day Light Saving: value of hour adjustment	Daylightsaving None
Store Operation	Storeoperation Reset

Calendar Date:

Week Day	Monday
Month	January
Date	1
Year	0

7.10. SDMMC1

Mode: SD 4 bits Wide bus with dir voltage converter

7.10.1. Parameter Settings:

SDMMC parameters:

Clock transition on which the bit capture is made	Rising transition
SDMMC Clock output enable when the bus is idle	Disable the power save for the clock
SDMMC hardware flow control	The hardware control flow is disabled
SDMMC clock divide factor	0
Is external transceiver present ?	no

7.11. SPI1

Mode: Transmit Only Master
Hardware NSS Signal: Hardware NSS Output Signal

7.11.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**32 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**32 ***
Baud Rate	**2.34375 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Output Hardware
Fifo Threshold	**Fifo Threshold 04 Data ***
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	**04 Cycle ***
Master Inter Data Idleness	**04 Cycle ***
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

7.12. SPI4

Mode: Full-Duplex Master
Hardware NSS Signal: Hardware NSS Output Signal

7.12.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2

Baud Rate	**9.375 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Output Hardware
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

7.13. SYS

Timebase Source: SysTick

7.14. TIM3

Combined Channels: Encoder Mode

7.14.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	Encoder Mode TI1
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division

Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

7.15. USART2

Mode: Asynchronous

7.15.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.16. USB_OTG_FS

Mode: Device_Only

7.16.1. Parameter Settings:

Speed	Full Speed 12MBit/s
Enable internal IP DMA	Disabled
Low power	Disabled
Battery charging	Disabled
Link Power Management	Disabled
Use dedicated end point 1 interrupt	Disabled
VBUS sensing	Disabled
Signal start of frame	Disabled

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PF12	ADC1_INP6	Analog mode	No pull-up and no pull-down	n/a	
ADC2	PF13	ADC2_INP2	Analog mode	No pull-up and no pull-down	n/a	
ADC3	PC3_C	ADC3_INP1	Analog mode	No pull-up and no pull-down	n/a	
DEBUG	PA13 (JTMS/SWDIO)	DEBUG_JTMS-SWDIO	n/a	n/a	n/a	
	PA14 (JTCK/SWCLK)	DEBUG_JTCK-SWCLK	n/a	n/a	n/a	
	PB3 (JTDO/TRACESWO)	DEBUG_JTDO-SWO	n/a	n/a	n/a	
ETH	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA1	ETH_REF_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA7	ETH_CRS_DV	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC4	ETH_RXD0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC5	ETH_RXD1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB11	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB12	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB13	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
I2C2	PF0	I2C2_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	
	PF1	I2C2_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	
QUADSPI	PF6	QUADSPI_BK1_IO3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PF7	QUADSPI_BK1_IO2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PF8	QUADSPI_BK1_IO0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PF10	QUADSPI_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD12	QUADSPI_BK1_IO1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB6	QUADSPI_BK1_NCS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
RCC	PC14-OSC32_IN (OSC32_IN)	RCC_OSC32_IN	n/a	n/a	n/a	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0-OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a	
SDMMC1	PC6	SDMMC1_D0DIR	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC7	SDMMC1_D123DIR	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC8	SDMMC1_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC9	SDMMC1_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC10	SDMMC1_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC11	SDMMC1_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC12	SDMMC1_CK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD2	SDMMC1_CMD	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PB8	SDMMC1_CKIN	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PB9	SDMMC1_CDIR	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
SPI1	PD7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG10	SPI1_NSS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG11	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
SPI4	PE2	SPI4_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE4	SPI4_NSS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE5	SPI4_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE6	SPI4_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM3	PB4 (NJTRST)	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB5	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART2	PD5	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD6	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USB_OTG_FS	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	Low	
Single Mapped Signals	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
GPIO	PB14	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	A_CH2_FAULT
	PB15	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	A_CH3_FAULT
	PD8	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	A_CH1_FAULT

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PG2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	Button_+
	PG3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	Button_-
	PG4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	Button_Func
	PG5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	Button_pH
	PG6	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	BUtton_Clock
	PG7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	Button_Emh
	PA15 (JTDI)	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	LEVEL_SWITCH
	PD3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SD_CARD_INS
	PD4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	SD_CARD_CS
	PE0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SKIP_N_UNLOADED_REL
	PE1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SKIP_N_UNLOADED_BEEPER

8.2. DMA configuration

nothing configured in DMA service

8.3. BDMA configuration

nothing configured in DMA service

8.4. MDMA configuration

nothing configured in DMA service

8.5. NVIC configuration

8.5.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
PVD and AVD interrupts through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 global interrupts	unused		
TIM3 global interrupt	unused		
I2C2 event interrupt	unused		
I2C2 error interrupt	unused		
SPI1 global interrupt	unused		
USART2 global interrupt	unused		
SDMMC1 global interrupt	unused		
Ethernet global interrupt	unused		
Ethernet wake-up interrupt through EXTI line 86	unused		
FPU global interrupt	unused		
SPI4 global interrupt	unused		
QUADSPI global interrupt	unused		
USB On The Go FS End Point 1 Out global interrupt	unused		
USB On The Go FS End Point 1 In global interrupt	unused		
USB On The Go FS global interrupt	unused		
HSEM1 global interrupt	unused		
ADC3 global interrupt	unused		

8.5.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false

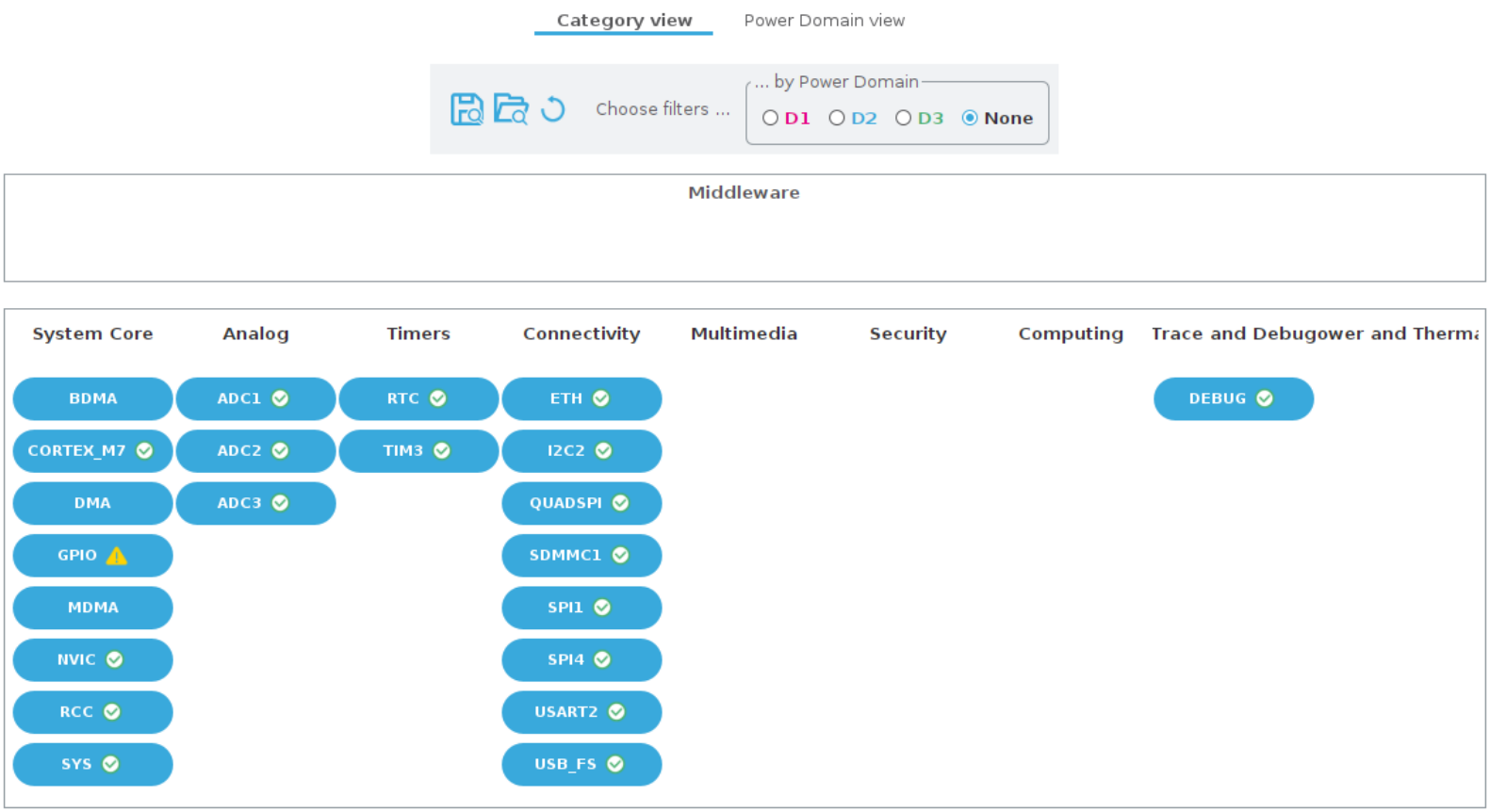
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true

*** User modified value**

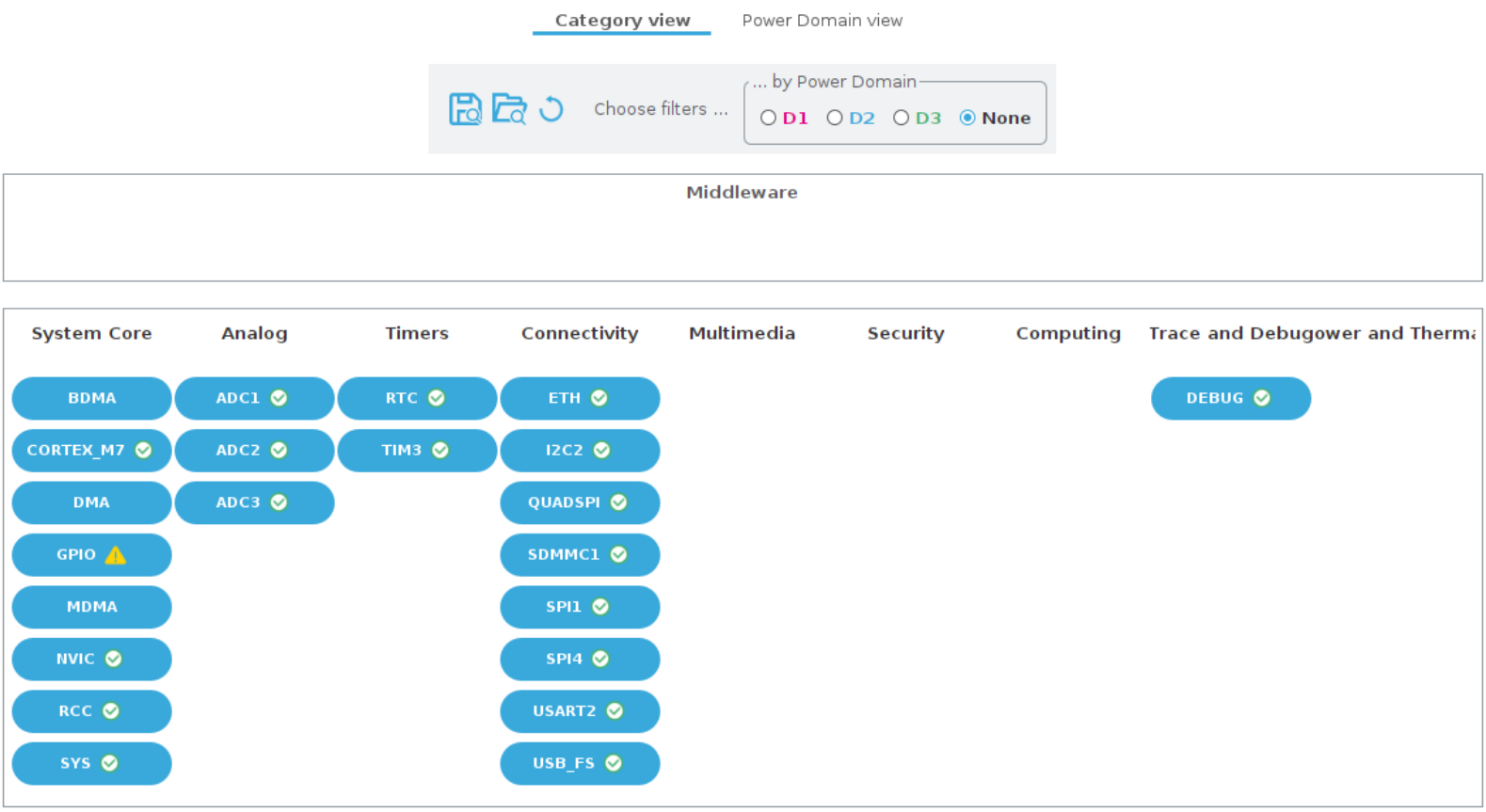
9. System Views

9.1. Category view

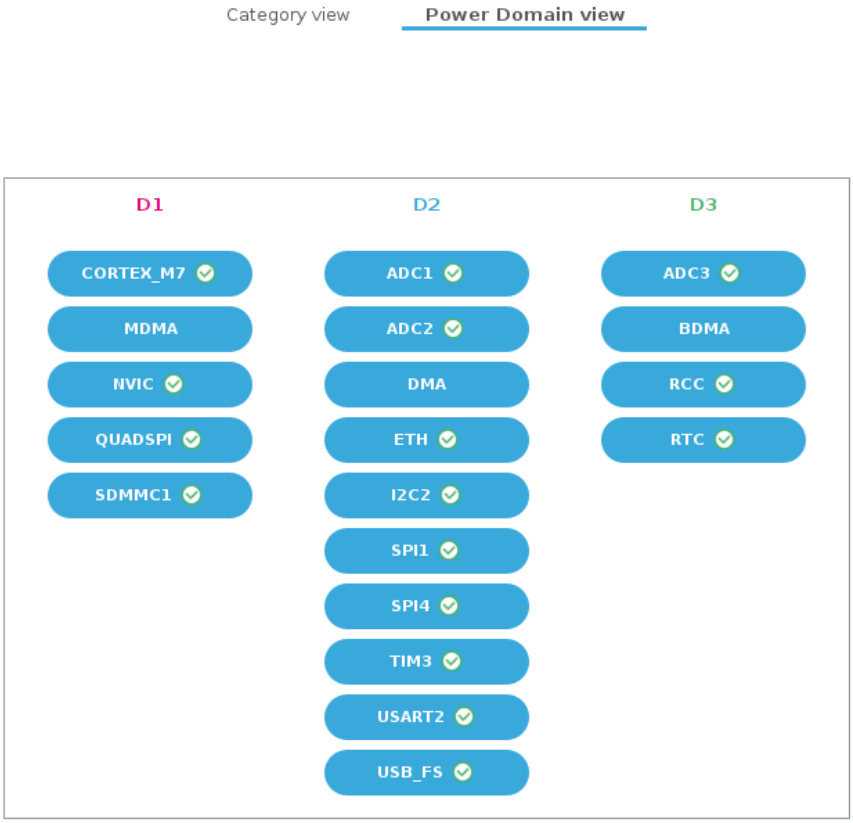
9.1.1. Current



9.1.2. Without filters



9.2. Power Domain view



10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00387108.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00314099.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00237416.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00368411.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00072315.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073742.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00081379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00121475.pdf
Application note	http://www.st.com/resource/en/application_note/DM00129215.pdf
Application note	http://www.st.com/resource/en/application_note/DM00151811.pdf
Application note	http://www.st.com/resource/en/application_note/DM00160482.pdf
Application note	http://www.st.com/resource/en/application_note/DM00220769.pdf
Application note	http://www.st.com/resource/en/application_note/DM00227538.pdf
Application note	http://www.st.com/resource/en/application_note/DM00257177.pdf
Application note	http://www.st.com/resource/en/application_note/DM00272912.pdf
Application note	http://www.st.com/resource/en/application_note/DM00272913.pdf
Application note	http://www.st.com/resource/en/application_note/DM00226326.pdf
Application note	http://www.st.com/resource/en/application_note/DM00236305.pdf

Application note	http://www.st.com/resource/en/application_note/DM00296349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00327191.pdf
Application note	http://www.st.com/resource/en/application_note/DM00287603.pdf
Application note	http://www.st.com/resource/en/application_note/DM00337702.pdf
Application note	http://www.st.com/resource/en/application_note/DM00393275.pdf
Application note	http://www.st.com/resource/en/application_note/DM00337873.pdf
Application note	http://www.st.com/resource/en/application_note/DM00354244.pdf
Application note	http://www.st.com/resource/en/application_note/DM00373474.pdf
Application note	http://www.st.com/resource/en/application_note/DM00315319.pdf
Application note	http://www.st.com/resource/en/application_note/DM00356635.pdf
Application note	http://www.st.com/resource/en/application_note/DM00380469.pdf
Application note	http://www.st.com/resource/en/application_note/DM00354333.pdf
Application note	http://www.st.com/resource/en/application_note/DM00395696.pdf
Application note	http://www.st.com/resource/en/application_note/DM00431633.pdf
Application note	http://www.st.com/resource/en/application_note/DM00493651.pdf
Application note	http://www.st.com/resource/en/application_note/DM00535045.pdf
Application note	http://www.st.com/resource/en/application_note/DM00525510.pdf
Application note	http://www.st.com/resource/en/application_note/DM00536349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00609692.pdf
Application note	http://www.st.com/resource/en/application_note/DM00622045.pdf
Application note	http://www.st.com/resource/en/application_note/DM00623136.pdf
Application note	http://www.st.com/resource/en/application_note/DM00625700.pdf
Application note	http://www.st.com/resource/en/application_note/DM00660346.pdf
Application note	http://www.st.com/resource/en/application_note/DM00600614.pdf
Application note	http://www.st.com/resource/en/application_note/DM00628458.pdf
Application note	http://www.st.com/resource/en/application_note/DM00725181.pdf