



Datasheet for AncASIC_P1

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1 Introduction

The AncASIC is a proposed ASIC manufactured in the XFAB 110 nm PD-SOI process (XT011). Each chip is intended to provide the electrical interface (including both data and serial power) between the control room and an individual large-area monolithic active pixel sensor (LAS). The current chip (AncASIC_P1) is an early-stage prototype that is designed to enable independent testing and functional verification of several key components of the complete AncASIC.

1.1 Components

The AncASIC_P1 ASIC includes the following components:

- An I₂C controller (programming interface for configuring individual configuration registers)
- Negative voltage bias generator (NVBG)
- Current-mode logic (CML) transmitter and receiver
- A passthrough, differential transmission line
- Test devices (MOSFET, BJT, resistor, etc.)
- Pre-regulator designed by LBNL ASIC group

The overall layout of these components is summarized in Fig. 1.

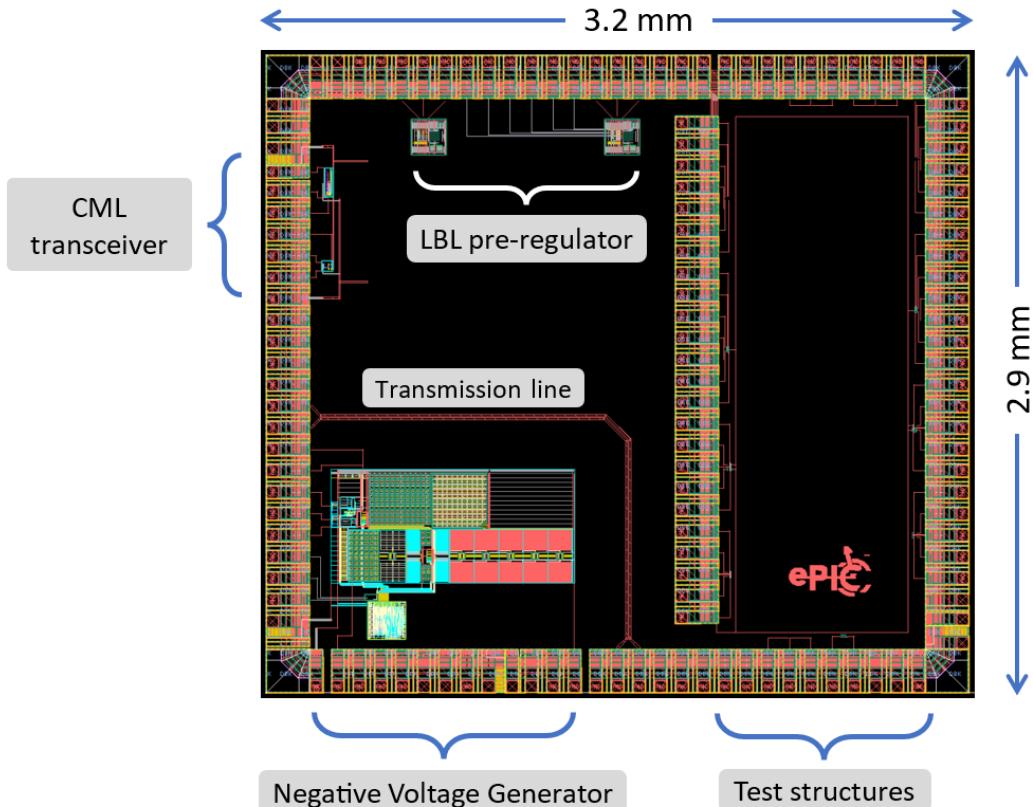


Figure 1: AncASIC_P1 layout.

1.2 Physical dimensions

- Chip size: 3.2×2.9 mm
- Pad pitch = $100 \mu\text{m}$
- Number of pads = 133
- All wire-bond pads are the same size
- The bonding pads for the NVBG (located near the bottom-left corner) are disconnected from the rest of the pad ring, which is necessary for them to output negative voltages without turning on protection diodes

1.3 Electrical interface

Fig. 2 graphically summarizes the pinout of the ASIC.

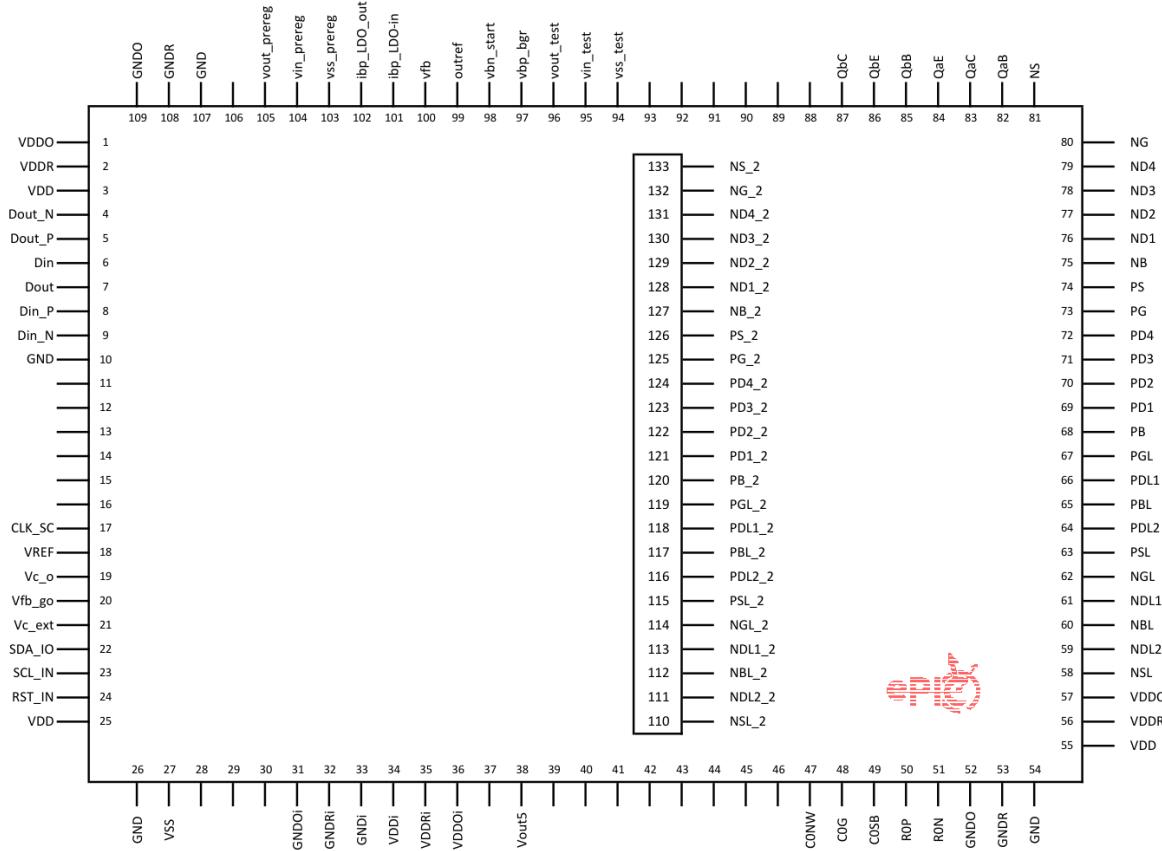


Figure 2: AncASIC_P1 physical pinout.

2 Electrical Specification

The table below lists the names, input/output type, signal level, and brief description of each bond pad on the ASIC. Blank lines correspond to unconnected pads.

Pin	Name	I/O	Signal level			Description
			Min	Typ	Max	
1	VDDO	Power		1.2		V Power Supply
2	VDDR	Power		1.2		V Power Supply
3	VDD	Power		1.2		V Power Supply
4	Dout_N	Differential out	400	mV		CML Transmitter output N
5	Dout_P					CML Transmitter output P
6	Din	Analog In		1.2		V CML Transmitter input
7	Dout	Analog Out		1.2		V CML Receiver output
8	Din_P	Analog In				V CML Receiver input P
9	Din_N	Analog In				V CML Receiver input N
10	GND	Ground	0	0	0	V Ground
11						
12						
13						
14						
15						
16						
17	CLK_SC	Digital In	0	0	1.2	V Switched-capacitor clock
18	VREF	Analog In	0	0	1.2	V Reference voltage
19	Vc_o	Analog Out	0	0	1.2	V Monitoring signal
20	Vfb_go	Analog Out	0	0	1.2	V Monitoring signal
21	Vc_ext	Analog Out	0	0	1.2	V Monitoring signal
22	SDA_IO	Digital I/O	0	1.2	1.2	V I2C data
23	SCL_IN	Digital I/O	0	1.2	1.2	V I2C clock
24	RST_IN	Digital I/O	0	0	1.2	V I2C reset
25	VDD	Power	0	1.2	1.2	V Power Supply
26	GND	Ground	0	0	0	V Ground
27	Vout1p2	Analog Out	-1.2	-1.2	-1.2	V NVBG ouptut
28						
29						
30						
31	GNDOi	Ground	0	0	0	V Isolated supply for NVBG
32	GNDri	Ground	0	0	0	V Isolated supply for NVBG
33	GNDi	Ground	0	0	0	V Isolated supply for NVBG
34	VDDi	Power	0	1.2	1.2	V Isolated supply for NVBG
35	VDDRi	Power	0	1.2	1.2	V Isolated supply for NVBG
36	VDDOi	Power	0	1.2	1.2	V Isolated supply for NVBG
37						
38	Vout5	Analog Out	-5.0	-1.2	0	V NVBG output
39						
40						
41						
42						
43						
44						
45						
46						
47	C0_NW	Analog I/O	0	0	1.2	V
48	C0_G	Analog I/O	0	0	1.2	V
49	C0_SB	Analog I/O	0	0	1.2	V
50	R0_P	Analog I/O	0	0	1.2	V
51	R0_N	Analog I/O	0	0	1.2	V

Pin	Name	I/O	Signal level			Description
			Min	Typ	Max	
52	GND0	Ground	0	0	0	V
53	GNDR	Ground	0	0	0	V
54	GND	Ground	0	0	0	V
55	VDD	Power	0	1.2	1.2	V
56	VDDR	Power	0	1.2	1.2	V
57	VDDO	Power	0	1.2	1.2	V
58	NSL	Analog I/O	0	0	1.2	V
59	NDL2	Analog I/O	0	0	1.2	V
60	NBL	Analog I/O	0	0	1.2	V
61	NDL1	Analog I/O	0	0	1.2	V
62	NGL	Analog I/O	0	0	1.2	V
63	PSL	Analog I/O	0	0	1.2	V
64	PDL2	Analog I/O	0	0	1.2	V
65	PBL	Analog I/O	0	0	1.2	V
66	PDL1	Analog I/O	0	0	1.2	V
67	PGL	Analog I/O	0	0	1.2	V
68	PB	Analog I/O	0	0	1.2	V
69	PD1	Analog I/O	0	0	1.2	V
70	PD2	Analog I/O	0	0	1.2	V
71	PD3	Analog I/O	0	0	1.2	V
72	PD4	Analog I/O	0	0	1.2	V
73	PG	Analog I/O	0	0	1.2	V
74	PS	Analog I/O	0	0	1.2	V
75	NB	Analog I/O	0	0	1.2	V
76	ND1	Analog I/O	0	0	1.2	V
77	ND2	Analog I/O	0	0	1.2	V
78	ND3	Analog I/O	0	0	1.2	V
79	ND4	Analog I/O	0	0	1.2	V
80	NG	Analog I/O	0	0	1.2	V
81	NS	Analog I/O	0	0	1.2	V
82	QaB	Analog I/O	0	0	1.2	V
83	QaC	Analog I/O	0	0	1.2	V
84	QaE	Analog I/O	0	0	1.2	V
85	QbB	Analog I/O	0	0	1.2	V
86	QbE	Analog I/O	0	0	1.2	V
87	QbC	Analog I/O	0	0	1.2	V
88						
89						
90						
91						
92						
93						
94	Vss_test					LBL Pre-regulator signal
95	Vin_test					LBL Pre-regulator signal
96	Vout_test					LBL Pre-regulator signal
97	Vbp_bgr					LBL Pre-regulator signal
98	Vbn_start					LBL Pre-regulator signal
99	Outref					LBL Pre-regulator signal
100	Vfb					LBL Pre-regulator signal
101	Ibp_LDO_in					LBL Pre-regulator signal
102	Ibp_LDO_out					LBL Pre-regulator signal

Pin	Name	I/O	Signal level			Description	
			Min	Typ	Max		
103	Vss_prereg					LBL Pre-regulator signal	
104	Vin_prereg					LBL Pre-regulator signal	
105	Vout_prereg					LBL Pre-regulator signal	
106							
107	GND	Ground	0	0	0	V	Ground
108	GNDR	Ground	0	0	0	V	Ground
109	GND0	Ground	0	0	0	V	Ground
110	NSL_2	Analog I/O	0	0	1.2	V	Shared Source of Large NFETs (copy #2)
111	NDL2_2	Analog I/O	0	0	1.2	V	Drain of Large NFET ML2 (copy #2)
112	NBL_2	Analog I/O	0	0	1.2	V	Shared Bulk of Large NFETs (copy #2)
113	NDL1_2	Analog I/O	0	0	1.2	V	Drain of Large NFET ML1 (copy #2)
114	NGL_2	Analog I/O	0	0	1.2	V	Shared Gate of Large NFETs (copy #2)
115	PSL_2	Analog I/O	0	0	1.2	V	Shared Source of Large PFETs (copy #2)
116	PDL2_2	Analog I/O	0	0	1.2	V	Drain of Large PFET ML2 (copy #2)
117	PBL_2	Analog I/O	0	0	1.2	V	Shared Bulk of Large PFETs (copy #2)
118	PDL1_2	Analog I/O	0	0	1.2	V	Drain of Large PFET ML1 (copy #2)
119	PGL_2	Analog I/O	0	0	1.2	V	Shared Gate of Large PFETs (copy #2)
120	PB_2	Analog I/O	0	0	1.2	V	Shared Bulk of PFETs (copy #2)
121	PD1_2	Analog I/O	0	0	1.2	V	Drain of PFET M1 (copy #2)
122	PD2_2	Analog I/O	0	0	1.2	V	Drain of PFET M2 (copy #2)
123	PD3_2	Analog I/O	0	0	1.2	V	Drain of PFET M3 (copy #2)
124	PD4_2	Analog I/O	0	0	1.2	V	Drain of PFET M4 (copy #2)
125	PG_2	Analog I/O	0	0	1.2	V	Shared Gate of PFETs (copy #2)
126	PS_2	Analog I/O	0	0	1.2	V	Shared Source of PFETs (copy #2)
127	NB_2	Analog I/O	0	0	1.2	V	Shared Bulk of NFETs (copy #2)
128	ND1_2	Analog I/O	0	0	1.2	V	Drain of NFET M1 (copy #2)
129	ND2_2	Analog I/O	0	0	1.2	V	Drain of NFET M2 (copy #2)
130	ND3_2	Analog I/O	0	0	1.2	V	Drain of NFET M3 (copy #2)
131	ND4_2	Analog I/O	0	0	1.2	V	Drain of NFET M4 (copy #2)
132	NG_2	Analog I/O	0	0	1.2	V	Shared Gate of NFETs (copy #2)
133	NS_2	Analog I/O	0	0	1.2	V	Shared Source of NFETs (copy #2)

Table 1: Pin functions

3 Building blocks

3.1 Negative Voltage Generator

The Negative Voltage Generator (NVG) provides the reverse bias voltage to deplete the charge collection region of the sensor. The design is based on a switched capacitor converter (charge pump) configured as a negative voltage multiplier. A detailed description of the circuit has been published elsewhere¹; only a brief summary is included in this document.

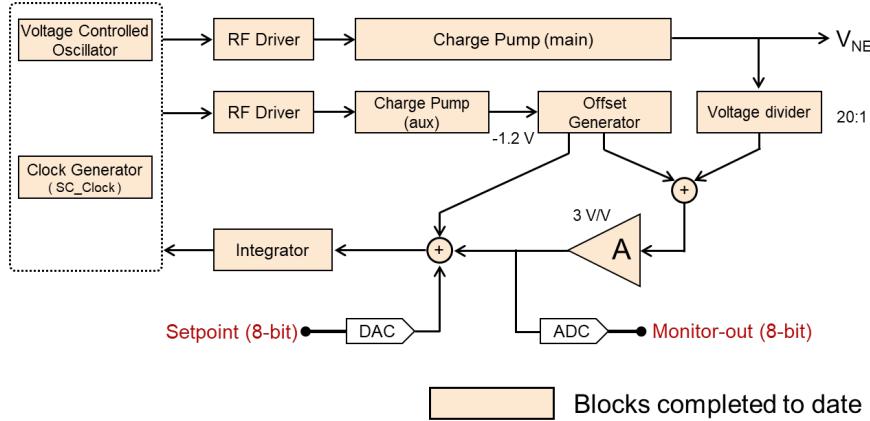


Figure 3: NVG conceptual block diagram

Figure 3 shows a top-level block diagram of the entire closed-loop NVG design. A 5-stage charge pump generates the negative voltage output (V_{NEG}). A single stage auxiliary charge pump generates a negative power supply ($V_{SS} = -1.2\text{ V}$) for the feedback circuits. A voltage-controlled oscillator (VCO) and RF drivers provide the RF clock for the main and auxiliary charge pumps. The RF driver and pump capacitors of the main charge pump are split into 16 identical parallel branches. The number of enabled branches can be set by the thermometer-coded control signal ENcp (16-bit) to provide coarse control over the output voltage, thus reducing the control range of the feedback loop. Thermometer coding also provides robustness to single-event upsets (SEUs). An inverting switched capacitor (SC) amplifier is used to invert the negative output voltage for closed-loop operation. The VCO control voltage, V_c , is set by a switched capacitor integrator in the feedback path. All DC bias currents are generated internally by 4-bit current DACs.

Parameters:

The design supports multiple programmable parameters, as summarized in Table 2.

Parameter	Description
linteg	bias current for the SC integrator
lvco	bias current for the VCO
loff	bias current for the offset generator
ENCP	enable branches of the main charge pump and RF driver
EN<2>	selects VCO control voltage (V_c) - 0 = external control voltage - 1 = output of the SC integrator
EN<1>	Enable RF clock for main charge pump
EN<0>	Enable RF clock for aux. charge pump

Table 2: Programmable control parameters

¹Soumyajit Mandal, Grzegorz W. Deptuch, and Prafull Purohit, An Integrated Negative Bias Voltage Generator for Stitched Pixel Sensors, presented at the *IEEE Midwest Circuits and Systems Conference (MWSCAS)*, Lansing, MI, August 2025.

3.2 I2C Controller

An I2C-based serial interface is used to configure and control individual components in the AncASIC_P1. As shown in Figure 4, the I2C controller supports multiple configuration registers and each configuration register is connected to AncASIC control signals. Table 3 explains the connections between the individual configuration registers and their corresponding AncASIC control signals.

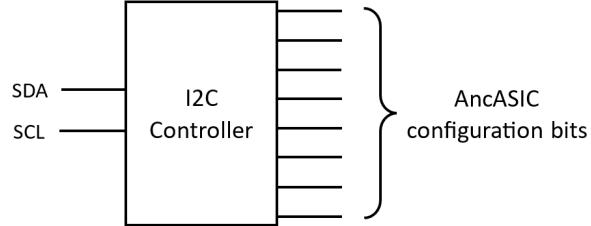


Figure 4: I2C controller.

3.2.1 I2C register map

I2C register	AncASIC parameter
Register[0] <2:0>	$EN <2:0>$
Register[1] <7:0>	$EN_{CP} <15:8>$
Register[2] <7:0>	$EN_{CP} <7:0>$
Register[3] <7:0>	$I_{integ} <15:8>$
Register[4] <7:0>	$I_{integ} <7:0>$
Register[5] <7:0>	$I_{vco} <15:8>$
Register[6] <7:0>	$I_{vco} <7:0>$
Register[7] <7:0>	$I_{off} <15:8>$
Register[8] <7:0>	$I_{off} <7:0>$

Table 3: I2C configuration map

3.2.2 I2C device address

The I2C device address of the chip is hardwired to **6'b111000 + a0**.

3.2.3 I2C write operation

During an I2C write operation, the master controller will send a START condition with the slave address and the R/W bit set for the write operation ($R/W = 0$). After receiving acknowledgment from slave, the master will then send the address of internal register to write. The master sends the register data after receiving another acknowledgment. At this point, the master can either stop the operation by sending the STOP condition or continue the write operation by sending data for the next register, in which case the register address is automatically incremented by the slave. This process is summarized in Fig. 5.

3.2.4 I2C read operation

In order to read data from a slave, the master must first communicate the register address to slave by starting a write operation ($R/W = 0$), followed by the register address. Once the slave acknowledges the register address, the master should restart the sequence by sending a Repeated START (Sr), followed by the slave address for reading ($R/W = 1$). After receiving an acknowledgment, the master releases the data line (SDA) and provides the clock (SCL) to receive the data from slave. The master

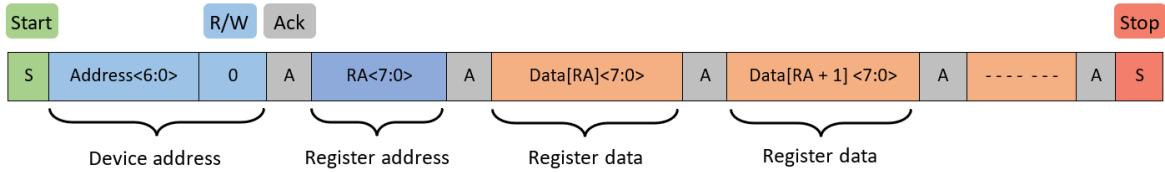


Figure 5: I2C write operation.

will send an ACK after receiving a byte of data to indicate that it is ready for next byte. In this situation, the slave will automatically increment the address after each byte. To stop the read operation, the master will send a NACK and then a STOP condition. This process is summarized in Fig. 6.

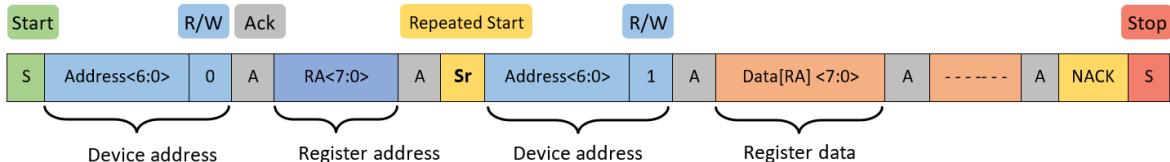


Figure 6: I2C read operation.

Note:

- I2C data bytes are transmitted with Most Significant Bit (MSB) first.
- Addressing registers outside the address space of the channel is generally prohibited. During a write operation, this results in unspecified behavior (it can lead to overwriting different registers), while during a read operation it will result in readout of the value 0xFF.

3.3 Test structures

In order to test the radiation hardness of devices in the XT011 process, several test devices are included in the AncASIC_P1. The connection information and physical dimensions of each device are summarized below.

- Standard V_T NMOS transistors:

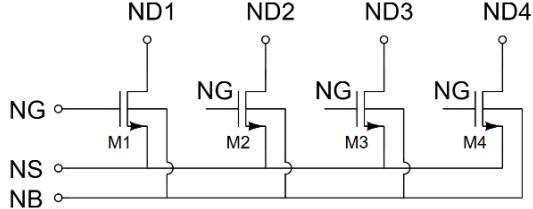


Figure 7: Standard V_T NMOS devices.

NMOS test structures				
	M1	M2	M3	M4
W	1 μm	1 μm	1 μm	1 μm
L	110 nm	150 nm	500 nm	1 μm

Table 4: Physical dimensions

- Standard V_T PMOS transistors:

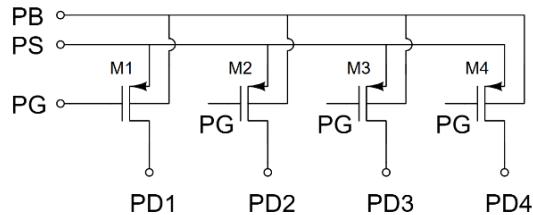


Figure 8: Standard V_T PMOS devices.

PMOS test structures				
	M1	M2	M3	M4
W	1 μm	1 μm	1 μm	1 μm
L	110 nm	150 nm	500 nm	1 μm

Table 5: Physical dimensions

- Standard V_T NMOS transistors:

- Large transistors for leakage measurements.
- Two devices with different Deep Trench Isolation (DTI) enclosure spacing.

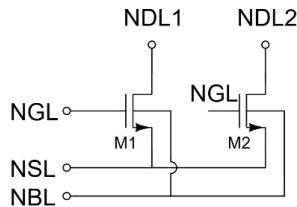


Figure 9: Standard V_T NMOS (large).

Large NMOS devices fingers: 10, multiplier: 10		
	M1	M2
W	100 μm	100 μm
L	150 nm	150 nm
DTI enclosure	Min.	1 μm

Table 6: Physical dimensions

- Standard V_T PMOS transistors:

- Large transistors for leakage measurements.
- Two devices with different Deep Trench Isolation (DTI) enclosure spacing.

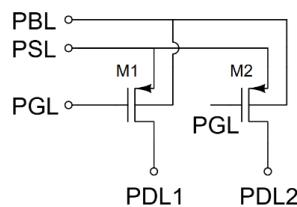


Figure 10: Standard V_T PMOS (large).

Large PMOS devices fingers: 10, multiplier: 10		
	M1	M2
W	100 μm	100 μm
L	150 nm	150 nm
DTI enclosure	Min.	1 μm

Table 7: Physical dimensions

Note: A second copy of all the MOS transistors is included in the AncASIC_P1 to simplify testing. These devices are connected to the inner column of pads visible in Fig. 2.

- Additional devices:

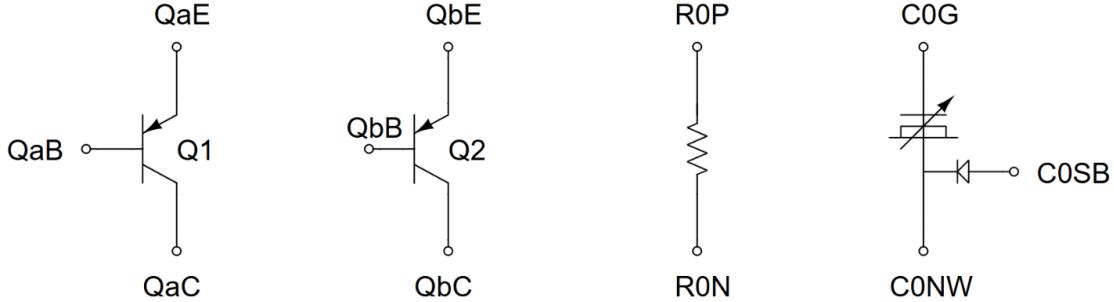


Figure 11: Additional test devices: BJTs, polysilicon resistor, and MOS capacitor.

	Device	Value	Description
Q1	qpva		PNP transistor
Q2	qpvb		PNP transistor
R0	Poly resistor	2027.37 Ω	
C0	Mosvc	7 $\mu\text{m} \times 7 \mu\text{m}$	

Table 8: Additional devices available for testing

3.4 Transmission line (passthrough)

The high-speed data coming from the sensor will be collected by a transceiver ASIC (IpGBT) and sent to the control room. Several options for the hardware implementation are under consideration and one of the options is to route this data through the AncASIC. In order to test and understand the effects of sending high-speed data through the AncASIC, a passthrough differential transmission line is implemented in this prototype using the thick top metal. Fig. 12 summarizes the layout of this structure, which is designed to have a characteristic impedance of $Z_0 \approx 100 \Omega$.



Figure 12: Differential transmission line for testing high-speed data transmission.

The geometric parameters of the transmission line are listed below:

- Trace width = 10 μm
- Trace spacing = 6 μm
- Trace length = 2500 μm

3.5 CML Transceiver

The CML transceiver circuits are designed to enable DC-coupled slow control links between adjacent serially-powered AncASIC chips. Simulations show successful transmission of non-return-to-zero (NRZ)-coded data up to 320 Mb/s between chips with an end-to-end time delay² of 1.06 ns.

3.5.1 Transmitter

Fig. 13 shows the schematic of the CML transmitter. The output common-mode voltage of the transmitter should remain near V_{SS} (0 V) to allow DC coupling to the next chip in the serial-powered chain. Accordingly, the design uses a PMOS differential pair. Other design parameters are summarized below.

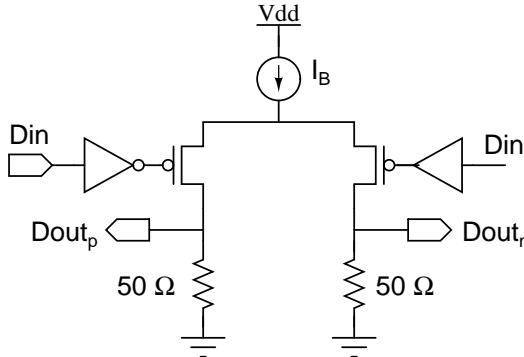


Figure 13: CML transmitter.

- Differential output impedance: $Z_o = 100 \Omega$
- Bias current: $I_B = 8 mA$
- Output swing (into a matched load): $V_{out} = 400 mV_{pp}$

3.5.2 Receiver

Fig. 14 shows the schematic of the CML receiver. The circuit supports input common-mode voltages near V_{DD} (1.2 V) to allow DC coupling from the previous chip in the serial-powered chain. Accordingly, the design uses an NMOS differential pair buffered with source followers. The output is generated by a CMOS inverter with resistive feedback to ensure rail-to-rail output swing will little duty cycle distortion. Other design parameters are summarized below.

- Differential input impedance: $Z_i = 100 \Omega$
- Bias current: $I_{B1} = 50 \mu A$
- Output swing: rail-to-rail (1.2 V)

²Not including additional time delays due to the transmission line between the chips.

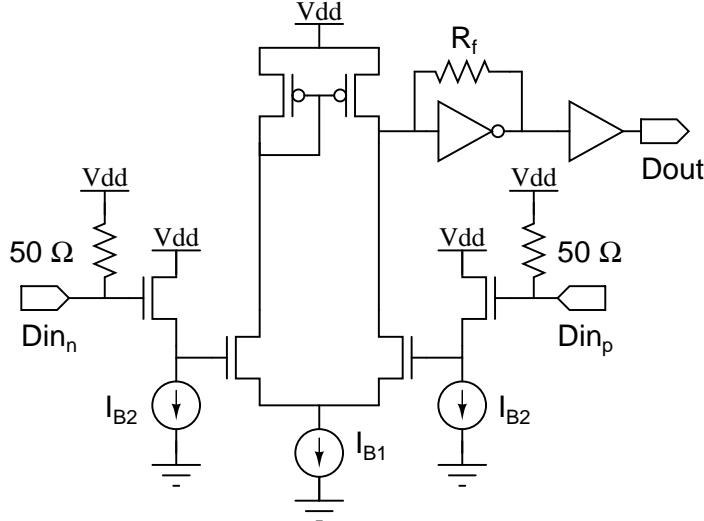


Figure 14: CML receiver.

4 Test plan

4.1 Negative Voltage Generator

This section describes the test procedure suggested to verify the functionality of the proposed negative voltage generator (NVG). It is assumed that the feedback loop used for voltage regulation has been enabled. If necessary, the feedback loop can be disabled by setting a control signal over the included I²C interface.

- **Output range:** Begin by setting the load capacitance, C_L , and switched-capacitor clock frequency, f_{SC} , to reasonable values (for example, 1 nF and 1 MHz, respectively). Next, vary the reference voltage, V_{REF} , over the range 0-0.8 V and verify that the no-load output voltage in steady-state obeys the expected relationship, which is

$$V_{OUT} = -(20/3)V_{REF}.$$

Repeat the output voltage measurements for load currents, I_L , varying over the range 0-1 mA and analyze the results to estimate the load regulation, $\Delta V_{OUT}/\Delta I_L$.

- **Line regulation:** Measure the steady-state output voltage, V_{OUT} , as a function of the supply voltage, V_{DD} , over the range 1-1.4 V while keeping V_{REF} fixed. Analyze the results to estimate the line regulation, $\Delta V_{OUT}/\Delta V_{DD}$.
- **Transient response:** Use an oscilloscope to measure the output voltage, v_{OUT} , during startup, i.e., immediately after V_{DD} has been applied. Analyze the results to estimate the rise time, settling time, and peak overshoot as a function of V_{REF} . Repeat for different values of the load current, I_L .
- **Loop bandwidth:** Repeat the transient response tests for different values of f_{SC} , which is proportional to the loop bandwidth when other parameters are kept constant. Additionally, verify that loop stability can be maintained as C_L increases by decreasing the value of f_{SC} .
- **Power supply rejection ratio (PSRR):** Set V_{REF} and I_L to fixed values. Next, inject a small-signal sinusoidal ripple into the supply voltage, for example by generating V_{DD} from a signal generator rather than a DC power supply. Measure the amplitude of the resulting output ripple, $V_{OUT,AC}$, as a function of the ripple frequency. Finally, estimate the PSRR (in dB) as a function of frequency as the ratio

$$PSRR(f) = \frac{V_{OUT,AC}(f)}{V_{DD,AC}}$$

where $V_{DD,AC}$ is the amplitude of the input ripple.

- **Output noise and ripple:** Due to the use of periodic waveforms within both the charge pump and the feedback loop (namely, the RF and switched-capacitor clock signals), V_{OUT} exhibits periodic ripple even when V_{DD} is ripple-free. Additionally, V_{OUT} exhibits random noise. To characterize these error sources, use an oscilloscope to record V_{OUT} in steady-state for various values of V_{REF} and I_L . Analyze the results to estimate the output histogram, peak and rms variability, and frequency spectrum.
- **Temperature:** Repeat all earlier tests for ambient temperatures between 25°C and 85°C. The use of an environmental chamber is recommended for this purpose.

4.2 CML transceiver

4.2.1 Single chip tests

Drive transmission lines of different lengths with a pseudorandom binary sequence (PRBS) and measure the resulting transmission loss, time delay, and eye diagram for different data rates.

4.2.2 Daisy-chain tests

Connect multiple chips with appropriate supply voltages (based on the serial powering scheme) as shown in Fig. 15. Drive PRBS data through the chain and then measure:

- Transmission loss between stages
- Time delay from each stage
- Eye diagram of the output data stream on each chip

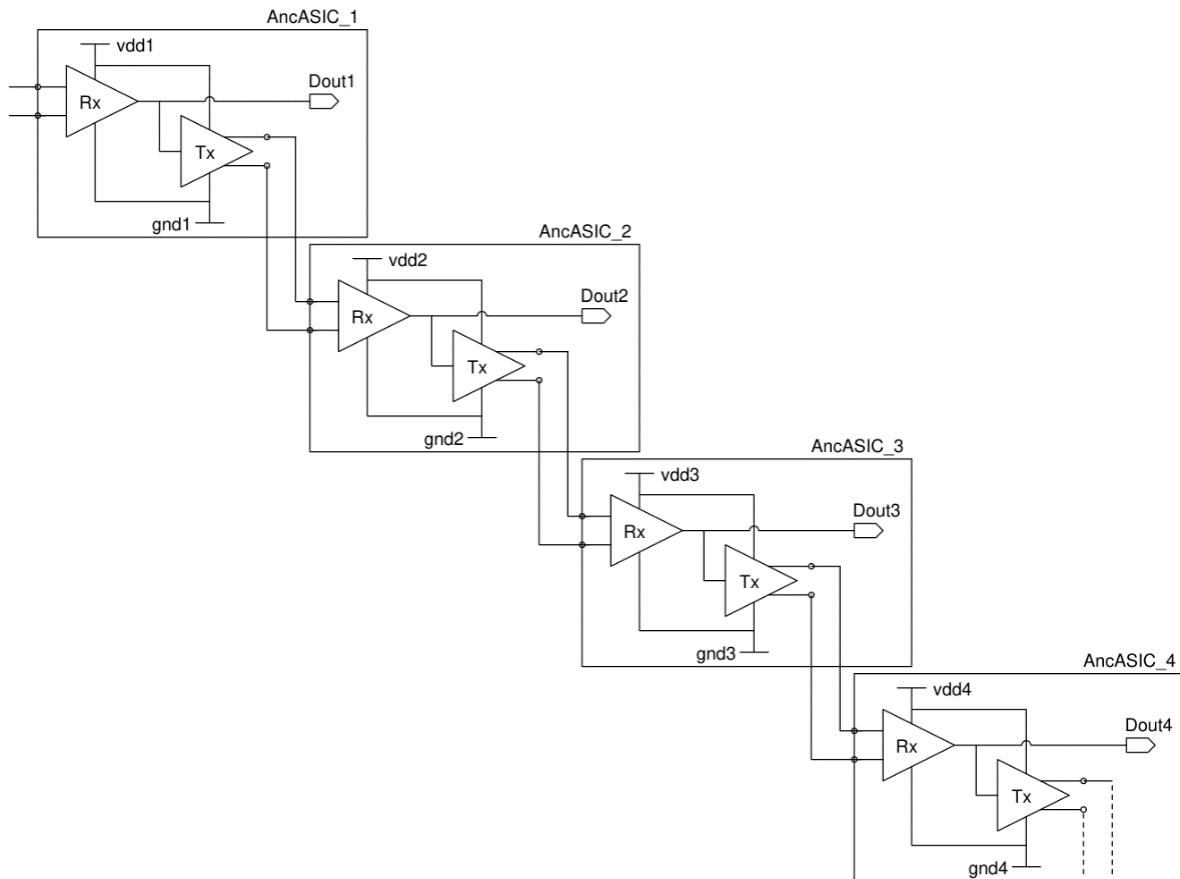


Figure 15: Testing DC coupled signal transmission.

4.3 Test structures

To study the effects of total ionizing dose (TID) and/or displacement damage to devices in the XT011 process, a few test structures (devices) are included in the AncASIC_P1 prototype. The goal is to study the change in device performance as a result of steady-state irradiation.

4.3.1 Measurement sequence

Fig. 16 shows an example measurement flow for studying TID effects on MOS transistors and other devices. The suggested flow begins with making the initial electrical measurements at room temperature. The devices should be irradiated later up to 10 Mrad and the electrical parameters should be measured in frequent intermediate steps, for example 10 krad, 100 krad, 1 Mrad, and 10 Mrad. It is also useful to perform similar measurements during annealing with and without voltage bias at different temperatures.

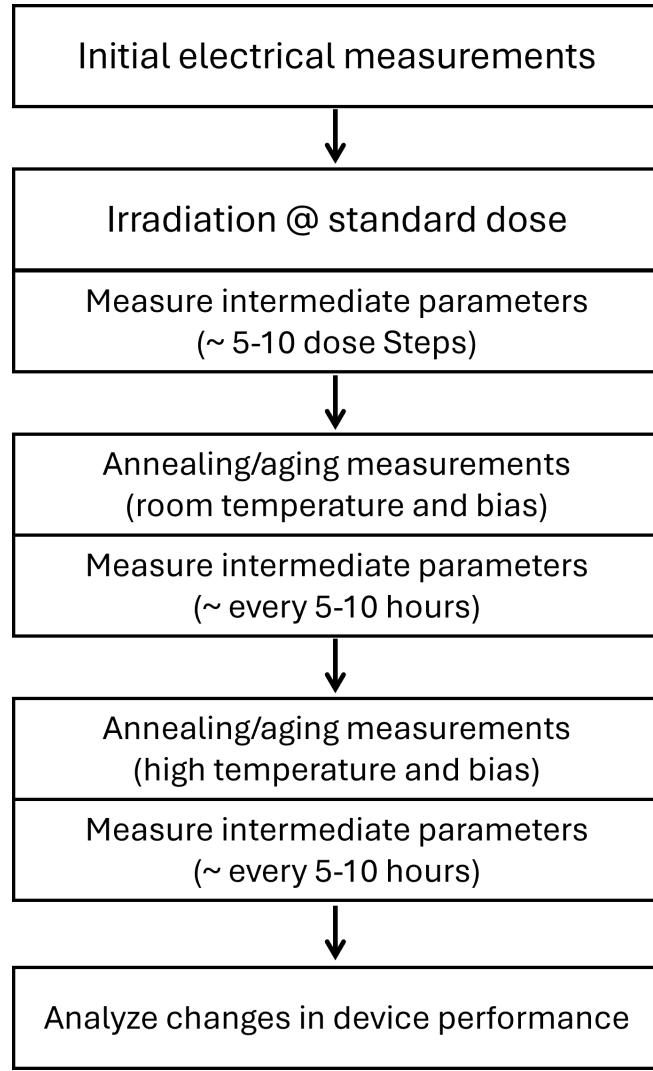
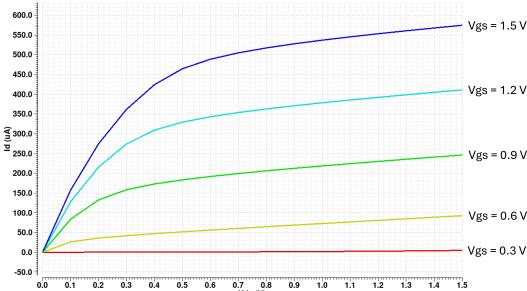


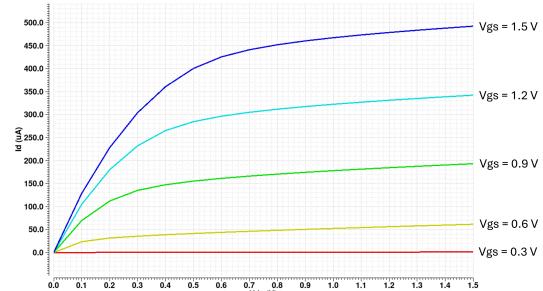
Figure 16: TID measurement flow

4.3.2 Reference electrical measurements

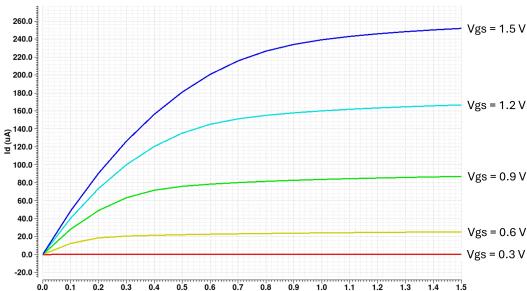
For reference, the simulated V_{DS} - I_D curves of the NMOS and PMOS test devices are summarized in Figs. 17 and 18, respectively. Note that these results correspond to the “typical” (tt) process corner.



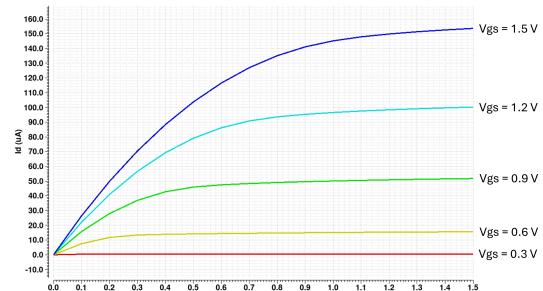
(a) NMOS1



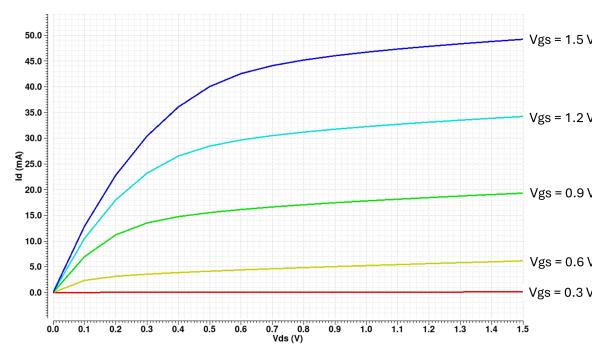
(b) NMOS2



(c) NMOS3



(d) NMOS4



(e) NMOS-L

Figure 17: NMOS I/V curves.

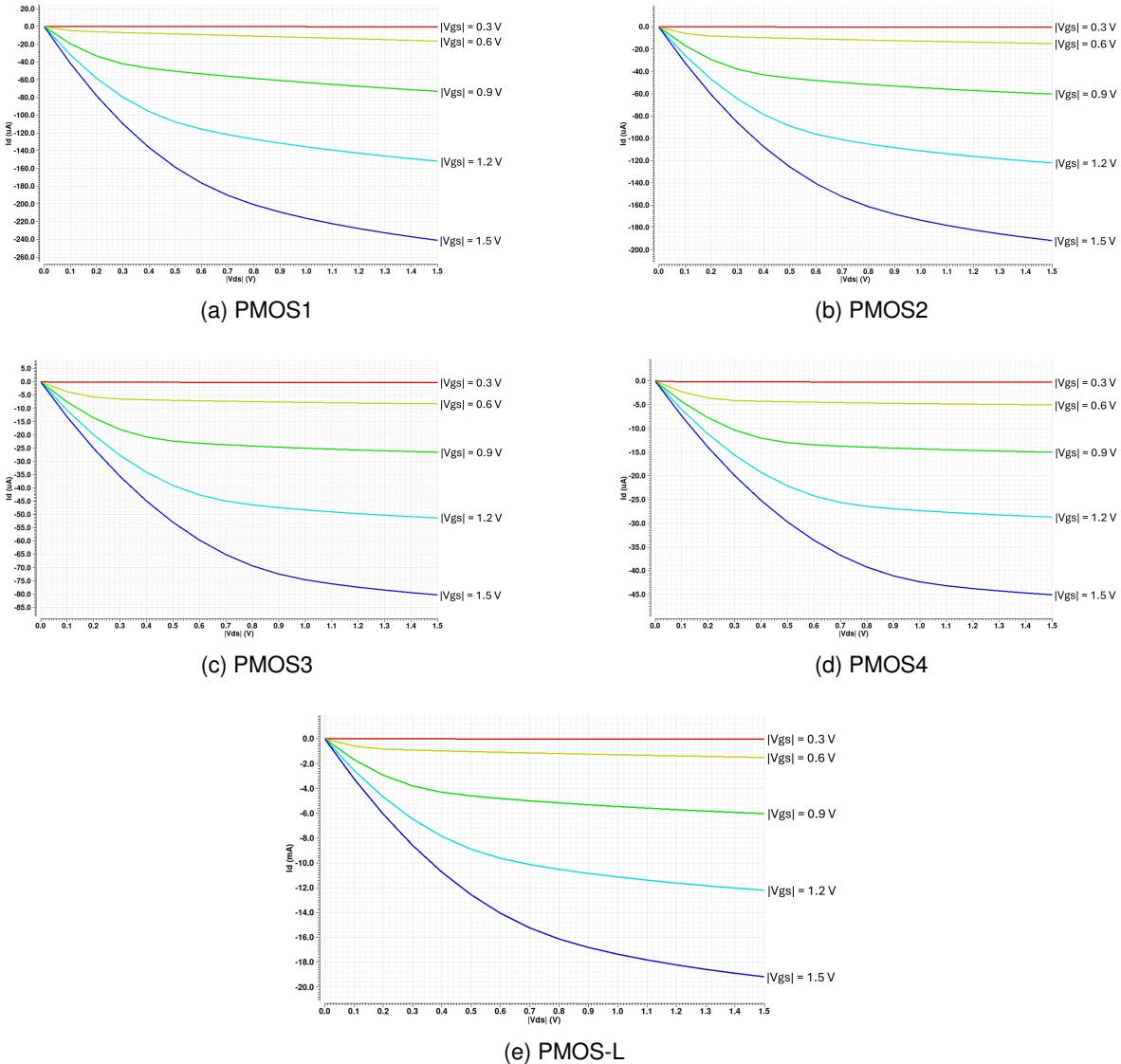


Figure 18: PMOS I/V curves.