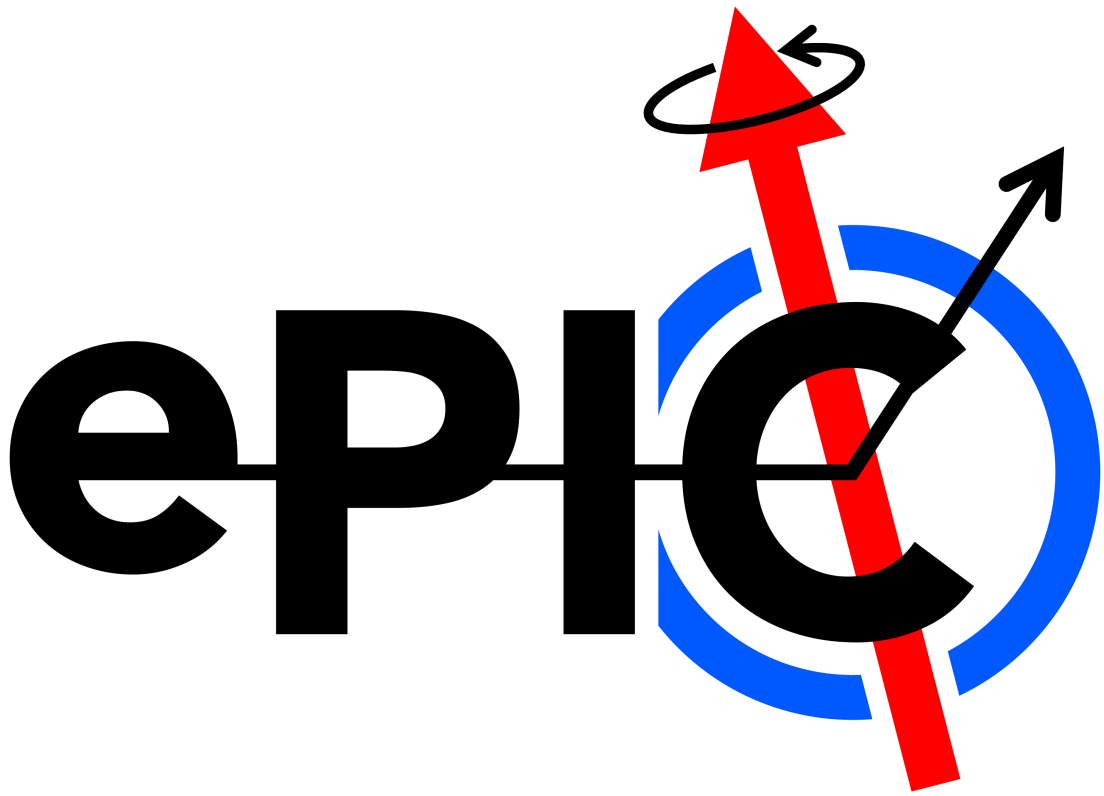
ePIC SVT - Specification for EIC-LAS and Ancillary Chip

March 25, 2025



Revision History

Revision	Date	Author(s)	Description
1.0	25.03.25	All	First Version

1 Introduction

This document contains specifications for the chips needed for construction of the ePIC SVT - the EIC-LAS and the ancillary chip.

2 Negative Voltage Generator (NVG)

This block provides a negative voltage to back-bias the EIC-LAS. This is necessary because the level of the back-bias voltage is sufficiently low, and requried to be sufficiently precise, that it is needed to generate the negative voltage relative to the local ground in the serial powering chain.

2.1 Specifications

Negative Bias Generator Specification				
Specification	Unit	Value	Comment	Status
Voltage Range	V	-1 to -5	Relative to local ground	Confirmed in simulation
Current Capacity	mA	1		Dev
Voltage Ripple	mV	< 0.15		Confirmed in simulation: 150 μV_{pp} for $V_{OUT} = -1.5$ V, $C_L = 1$ nF
Power	mW	< 15		Confirmed in simulation: $\sim$11 mW for $V_{OUT} = -1.5$ V
Supply Voltage	V	$1.2 \pm 10\%$		Confirmed in simulation from 1.1 V - 1.3 V
Area	µm^2	$< 4 \times 10^5$		Initial version: $250\ \mu$m $\times$ $1000\ \mu$m $= 2.5 \times 10^5\ \mu$m^2

2.2 Testing Plan

This section describes the suggested testing procedure for verifying the functionality of the proposed negative voltage generator (NVG). It is assumed that the feedback loop used for voltage regulation has been enabled. If necessary, the feedback loop can be disabled by setting a control signal over the included I^{2}C interface.

- **Output range**: Begin by setting the load capacitance, C_L, and switched-capacitor clock frequency, f_{SC}, to reasonable values (for example, 1 nF and 1 MHz, respectively). Next, vary the reference voltage, V_{REF}, over the range 0-0.8 V and verify that the no-load output voltage in steady-state obeys the expected relationship, which is

  $$V_{OUT} = -(20/3)V_{REF}.$$

  Repeat the output voltage measurements for load currents, I_L, varying over the range 0-1 mA and analyze the results to estimate the load regulation, $\Delta V_{OUT}/\Delta I_L$.

- **Line regulation**: Measure the steady-state output voltage, V_{OUT}, as a function of the supply voltage, V_{DD}, over the range 1-1.4 V while keeping V_{REF} fixed. Analyze the results to estimate the line regulation, $\Delta V_{OUT}/\Delta V_{DD}$.

- **Transient response**: Use an oscilloscope to measure the output voltage, v_{OUT}, during startup, i.e., immediately after V_{DD} has been applied. Analyze the results to estimate the rise time, settling time, and peak overshoot as a function of V_{REF}. Repeat for different values of the load current, I_L.

- **Loop bandwidth**: Repeat the transient response tests for different values of f_{SC}, which is proportional to the loop bandwidth when other parameters are kept constant. Additionally, verify that loop stability can be maintained as C_L increases by decreasing the value of f_{SC}.

- **Power supply rejection ratio (PSRR)**: Set V_{REF} and I_L to fixed values. Next, inject a small-signal sinusoidal ripple into the supply voltage, for example by generating V_{DD} from a signal generator rather than a DC power supply. Measure the amplitude of the resulting output ripple, $V_{OUT,AC}$, as a function of the ripple frequency. Finally, estimate the PSRR (in dB) as a function of frequency as the ratio

  $$PSRR(f) = \frac{V_{OUT,AC}(f)}{V_{DD,AC}}$$

  where $V_{DD,AC}$ is the amplitude of the input ripple.

- **Output noise and ripple**: Due to the use of periodic waveforms within both the charge pump and the feedback loop (namely, the RF and switched-capacitor clock signals), V_{OUT} exhibits periodic ripple even when V_{DD} is ripple-free. Additionally, V_{OUT} exhibits random noise. To characterize these error sources, use an oscilloscope to record V_{OUT} in steady-state for various values of V_{REF} and I_L. Analyze the results to estimate the output histogram, peak and rms variability, and frequency spectrum.
- **Temperature**: Repeat all earlier tests for ambient temperatures between 25°C and 85°C. The use of an environmental chamber is recommended for this purpose.

3 SLDO

This block provides powering for the EIC-LAS. It generates the four required output voltages from a single input current. The reason for this is to reduce the amount of material in the detector.

3.1 Overview

The SLDO consists of three main blocks:

- SLDO: The Shunt LDO circuit itself.
- Bandgap: A bandgap used to generate biases for the SLDO circuit
- Pre-regulator: An LDO and bandgap sitting in front of the other blocks which power them and help with their start-up.

These are shown in Figure 1.

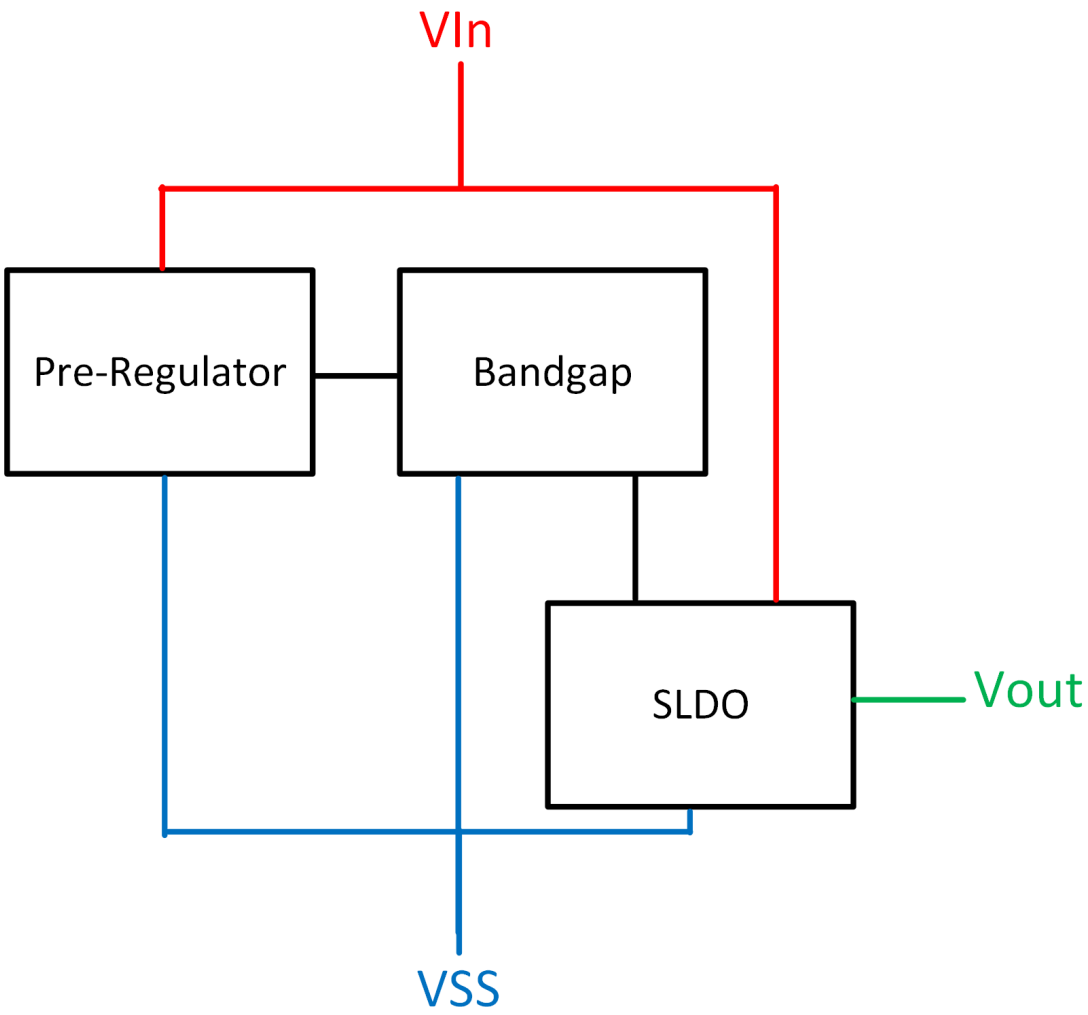


Figure 1: SLDO Overview

The SLDO is quite a complex circuit, so its operation is illustrated in Figure 2. It operates as follows:

1. The total current in the SLDO is the sum of the current going out to the load, and the current being shunted to ground - $Iin = Iload + Ishunt$.
2. The circuitry controlling the pass transistor compares the output voltage Vload to a target reference and adjusts the pass transistor gate so that this is acheived.

3. The desired current through the SLDO (Iin) is selected using the resistor R3. The reference current in the R3 branch ($Vin/R3$) is compared to a small fraction of the pass transistor current mirrored by the pass transistor control circuitry (Iin/k). The transistors M1 and M2 convert these currents to voltages for comparison. The shunt transistor control circuitry increases or decreases $Ishunt$ until the two voltages are equal, and by extension

$$Iin/k \approx Vin/R3 \tag{1}$$

4. Any deviations in $Iload$ will be compensated by changes to $Ishunt$ so that $Iload$ remains constant.

5. Re-arranging Eqn 1 we see that the input impedance of the SLDO (Vin/Iin) is $R3/k$.

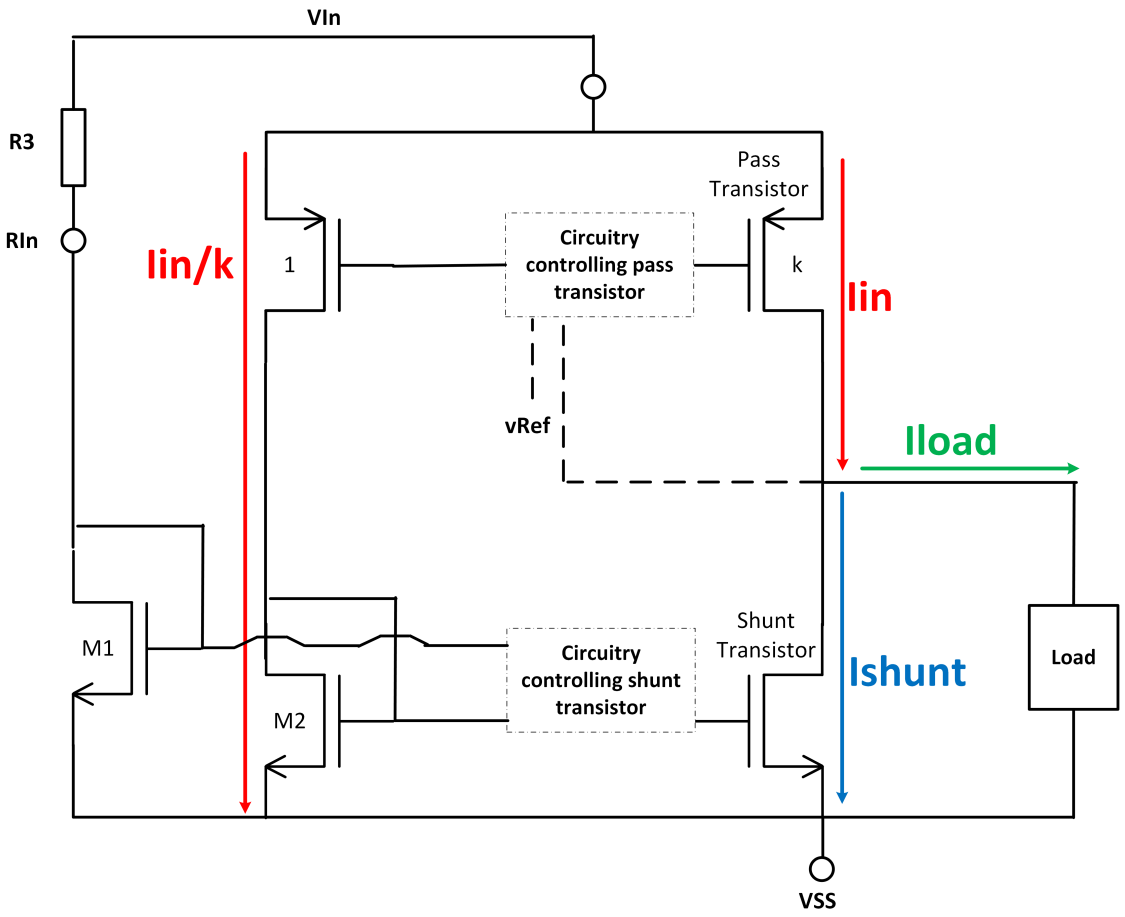


Figure 2: SLDO Overview

The SLDO also provides a load over-current protection function which switches the output to high impedance when it detects an over-current situation in the load. In terms of setting up the SLDO for test or operation, this circuit is the most important because most of the control siginals apply to it. Its operation is shown in Figure 3 and described below:

- An overcurrent condition in the load is detected as the shunted current falling below a preset threshold. This triggers the ”disable” signal.
- To avoid small transients triggering a shutdown, the disable signal is delayed and used as the clock input to a D-type flip-flop. The D input is the original disable signal. This means only events which cause a disable pulse longer than 100us lead to a shutdown.
- The multiplexer I1 allows to select between the internally generated Ishunt signal and an external version, so that, for example, the AncBrain could control shutdown instead of the analog circuit.

- If the flip flop successfully clocks in a ”1” - from a pulse longer than 100us, then it closes a switch around the pass transistor, shorting it out and putting the output in a high impedance mode.
- Since the core of this circuit is a memory element, the overcurrent condition is latched and needs to be reset to return to operation. This is the purpose of the activate and reset signals. Note that a ”1” stored in the latch represents the condition in which the output is high impedance, and a ”0” represents normal operation. Detection of an overcurrent condition results in a ”1” being loaded. The control signals are:
  - reset_OCP_N: Resets the flip-flop to zero, thereby enabling the output. This can be used to re-start after an overrcurrent condition, or, if held low, prevents the overcurrent protection from engaging.
  - activate_OCP_N: Resets the flip-flop to zero, thereby engaging the overcurrent protection. Can be used hold the output in tri-state until you want to enable it.

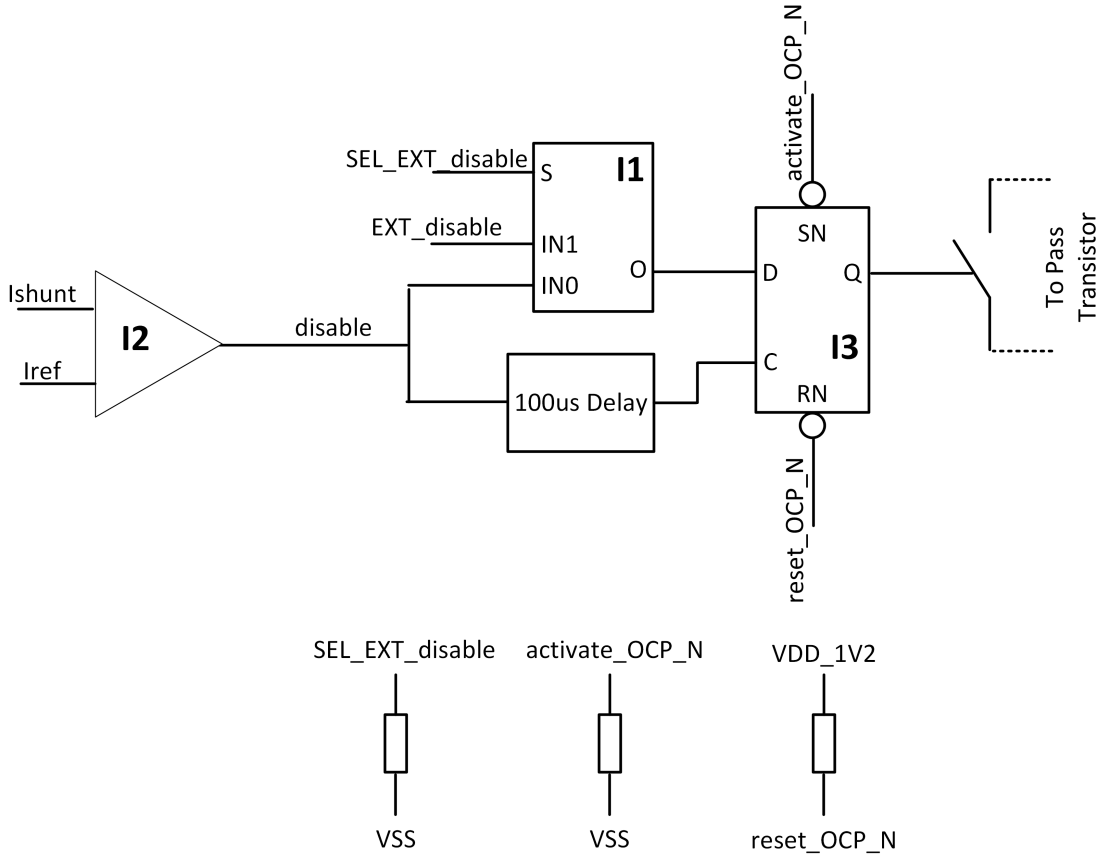


Figure 3: SLDO Overview

3.2 Modes

Broadly speaking, the control signals described above allow the chip to be operated in two main modes. In Mode 0, all outputs are in the tri-state condition at powerup and need to be enabled once the current/voltage ramp is over. In Mode 1, the outputs are enabled at power up and ramp up as the input current/voltage is ramped. These are described in more detail below.

3.2.1 Mode 0

The controls to operate in Mode 0 are:

- activate_OCP_N: Start at 1, set to 0 to allow outputs to be enabled.

- reset_OCP_N: Pulse low to enable outputs. Keep low if you want to disable overcurrent protection.

This is illustrated in Figure 4

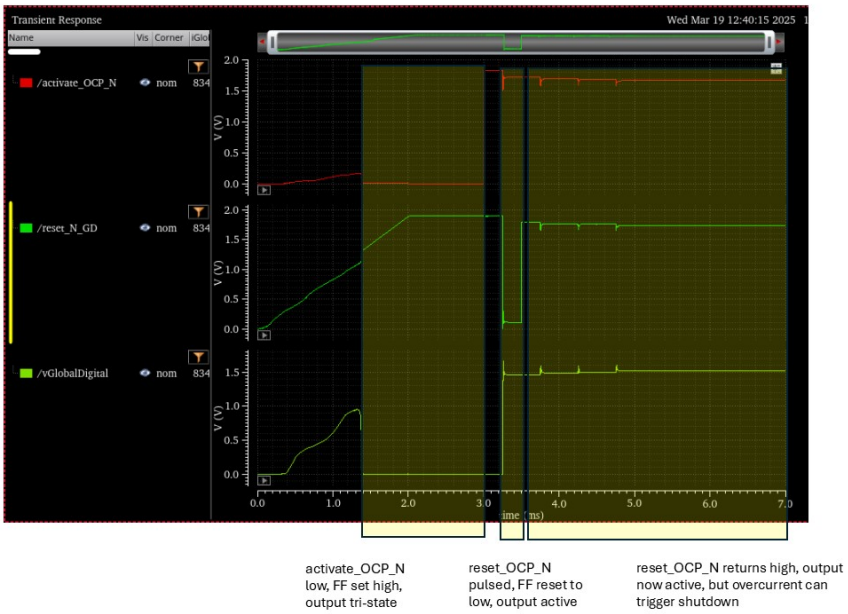


Figure 4: Signal timing for Mode 0

3.2.2 Mode 1

The controls to operate in Mode 1 are:

- activate_OCP_N: 1
- reset_OCP_N: 0 (set to 1 after startup to allow overcurrent detection to function)

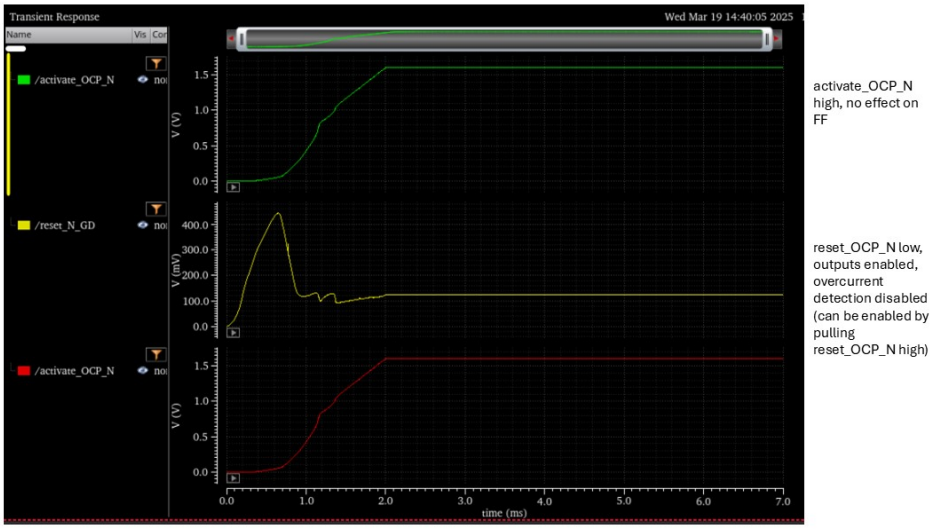


Figure 5: Signal timing for Mode 1

Currently, the SLDO is implemented in a small MPW structure for testing. This is referred to as MPW2_SLDO. This structure exposes several key voltages for test and debug purposes.

3.3 Specifications

Shunt LDO Specification						
Specification	**Unit**	**Value**			**Comment**	**Status**
		Min	**Typ**	**Max**		
Voltage Output	V	1.1	1.32	1.4		Dev
No. of Channels			5		Inc 1 for AncASIC	Dev
Current Capacity	A	0	0.95	1.5	Per Channel	Dev
Power	W		0.45	0.6	10% shunt current	Dev
Input Voltage	V		1.55			Dev
Area	μm^2		40000			Dev
Start-up Ramp Rate	kV/s		3.1			Dev
Over-Voltage Limit	V		2.0			Dev
Max Current @ Over-Voltage Limit	A					Dev
PSRR (Line Regulation)	dB@40mA,1kHz dB@950mA,1kHz dB@40mA,160MHz dB@950mA,160MHz		-58 -40 -5 -5			Dev Dev Dev Dev

3.4 Pinout

The pinout of the SLDO, its control signals and test outputs and voltage ratinga are as described in the following sections.

3.4.1 Maximum Ratings

All pins have the following voltage ratings.

	Min	**Max**	**Absolute Max**
Voltage Rating	0	1.6	1.8

3.4.2 Pin Functions

This section describes the pins of the SLDO circuit. Note that, since this document is intended to cover both the MPW test structure and the eventual SLDO, some pins are marked ”MPW only”. These pins will not exist on the final device.

The eventual AncASIC will have a monitoring ADC as part of the AncBrain. The table also indicates which pins should be connected to this monitoring ADC, and whether those pins should be monitored regularly (M) or only checked on-request (OR). The first case is appropriate for pins whose value might indicate a fault condition, the second is for those whose value might be used to debug an issue.

Pin	Type	Function	Default
Vin	Power (M)	Input current/voltage	
Rin	Analog I/O	Input pin for current setting resistor	
VDD_pre_reg	Analog I/O (OR)	Test output for current from pre-regulator	
Vout	Power (M)	Regulated output voltage to load	
Iin_12u_OVP	Analog I/O (OR)	Bias current for use by OVP circuit	12uA out of pad
VOUT_OVP	Analog I/O (OR)	Bias voltage for use by OVP circuit	
control$< 4:0 >$	Digital Input	5 bit control of output voltage	
reset_OCP_N	Digital Input[1]	Reset signal for overcurrent protection. Re-enables output (active low)	1[2]
activate_OCP_N	Digital Input[1]	External signal to put output into tri-state (active low)[3]	0[2]
EXT_disable	Digital Input[1]	External signal to override internal overcurrent disable signal	0[2]
SEL_EXT_disable	Digital Input[1]	Selects between internal overcurrent shutdown signal and EXT_disable	0[2]
dis_latch_qn	Digital Output[1]	Indicates that the overcurrent shutdown has been triggered (active low). On the MPW this is a test output. For the AncBrain it can indicate status.	
VOFS	Analog I/O (OR)	Test output for internal offset voltage generation. Can also be used to forcibly override internal signal.	
VG_PASS	Analog I/O (OR)	Test output for pass transistor gate voltage.	
VBG_pre	Analog I/O (OR)	Test output for pre_regulator bandgap voltage. Can also be used to forcibly override internal signal.	
VBG	Analog I/O (OR)	Test output for main bandgap voltage. Can also be used to forcibly override internal signal.	
Ishunt	Analog I/O (OR)	Test output for shunt transistor gate voltage	
VSENSE	Analog I/O	Sense line for output voltage. Connect to Vout at point of use.	
test_SPARE$< 10:0 >$ (MPW only)	Analog I/O	Unconnected. Spare in case FIB connection for debugging is needed	

1. All digital I/Os are supplied through analogue pads
2. Using on-chip 20kohm resistor
3. The overcurrent protection tri-states the output of the SLDO. This can also be triggered externally using the activate signal to disable the SLDO output if desired.

3.4.3 Physical Pinout

The physical pinout of the chip is as shown in Figure 6.

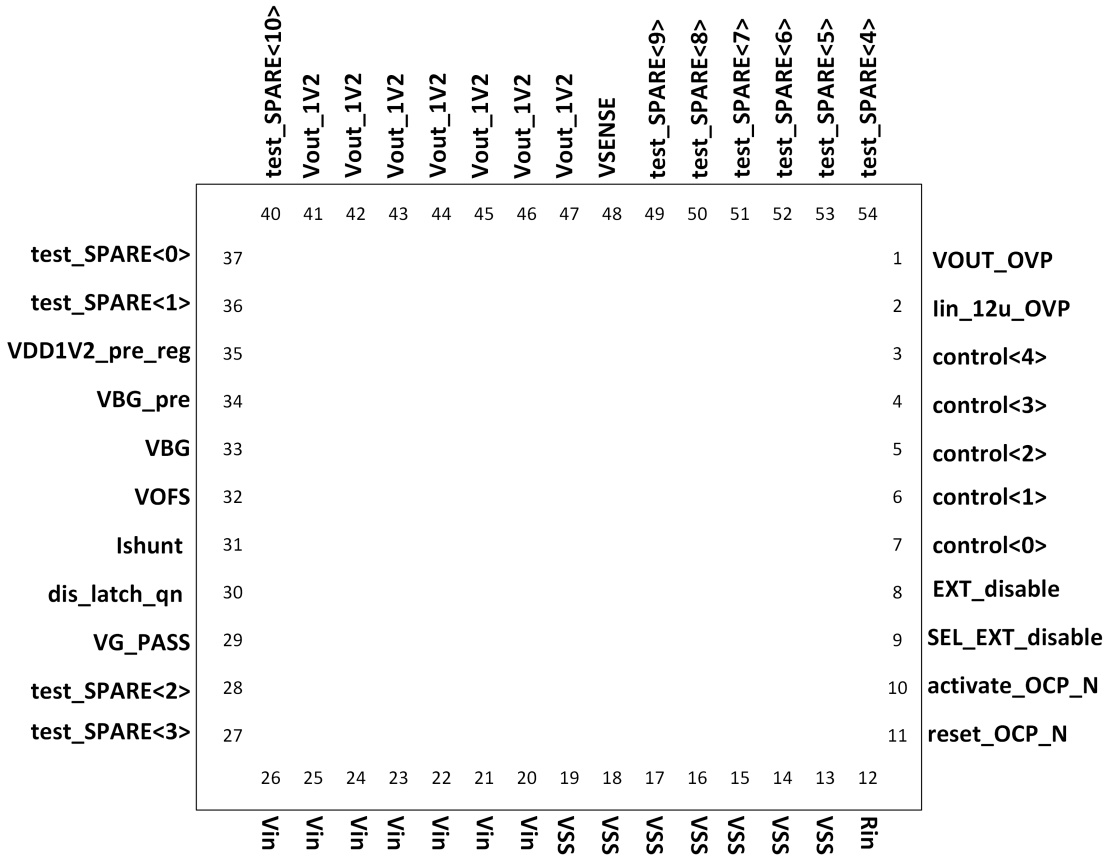


Figure 6: Physical Pinout

Details of the sizing are shown in Figure 7.

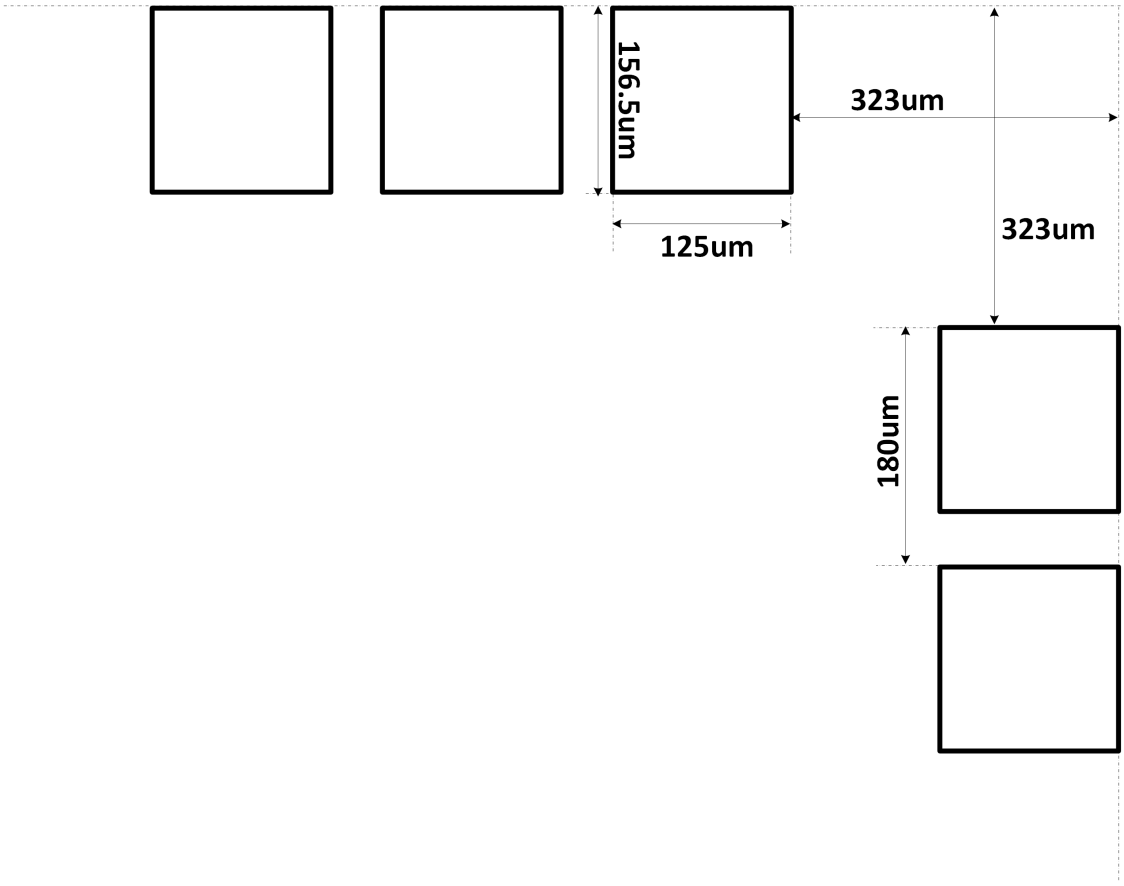


Figure 7: Detail of Physical Pinout

3.5 Test Plan - MPW2_SLDO

This section deals with the testing of the SLDO test structure (MPW2_SLDO). It outlines the suggested format of the test system, and details the required tests.

3.5.1 Recommended Test Board

Figure 8 shows an example of a possible tests system for MPW2_SLDO. This suggestion is guided by the following principles.

- Keep the board with the chip as simple as possible.
- Allow measurement of PSRR.
- Allow the analog I/Os to be both driven and read.
- Ensure the test system can test a load overcurrent condition.

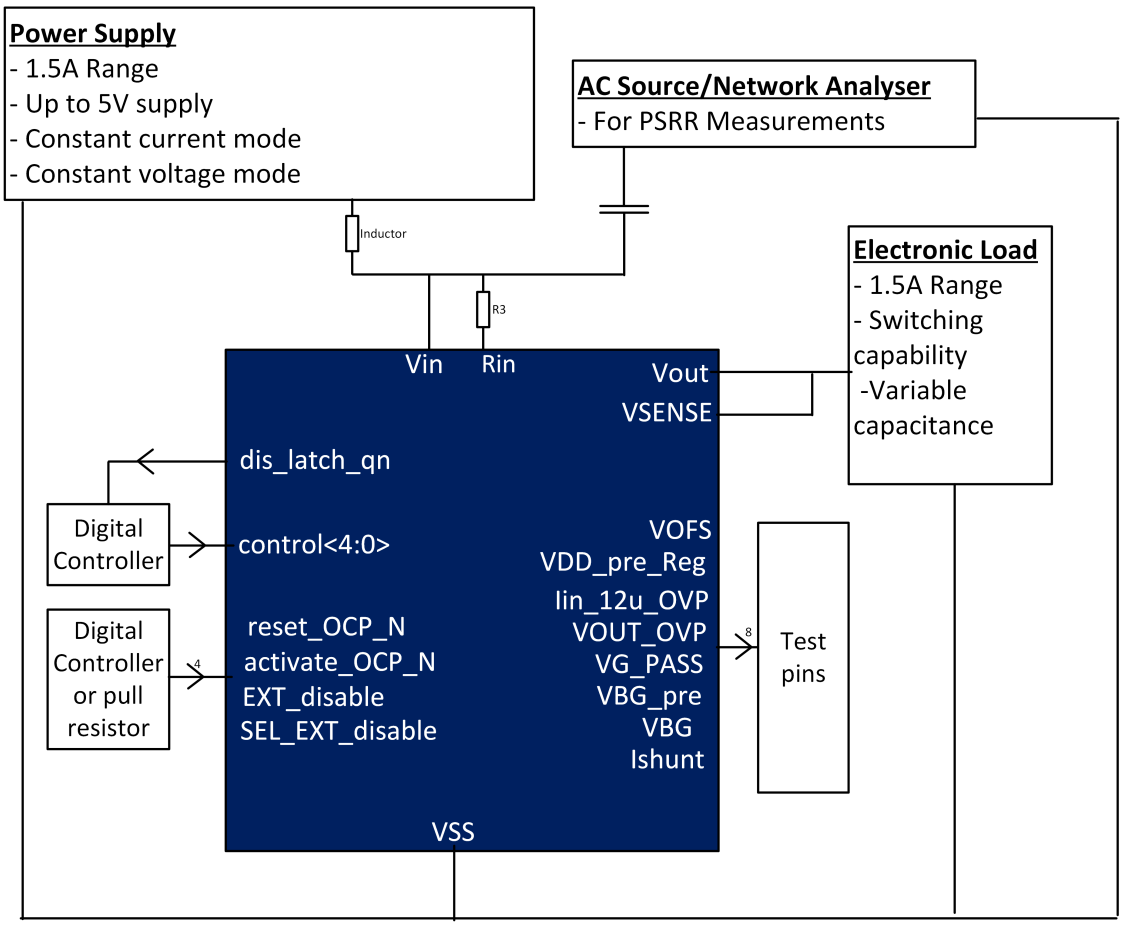


Figure 8: Suggested Test System

3.5.2 Required Tests

This section details the tests that need to be performed on MPW2_SLDO. All the tests below need to be performed in the conditions outlined in Table 2. The only exceptions to this are the DAC Scans and irradation tests. To simplify these, we will select a single condition. To ease early testing, a first pass of the tests can be carried out at room temperature. Temperature stability can be re-visited later.

Condition	Values
Load Capacitance	10nF, 100nF, 1uf, 10uF
Load Current	40mA, 500mA, 900mA
Temperature Range	-20°, 27°, 60°, 105°

Table 2: Test Conditions

3.5.2.1 Mode 1 Powerup

1. Set up the test system. Configure the control signals as shown in

Signal	Value
control$< 4:0 >$	10000
reset_OCP_N	0
activate_OCP_N	1
EXT_disable	0
SEL_EXT_disable	0

Table 3: Test Conditions

2. Ramp up the supply voltage to the target level
3. For each test condition, measure and record the output trace from Vout

3.5.2.2 Mode 1 PSRR

1. Set up the test system. Configure the control signals as shown in

Signal	Value
control$< 4:0 >$	10000
reset_OCP_N	0
activate_OCP_N	1
EXT_disable	0
SEL_EXT_disable	0

Table 4: Test Conditions

2. Ramp up the supply voltage to the target level
3. For each test condition, measure and record the Power Supply Rejection Ratio (PSRR) at the Vout pin.

3.5.2.3 Mode 1 Ramp Rate

1. Set up the test system. Configure the control signals as shown in

Signal	Value
control$< 4:0 >$	10000
reset_OCP_N	0
activate_OCP_N	1
EXT_disable	0
SEL_EXT_disable	0

Table 5: Test Conditions

2. Select a single test condition based on previous results
3. Ramp the supply from 0 to the target voltage at over 100us, 1ms, 10ms, 100ms and 1s
4. For each value, record the output trace and final value of Vout.

3.5.2.4 Mode 1 DAC Scan

1. Set up the test system. Configure the control signals as shown in

Signal	Value
control$< 4:0 >$	10000
reset_OCP_N	0
activate_OCP_N	1
EXT_disable	0
SEL_EXT_disable	0

Table 6: Test Conditions

2. Ramp up the supply voltage to the target level
3. Select a single test condition from the preceding tests.
4. Scan the 31 possible DAC codes. Record the value of Vout and plot against the code.

3.5.2.5 Mode 1 Irradiation

1. Set up the test system. Configure the control signals as shown in

Signal	Value
control$< 4:0 >$	10000
reset_OCP_N	0
activate_OCP_N	1
EXT_disable	0
SEL_EXT_disable	0

Table 7: Test Conditions

2. Select a single test condition from the preceding tests.
3. Perform the irradiation
4. During irradiation measure:
   - Vout
   - Iout
   - Iin

3.5.2.6 Mode 0 Powerup and overcurrent test

1. Set up the test system. Configure the control signals as shown in

Signal	Value
control$< 4:0 >$	10000
reset_OCP_N	1
activate_OCP_N	0
EXT_disable	0
SEL_EXT_disable	0

Table 8: Test Conditions

2. Ramp the power supply
3. Check that the output is in tri-state
4. Once this is complete, set activate_OCP_N high
5. Then briefly pulse reset_OCP_N low
6. The output should now be active
7. Apply a excess current to the output and check that it returns to tri-state.
   - Vout
   - Iout
   - Iin

4 AncBrain

This block will provide multiplexed access to the MOSIAX slow control signals. This is needed because MOSAIX slow control is point-to-point, which would lead to too much mass in the detector for ePIC.

Info on CLPS - LpGBT manual

4.1 Specifications

Slow Control Multiplexer Specification				
Specification	Unit	Value	Comment	Status
Input Signals	N/A	TBD		
Output Signals	N/A	PM Bus • PMWR • PMRD SC Bus • SCWR • SCRD GCLK GRST SYNC RESERVE	• CERN Low Power Signalling Compliant • Manchester Encoding • Exact details need to be confirmed with MOSAIX	
Voltage Ripple	mV			
Power	W			
Supply Voltage	A			
Area	µm^2			

5 65nm EIC-LAS

The 65nm EIC-LAS will be derived from the MOSAIX chip. Therefore all specifications except those quoted will be the same as for MOSAIX.

5.1 Specifications

65nm EIC-LAS Specification					
Specification	Unit	Value (typ)	Value (max)	Comment	Status
Number of RSUs	N/A	5-6			Dev
Output Data Channels	N/A	1-2		1 if no redundancy, 2 if redundancy desired	Dev
Data Output Speed	Gbit/s	10			Dev
Power	W	1.3	2	See notes for break-down	Dev
Supply Voltage	V	1.32	1.32		Dev
Area	μm^2				Dev

Notes

1. Power consumption from [1] which is itself based on the MOSAIX Engineering Specification Review [2]

5.2 Slow Control

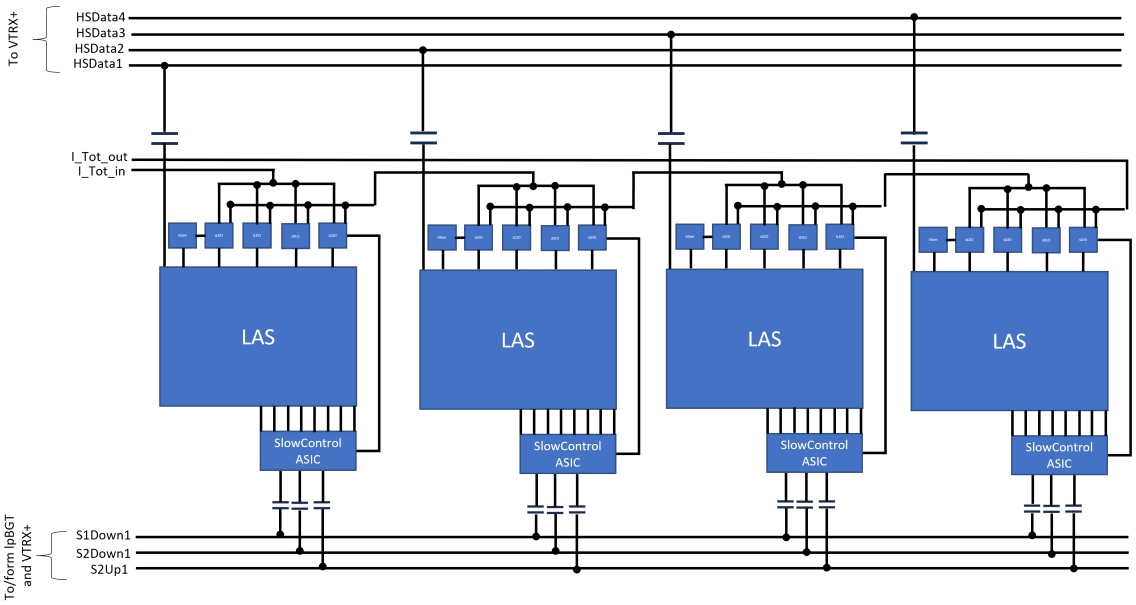
The slow control functionality of MOSAIX is evolving. The most recent documentation can be found in [3].

6 APPENDICES

6.1 APPENDIX A: Stave Overview

This section contains details of how the stave will be arranged, since this is important for the design of the ancillary ASIC.

Figure 9: Diagram of a single stave



6.2 APPENDIX B: MOSAIX Documentation

ITS3 have an online repository for their (every updating) documentation for MOSAIX:
https://mosaixdoc.docs.cern.ch/

Access to this requires a CERN account and to be registered on a suitable mailing list (e-group). The link above contains a direct link to the recommended mosaix-doc-users e-group. Once an account has been granted access, the direct link to the documentation is:
https://mosaixdoc.docs.cern.ch/master

Some helpful links to areas of interest:

- LEC data router.
- Slow control interfaces.
- Slow control protocol.
- Slow control building blocks.
- Powering scheme.
- Datasheet (contains bond pad layout).

6.3 APPENDIX C: Ancillary Chip Sign-off Requirements

6.4 PVT Corners

6.4.1 Analog

- Corner: SS, SF, FS, SS
- Temperature: -20 °C, 105 °C
- Supply: 1.2 V (+/- 10 % voltage variation)

6.4.2 Digital

- Corner: slow, typ, fast
- Temperature: -40 °C, 105 °C
- Supply: 1.2 V (+/- 10 % voltage variation)
- skew MIN, MAX (will be defined based on the final clock rate)

6.4.3 Power Integrity Analysis

- Static IR Drop
- Dynamic IR Drop
- Electromigration

6.4.4 Verification

6.5 APPENDIX D: Outstanding Questions

Since MOSAIX itself and the system in general are still in development, some of the information needed for completing the AncASIC and LAS is not yet available. Here we summarise some of the outstanding questions.

6.5.1 Negative Voltage Generator

1. Level of radiation hardness required?

6.5.2 SLDO

1. Level of redundancy required? Single failure would currently fail an EIC-LAS (only 1 per chip). Cannot be paralleled – tri-state option needed?
2. Level of radiation hardness required?

6.5.3 AncBrain

1. Level of radiation hardness required?
2. Interface to ITS3?
3. What is the common mode and power supply level of the CLPS on MOSAIX for slow control?
4. What is the delay between a write and a response operation?
5. Shall the slow-control link be continuous (sending idle symbols when no transmission) or pauseable (switching off when no transmission)? If the slow control link is pauseable and the interface is AC-coupled, some preamble of mixed 1s and 0s needs to be sent on the data lines prior to the start symbol - the start symbol must the first symbol marked with clock - to re-establish the DC-balance or the transmitter – receiver pairs must be designed to latch last bits and the transmitter must be suited to be put in off state with both lines of a pair equal in voltage; all this requires a bit deeper thinking with the analysis of what eLinks are adaptable to; further considerations related to the link
   - some advantage of pauseable could be less digital activity around the sensitive parts and saving some power,
   - pauseable seems to be more natural as sending slow control will be rare events,
   - with stopped slow control, AncASIC may be the source of readout of MAPS LAS synchronization, making the system autonomous (**important**),
6. Shall the SCL clock be considered system clock? (if yes, there will be less lines in the system, but AncASIC must take this into account by allowing reestablishing internal divisions; typically, it is good to not to mix roles assigned to the clocks);
7. To confirm requirements for the jitter of the system clock should it be routed through the AncASIC to MAPS LAS, as it is decisive for the PLL in LAS and 10Gbps transmission from LAS;
8. To study transmission lines whether they will be able to handle 10Gbps data and multi-point access slow control;
9. The AncASIC automatically becomes and intermediate-chip between lpGBT and LAS, and cannot be just transparent (like in IB where slow control is connected 1:1), it must recognize its address gather data inside and service the link to LAS broadcast (broadcasting can be equal to “fast commands”);
10. How far autonomy of AncASIC can go? It can store LAS configuration data and handle communication to LAS on its own (anyway it has to do that because it must translate 3 wire interface to multi-wire interface);
11. Verification of slow control data integrity: reading all back from AncASIC / LAS or computing check-sums and reading back checksum or computing check-sums, reading back configuration from LAS with computing check-sums comparing both and sending status;

12. Addresses of AncASIC and their configuration on a given FPC can be done with eFuses to save precious pads;
13. How lpGBT will know that these bits sent on the 2.56Gbps link must go to these eLinks and those bit to those eLinks (option1 is eFuses programmed on lpGBT, other options? - we will not be using on-lpGBT I2C M/S ports);
14. Is there any other way of reading back slow control / statuses than maintaining one 10Gbps link only for this – being basically not used?

6.5.4 EIC-LAS

1. How many RSUs
2. What degree of multiplexing? Onto one channel? Or also a redundant channel?
3. JS: Is it perhaps possible to consider lower speed data links (to allow greater distance for E/O interface)? e.g. 1Gbps?
4. LG: Can we find a designer who do for the EIC-LAS readout simulations such as those presented by Gianluca in the back slides here? This person could start by looking at what information is needed for these studies and the ePIC SVT DSC could provide them. This would allow us to understand the speed for data transmission on and off chip. And answer JS' question above.

References

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[2] Pedro Vicente Leitao. *MOSAIX Engineering Specification Review - Powering*. URL: https://indico.cern.ch/event/1408655/#4-powering. (accessed: 26.07.2024).

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