```verilog
module  submodule_0(a0_sub0, a1_sub0, a2_sub0, a3_sub0, a4_sub0, y0_sub0, y1_sub0, y2_sub0, y3_sub0, y4_sub0);
    input a0_sub0,a1_sub0,a2_sub0,a3_sub0,a4_sub0;

    output y0_sub0,y1_sub0,y2_sub0,y3_sub0,y4_sub0;

    assign y0_sub0 = (1'b0);
    assign y1_sub0 = (a1_sub0&a4_sub0);
    and(y2_sub0,a2_sub0,a0_sub0);
    assign y3_sub0 = ((a1_sub0^a0_sub0)?(a3_sub0^a3_sub0):(a1_sub0&a1_sub0));
    nor(y4_sub0,a1_sub0,a0_sub0);
endmodule

...

module  mainmodule_0(a0, a1, a2, a3, a4, a5, a6, a7, a8, a9, a10, a11, a12, a13, a14, a15, a16, a17, a18, a19, y0, y1, y2,
y3, y4, y5, y6, y7, y8, y9, y10, y11, y12, y13, y14, y15, y16, y17, y18, y19);
    input a0,a1,a2,a3,a4,a5,a6,a7,a8,a9,a10,a11,a12,a13,a14,a15,a16,a17,a18,a19;
    output y0,y1,y2,y3,y4,y5,y6,y7,y8,y9,y10,y11,y12,y13,y14,y15,y16,y17,y18,y19;

submodule_0
s0(.a0_sub0(a0),.a1_sub0(a1),.a2_sub0(a2),.a3_sub0(a3),.a4_sub0(a4),.y0_sub0(y0),.y1_sub0(y1),.y2_sub0(y2),.y3_sub0(y3),.y4_
submodule_1 s1(a5,a6,a7,a8,a9,y5,y6,y7,y8,y9);
submodule_2
s2(.a0_sub2(a10),.a1_sub2(a11),.a2_sub2(a12),.a3_sub2(a13),.a4_sub2(a14),.y0_sub2(y10),.y1_sub2(y11),.y2_sub2(y12),.y3_sub2(
submodule_3
s3(.a0_sub3(a15),.a1_sub3(a16),.a2_sub3(a17),.a3_sub3(a18),.a4_sub3(a19),.y0_sub3(y15),.y1_sub3(y16),.y2_sub3(y17),.y3_sub3(
endmodule
```