Fuzz testing, fuzzing is a kind of software test technique. Providing invalid, unexpected or random data as input to a C compiler for example, GCC and LLVM. As Xuejun Yang, Yang Chen mentioned in their report, they designed a fuzzer called Csmith. The design of this fuzzer considered most of the C language and reported more than 325 bugs. However, some important aspect such as strings and dynamic memory allocation are not covered in the C smith. The algorithm of randomly generating program is the core part of this fuzzer and could be referred to the generating of the random netlist.

The BLIF is an abbreviation of the Berkeley Logic Interchange Format which traditionally used by SIS, VIS , and MVISS to represent logic networks (logic-level hierarchical circuit in textual form). In 1992 July 28's report presented by University of California Berkeley described the specific definition of BLIF, the circuit was regarded as a directed graph of combinational logic nodes and sequential logic elements. Models, Logical gates and Latches were clearly described in this document. The BLIF is the input of the netlist synthesis software.

ABC is similar to SIS/MVSIS, (Multi-Valued Logic Synthesis) which processes the design by applying a sequence of transformation to the current network created by the design specification form file (BLIF). The vision of the ABC used in this project is Windows version abc10216. The latest version of the abc was provided on Github. The Programmer’s Manual wrote in December 25, 2006 introduces the ABC internal data representation and illustrate the difference between the SIS/MVSIS. Netlist is an original network representation. In another word, the netlist is an one-to-one correspondence with the deigan specification form file (BLIF). It should be noticed that the ABC only support the BDDs(Binary decision diagram) format of the netlist. Besides, each net has uniqueness and the output of it is single. The standard of ABC will always automatically transform the netlist into logic network.

Yosys is a current existing recursive Verilog test software to verify the front circuit correctness of the Verilog synthesis circuit (Quartus).

The AIG file was used as the initial input file of ABC.