

# **EE-309 - Microprocessors**

## **Course Project**

# **IITB-RISC Multicycle Implementation**

**Prakhar Bansal : 200070056**  
**Pulkit Adil : 200070062**  
**Sahil Garg : 200070070**  
**Samarth Agarwal : 200070072**

# STATES

	$111 \rightarrow RF\_a_1$
S0	$RF\_d_1 \rightarrow mem\_A, alu\_a = T_1$ $mem\_D_{out} \rightarrow IR$
S1	$+1 \rightarrow alu\_b$ $T_1 \rightarrow alu\_a$ $alu\_c \rightarrow PC$
S2	$IR_{11-9} \rightarrow RF\_a_1$ $IR_{8-6} \rightarrow RF\_a_2$ $RF\_d_1 \rightarrow T_1$ $RF\_d_2 \rightarrow T_2$
S3	$T_1 \rightarrow alu\_a$ $T_2 \rightarrow alu\_b$ $alu\_c \rightarrow T_3$
S4	$IR_{5-3} \rightarrow RF\_a_3$ <del><math>T_3 \rightarrow RF\_d_3</math></del>
S5	$111 \rightarrow RF\_a_3$ $PC \rightarrow RF\_d_3$
S6	$T_2 \rightarrow 101S \rightarrow alu\_b$ $T_1 \rightarrow alu\_a$ $alu\_c \rightarrow T_3$
S7	$IR_{11-9} \rightarrow RF\_a_1$ $RF\_d_1 \rightarrow T_1$ $IR_{50} \rightarrow SE06 \rightarrow T_2$

	$IR_{8-0} \rightarrow SE_{\del{5}5} \rightarrow 75$
S8	$75 \rightarrow RF\_d3$ $IR_{11-9} \rightarrow RF\_a3$
S9	$IR_{8-6} \rightarrow RF\_a1$ $RF\_d1 \rightarrow T1$ $IR_{5-0} \rightarrow SE_{\del{1}6} \rightarrow T2$
S10	$T3 \rightarrow mem\_A$ $mem\_D_{out} \rightarrow T3$
S11	$IR_{11-9} \rightarrow RF\_a3$ $T3 \rightarrow RF\_d3$
S12	$IR_{11-9} \rightarrow RF\_a1$ $RF\_d1 \rightarrow T1$
S13	$T3 \rightarrow mem\_A$ $T1 \rightarrow mem\_D_{in}$
S14	$T1 \rightarrow alu\_a$ $T2 \rightarrow alu\_b$ <del><math>alu\_z \rightarrow alu\_z</math></del>
S15	$PC \rightarrow alu\_a$ $IR_{5-0} \rightarrow SE_6 \rightarrow alu\_b$ $alu\_out \rightarrow T3$

	$PC \rightarrow RF\_d3$ $IR_{11-9} \rightarrow RF\_a3$ $111 \rightarrow RF\_a1$ $RF\_d1 \rightarrow T1$ $IR_{8-0} \rightarrow SE9 \rightarrow T2$
S17	$111 \rightarrow RF\_a3$ $T3 \rightarrow RF\_d3$
S18	$PC \rightarrow RF\_d3$ $IR_{11-9} \rightarrow RF\_a3$ $IR_{8-6} \rightarrow RF\_a1$ $RF\_d1 \rightarrow PC$
S19	$IR_{11-9} \rightarrow RF\_a1$ $RF\_d1 \rightarrow T1$ $IR_{8-0} \rightarrow SE9 \rightarrow T2$
S20	$111 \rightarrow RF\_a1$ $RF\_d1 \rightarrow mem\_A, alu\_a$ <del><math>mem\_D_{out} \rightarrow IR</math></del> $+1 \rightarrow alu\_b$ $alu\_c \rightarrow PC$
S20	$IR_{11-9} \rightarrow RF\_a1$ $RF\_d1 \rightarrow mem\_a1, T1$ $mem\_d_{out} \rightarrow T2$ $111 \rightarrow RF\_a3$ $PC \rightarrow RF\_d3$ $IR_{7-0} \rightarrow TC$

W<sub>w</sub>  
WHILE (TC != 00000000) DO {

S21

TC → CC\_in  
CC\_addr → TC  
T1 → alu-a  
+1 → alu-b  
alu-c → T<sub>1</sub>  
CC\_out → RF\_a3  
T2 → RF\_d3

S22

T1 → mem\_A  
mem\_D<sub>out</sub> → T2  
}

S23

IR<sub>11-9</sub> → RF\_a1  
RF\_d1 → T1  
111 → RF\_a3  
PC → RF\_d3  
IR<sub>7-0</sub> → TC

S24

WHILE (TC != 00000000)

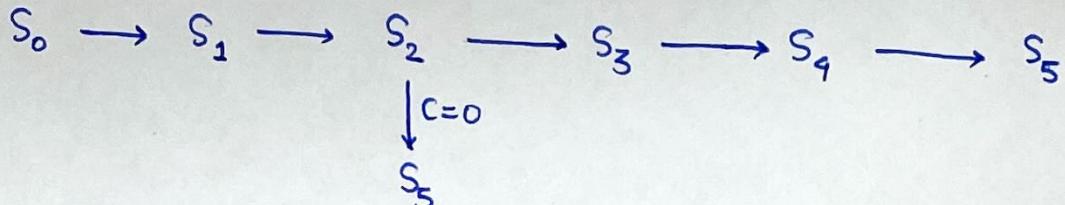
TC → CC\_in  
CC\_addr → TC  
CC\_out → RF\_a1  
T1 → mem\_A, alu-a  
RF\_d1 → mem\_D<sub>in</sub>  
+1 → alu-b  
alu-c → T1

## FLOWCHARTS

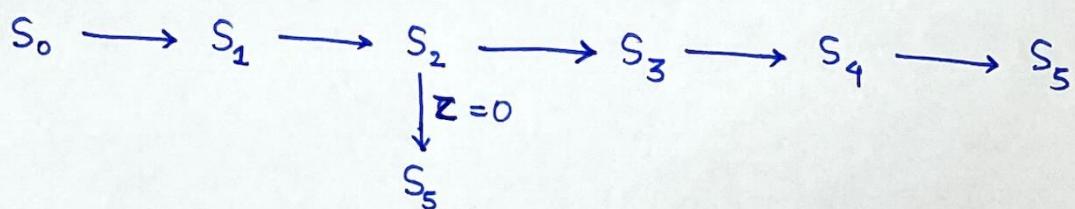
(1) ADD, NDU



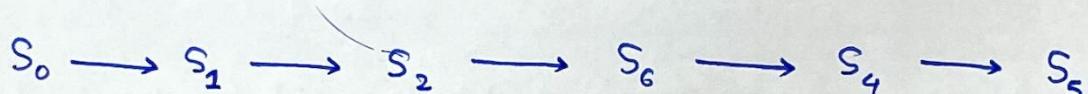
(2) ADC, NDC



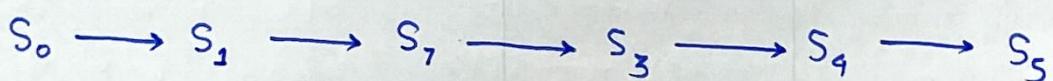
(3) ADZ, NDZ



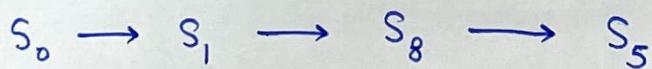
(4) ADL



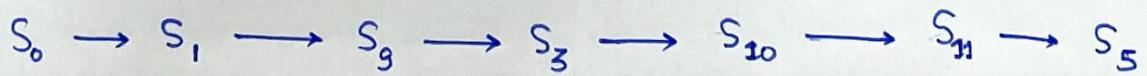
(5) ADT



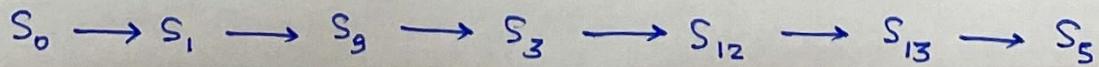
(6) LHI



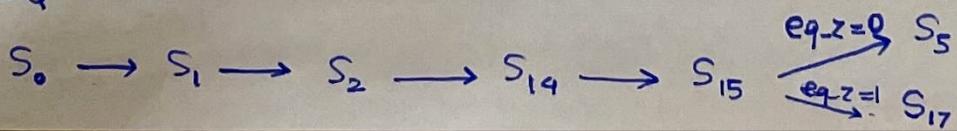
(7) LW



(8) SW



(9) BEQ



(10) JAL

$$S_0 \rightarrow S_1 \rightarrow S_{16} \rightarrow S_3 \rightarrow S_{17}$$

(11) JLR

$$S_0 \rightarrow S_1 \rightarrow S_{18} \rightarrow S_5$$

(12) JRI

$$S_0 \rightarrow S_1 \rightarrow S_{19} \rightarrow S_3 \rightarrow S_{17}$$

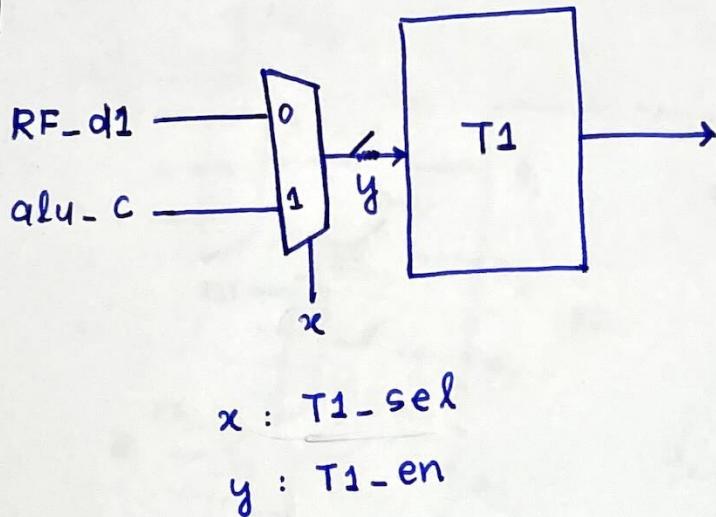
(13) LM

$$S_0 \rightarrow S_1 \rightarrow S_{20} \rightarrow S_{21} \rightarrow S_{22}$$

(14) SM

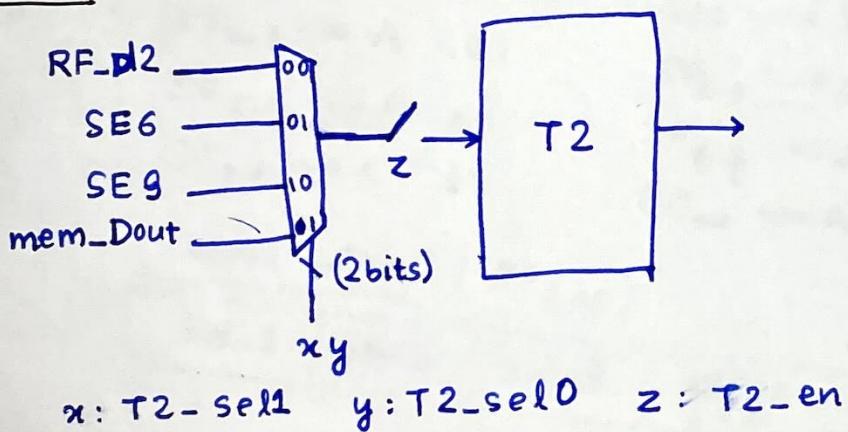
$$S_0 \rightarrow S_1 \rightarrow S_{23} \rightarrow S_{24}$$

T1



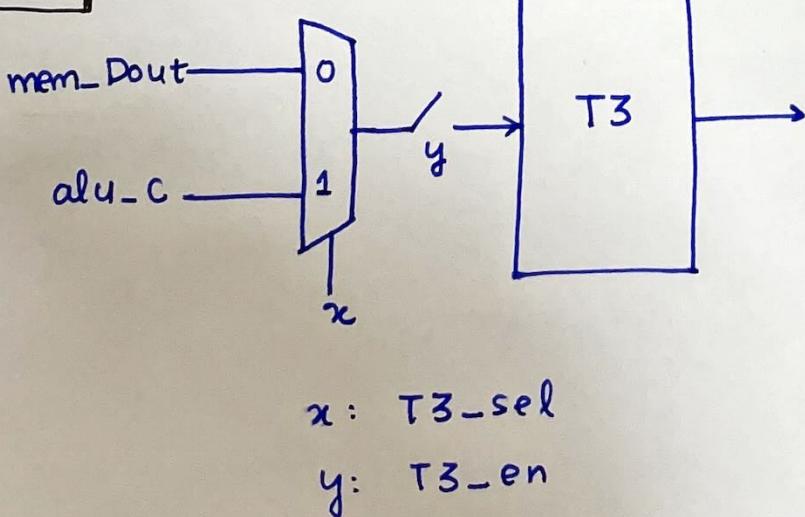
	x	y
none	x	0
$RF\_d1 \rightarrow T1$	0	1
$alu\_c \rightarrow T1$	1	1

T2



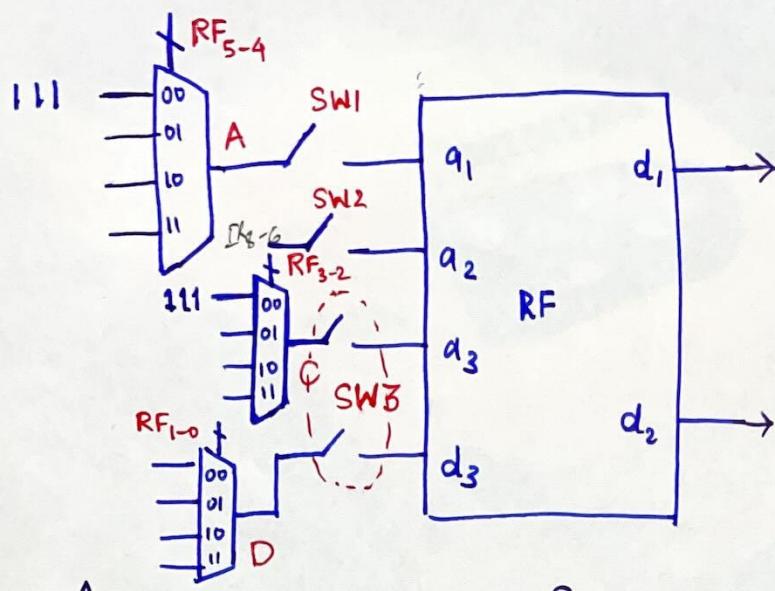
	x	y	z
none	x	x	0
$RF\_d2 \rightarrow T2$	0	0	1
$SE6 \rightarrow T2$	0	1	1
$SE9 \rightarrow T2$	1	0	1
$mem\_Dout \rightarrow T2$	1	1	1

T3



	x	y
none	x	0
$mem\_Dout \rightarrow T3$	0	1
$alu\_c \rightarrow T3$	1	1

## Register File



A

$111 \rightarrow A : 00$   
 $IR_{11-9} \rightarrow A : 01$   
 $IR_{8-6} \rightarrow A : 10$   
 $CC_{out} \rightarrow A : 11$

C

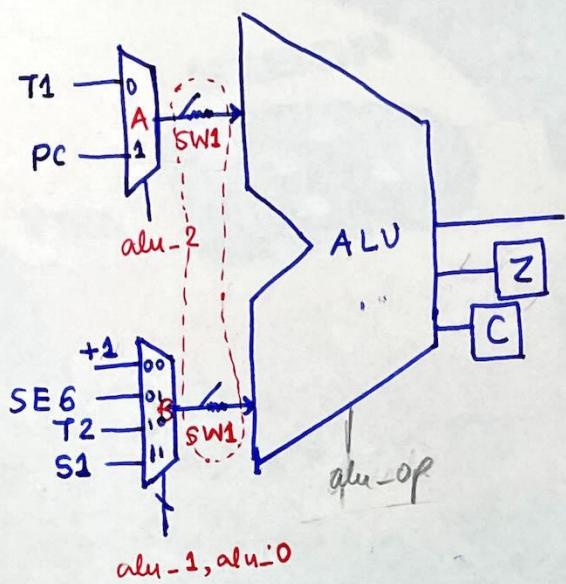
$111 \rightarrow C : 00$       S7  $\rightarrow D : 00$   
 $IR_{11-9} \rightarrow C : 01$       T3  $\rightarrow D : 01$   
 $IR_{8-6} \rightarrow C : 10$       PC  $\rightarrow D : 10$   
 $CC_{out} \rightarrow C : 11$       TR2  $\rightarrow D : 11$

D

Control Word (RF<sub>8-0</sub>)

SW-1	SW-2	SW-3	RR5	RR4	RR3	RR2	RR1	RR0
------	------	------	-----	-----	-----	-----	-----	-----

## ALU



A alu-2

t1 → a : 0

PC → a : 1

B

+1 → b : 00 alu-1 alu-0

SEG → b : 01

F2 → b : 10

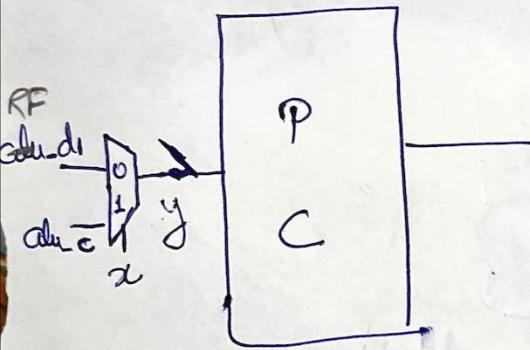
15 → b : 11

SW1 : 0 → open ; 1 → closed

Control word :

SW.1	ALU-2	alu-1	alu-0
------	-------	-------	-------

# PC

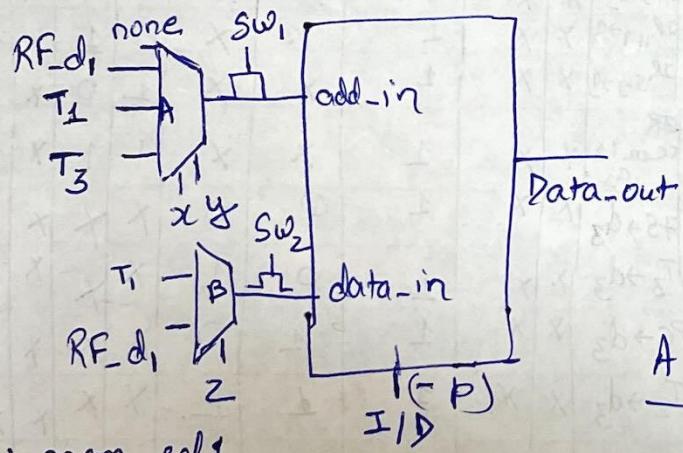


$x$ : PC\_Sel

$y$ : PC\_en

	$x$	$y$
RF none	$x$	0
alu-d <sub>1</sub> → PC	0	1
alu-c → PC	1	1

# Memory



$x$ : mem\_sel1

$y$ : mem\_sel0

$z$ : mem\_sel2

$w$ :

$p = I/D$

	$x$	$y$
none	0	0
RF-di → mem_A	0	1
T <sub>1</sub> → mem_A	1	0
T <sub>3</sub> → mem_A	1	1

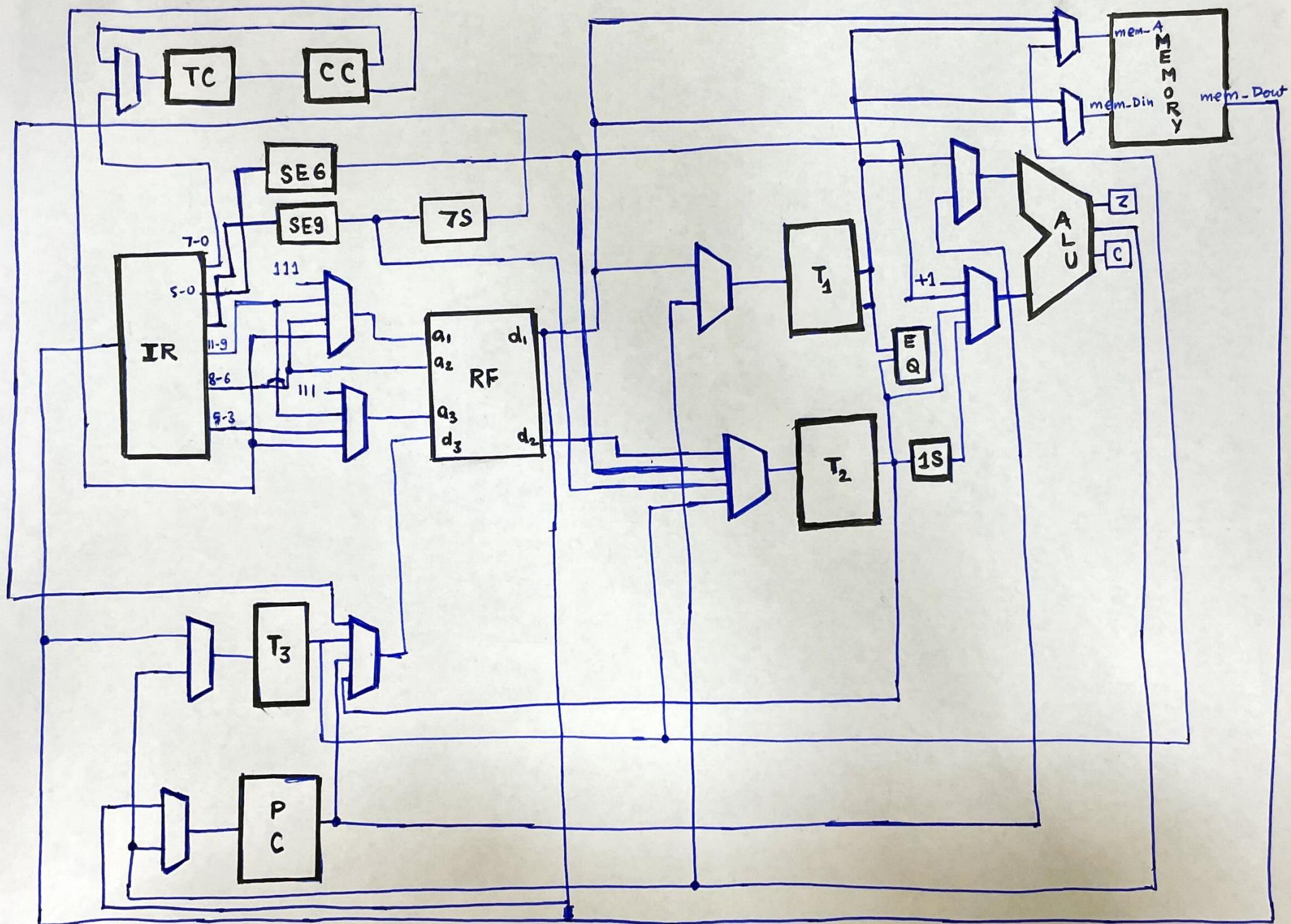
# B

	$z$
T <sub>1</sub> → mem_B	0
RF-di → mem_B	1

$sw_1 = x + y$

$sw_2 = w$

	$w$
0	write data_in <del>enable</del>
1	w.write data_in enable

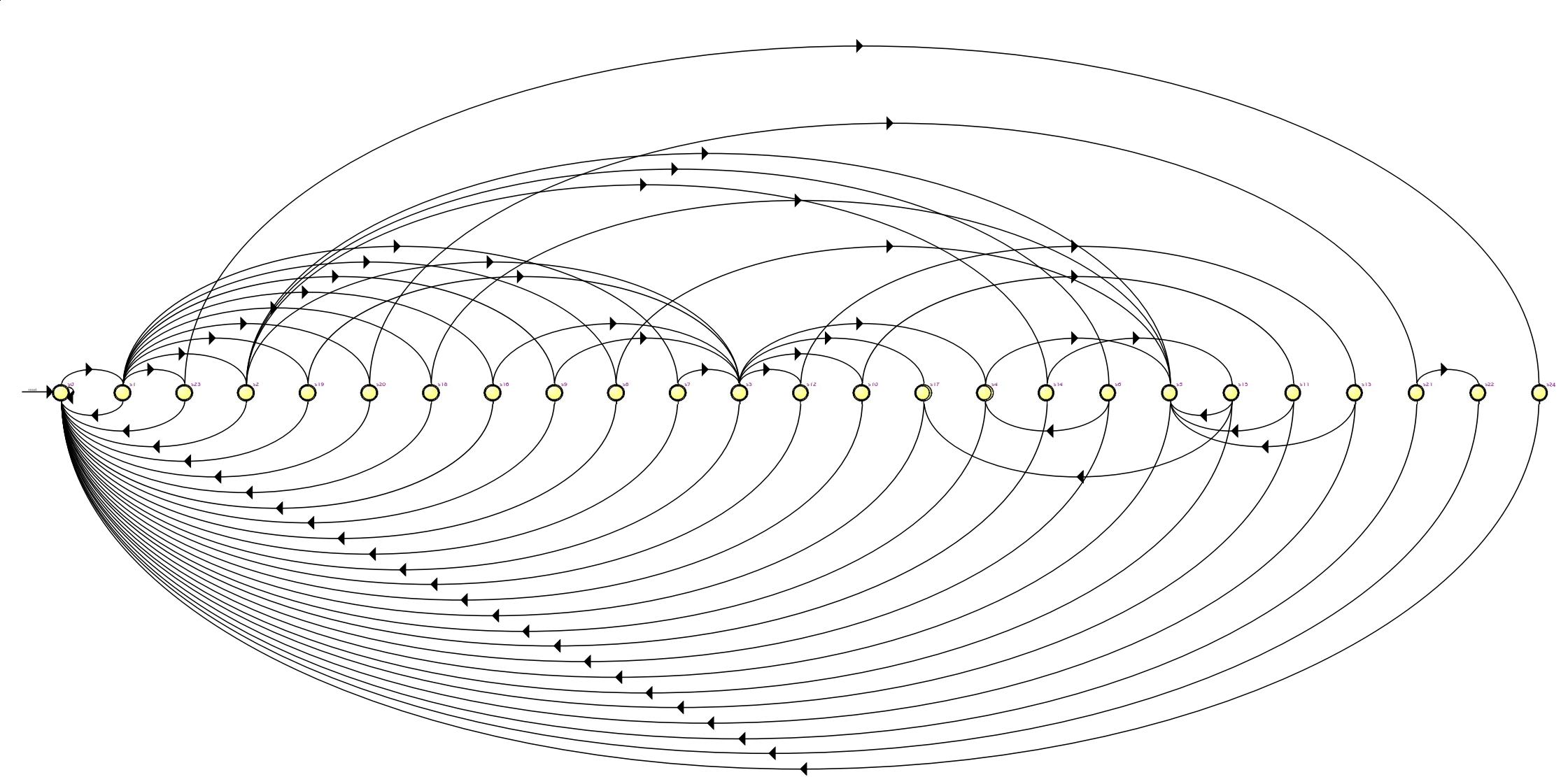


State	T1		T2			T3		TC
	T1_sel	T1_en	T2_sel1	T2_sel0	T2_en	T3_sel	T3_en	
	34	33	32	31	30	29	28	
S0	0	1	x	x	0	x	0	x
S1	x	0	x	x	0	x	0	x
S2	0	1	0	0	1	x	0	x
S3	x	0	x	x	0	1	1	x
S4	x	0	x	x	0	x	0	x
S5	x	0	x	x	0	x	0	x
S6	x	0	x	x	0	1	1	x
S7	0	1	0	1	1	x	0	x
S8	x	0	x	x	0	x	0	x
S9	0	1	0	1	1	x	0	x
S10	x	0	x	x	0	0	1	x
S11	x	0	x	x	0	x	0	x
S12	0	1	x	x	0	x	0	x
S13	x	0	x	x	0	x	0	x
S14	x	0	x	x	0	x	0	x
S15	x	0	x	x	0	1	1	x
S16	0	1	1	0	1	x	0	x
S17	x	0	x	x	0	x	0	x
S18	x	0	x	x	0	x	0	x
S19	0	1	1	0	1	x	0	x
S20	0	1	1	1	1	x	0	x
S21	1	1	x	x	0	x	0	0
S22	x	0	1	1	1	x	0	x
S23	0	1	x	x	0	x	0	1
S24	1	1	x	x	0	x	0	0

C	PC			MEMORY					
	TC_en	PC_sel	PC_en	MEM_sel2	MEM_sel1	MEM_sel0	MEM_wr	RF_8(SW1)	RF_7(SW2)
	26	25	24	23	22	21	20	19	18
0	x	0	x	0	1	0	1	0	
0	1	1	x	0	0	0	0	0	0
0	x	0	x	0	0	0	1	1	
0	x	0	x	0	0	0	0	0	0
0	x	0	x	0	0	0	0	0	0
0	x	0	x	0	0	0	0	0	0
0	x	0	x	0	0	0	0	0	0
0	x	0	x	0	0	0	0	1	0
0	x	0	x	0	0	0	0	0	0
0	x	0	x	0	0	0	0	0	0
0	x	0	x	0	0	0	0	1	0
0	x	0	x	1	1	0	0	0	0
0	x	0	x	0	0	0	0	0	0
0	x	0	x	0	0	0	0	1	0
0	x	0	0	1	1	1	0	0	0
0	x	0	x	0	0	0	0	0	0
0	x	0	x	0	0	0	0	0	0
0	x	0	x	0	0	0	0	0	0
0	0	1	x	0	0	0	0	0	0
0	x	0	x	0	0	0	1	0	
0	x	0	x	0	1	0	1	0	
1	x	0	x	0	0	0	0	0	0
0	x	0	x	1	0	0	0	0	0
1	x	0	x	0	0	0	1	0	
1	x	0	1	1	0	1	1	0	

RF							1S	SE6
RF_6(SW3)	RF_5	RF_4	RF_3	RF_2	RF_1	RF_0		
17	16	15	14	13	12	11	10	9
0	0	0	x	x	x	x	0	0
0	x	x	x	x	x	x	0	0
0	0	1	x	x	x	x	0	0
0	x	x	x	x	x	x	0	0
1	x	x	1	0	0	1	0	0
1	x	x	0	0	1	0	0	0
0	x	x	x	x	x	x	1	0
0	0	1	x	x	x	x	0	1
1	x	x	0	1	0	0	0	0
0	1	0	x	x	x	x	0	1
0	x	x	x	x	x	x	0	0
1	x	x	0	1	0	1	0	0
0	0	1	x	x	x	x	0	0
0	x	x	x	x	x	x	0	0
0	x	x	x	x	x	x	0	0
0	x	x	x	x	x	x	0	1
1	x	x	0	1	1	0	0	0
1	x	x	0	0	0	1	0	0
1	x	x	0	1	1	0	0	0
0	0	1	x	x	x	x	0	0
1	0	1	0	0	1	0	0	0
1	x	x	1	1	1	1	0	0
0	x	x	x	x	x	x	0	0
1	0	1	0	0	1	0	0	0
0	1	1	x	x	x	x	0	0

SE9	CC	7S	IR	ALU				EQ EQ_IN
	CC_in			ALU_3	ALU_2	ALU_1	ALU_0	
	8	7	6	5	4	3	2	1
0	0	0	1	0	x	x	x	0
0	0	0	0	1	0	0	0	0
0	0	0	0	0	x	x	x	0
0	0	0	0	1	0	1	0	0
0	0	0	0	0	x	x	x	0
0	0	0	0	0	x	x	x	0
0	0	0	0	1	0	1	1	0
0	0	0	0	0	x	x	x	0
1	0	1	0	0	x	x	x	0
0	0	0	0	0	x	x	x	0
0	0	0	0	0	x	x	x	0
0	0	0	0	0	x	x	x	0
0	0	0	0	0	x	x	x	0
0	0	0	0	1	0	1	0	1
0	0	0	0	1	1	0	1	0
1	0	0	0	0	x	x	x	0
0	0	0	0	0	x	x	x	0
0	0	0	0	0	x	x	x	0
1	0	0	0	0	x	x	x	0
0	0	0	0	0	x	x	x	0
0	1	0	0	1	0	0	0	0
0	0	0	0	0	x	x	x	0
0	0	0	0	0	x	x	x	0
0	1	0	0	1	0	0	0	0



# State Transition Diagram - FSM

# RTL Views

