

# STATES

	$111 \rightarrow RF\_a_1$
S0	$RF\_d_1 \rightarrow mem\_A, alu\_a = T_1$ $mem\_D_{out} \rightarrow IR$
S1	$+1 \rightarrow alu\_b$ $T_1 \rightarrow alu\_a$ $alu\_c \rightarrow PC$
S2	$IR_{11-9} \rightarrow RF\_a_1$ $IR_{8-6} \rightarrow RF\_a_2$ $RF\_d_1 \rightarrow T_1$ $RF\_d_2 \rightarrow T_2$
S3	$T_1 \rightarrow alu\_a$ $T_2 \rightarrow alu\_b$ $alu\_c \rightarrow T_3$
S4	$IR_{5-3} \rightarrow RF\_a_3$ <del><math>T_3 \rightarrow RF\_d_3</math></del>
S5	$111 \rightarrow RF\_a_3$ $PC \rightarrow RF\_d_3$
S6	$T_2 \rightarrow 101S \rightarrow alu\_b$ $T_1 \rightarrow alu\_a$ $alu\_c \rightarrow T_3$
S7	$IR_{11-9} \rightarrow RF\_a_1$ $RF\_d_1 \rightarrow T_1$ $IR_{50} \rightarrow SE06 \rightarrow T_2$

	$IR_{8-0} \rightarrow SE_{5-9} \rightarrow 75$ $75 \rightarrow RF\_d3$ $IR_{11-9} \rightarrow RF\_a3$
S8	
S9	$IR_{8-6} \rightarrow RF\_a1$ $RF\_d1 \rightarrow T1$ $IR_{5-0} \rightarrow SE_{16} \rightarrow T2$
S10	$T3 \rightarrow mem\_A$ $mem\_D_{out} \rightarrow T3$
S11	$IR_{11-9} \rightarrow RF\_a3$ $T3 \rightarrow RF\_d3$
S12	$IR_{11-9} \rightarrow RF\_a1$ $RF\_d1 \rightarrow T1$
S13	$T3 \rightarrow mem\_A$ $T1 \rightarrow mem\_D_{in}$
S14	$T1 \rightarrow alu\_a$ $T2 \rightarrow alu\_b$ <del><math>alu\_z \rightarrow alu\_z</math></del>
S15	$PC \rightarrow alu\_a$ $IR_{5-0} \rightarrow SE6 \rightarrow alu\_b$ $alu\_out \rightarrow T3$

	$PC \rightarrow RF\_d3$ $IR_{11-9} \rightarrow RF\_q3$ $111 \rightarrow RF\_a1$ $RF\_d1 \rightarrow T1$ $IR_{8-0} \rightarrow SE9 \rightarrow T2$
S17	$111 \rightarrow RF\_a3$ $T3 \rightarrow RF\_d3$
S18	$PC \rightarrow RF\_d3$ $IR_{11-9} \rightarrow RF\_a3$ $IR_{8-6} \rightarrow RF\_a1$ $RF\_d1 \rightarrow PC$
S19	$IR_{11-9} \rightarrow RF\_a1$ $RF\_d1 \rightarrow T1$ $IR_{8-0} \rightarrow SE9 \rightarrow T2$
S20	$111 \rightarrow RF\_a1$ $RF\_d1 \rightarrow mem\_A, alu\_q$ $mem\_D_{out} \rightarrow IR$ $+1 \rightarrow alu\_b$ $alu\_c \rightarrow PC$
S20	$IR_{11-9} \rightarrow RF\_a1$ $RF\_d1 \rightarrow mem\_a1, T1$ $mem\_d1_{out} \rightarrow T2$ $111 \rightarrow RF\_a3$ $PC \rightarrow RF\_d3$ $IR_{7-0} \rightarrow TC$

W<sub>w</sub>  
WHILE (TC != 00000000) DO {

S21

TC → CC\_in  
CC\_addr → TC  
T1 → alu-a  
+1 → alu-b  
alu-c → T<sub>1</sub>  
CC\_out → RF\_a3  
T2 → RF\_d3

S22

T1 → mem\_A  
mem\_D<sub>out</sub> → T2  
}

S23

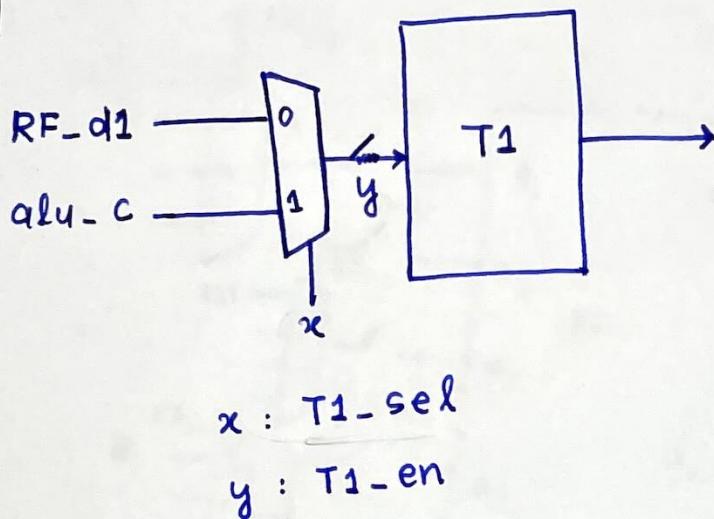
IR<sub>11-9</sub> → RF\_a1  
RF\_d1 → T1  
111 → RF\_a3  
PC → RF\_d3  
IR<sub>7-0</sub> → TC

S24

WHILE (TC != 00000000)

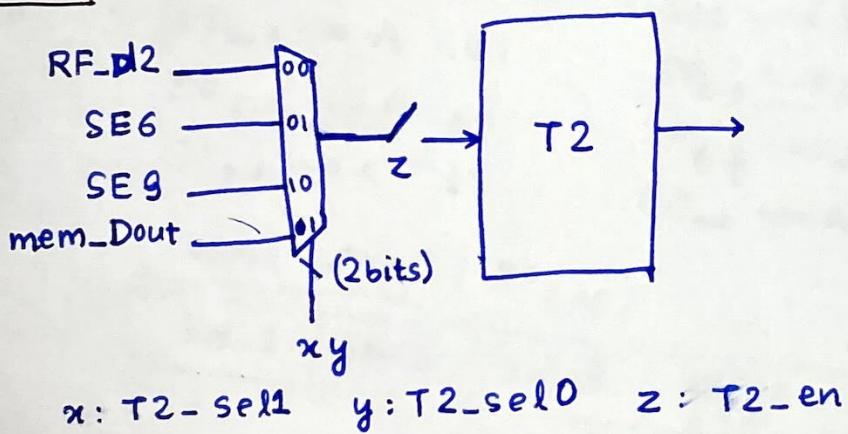
TC → CC\_in  
CC\_addr → TC  
CC\_out → RF\_a1  
T1 → mem\_A, alu-a  
RF\_d1 → mem\_D<sub>in</sub>  
+1 → alu-b  
alu-c → T1

T1



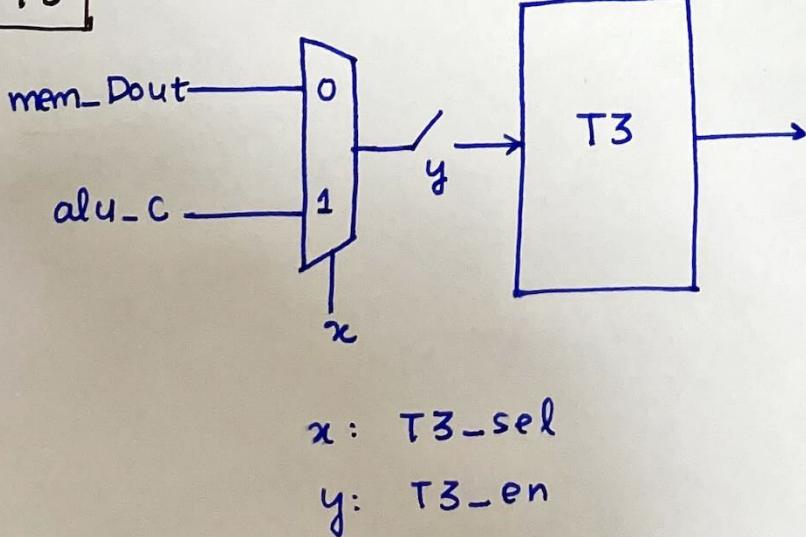
	x	y
none	x	0
$RF\_d1 \rightarrow T1$	0	1
$alu\_c \rightarrow T1$	1	1

T2



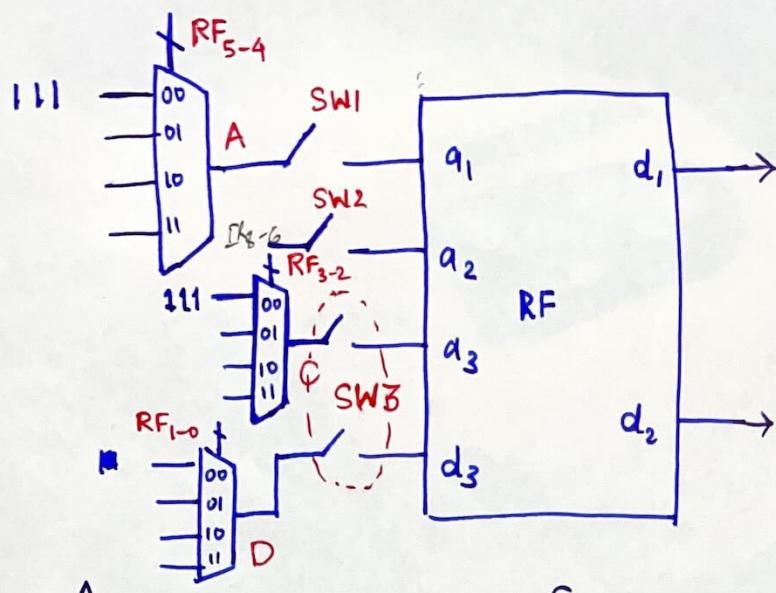
	x	y	z
none	x	x	0
$RF\_d2 \rightarrow T2$	0	0	1
$SE6 \rightarrow T2$	0	1	1
$SE9 \rightarrow T2$	1	0	1
$mem\_Dout \rightarrow T2$	1	1	1

T3



	x	y
none	x	0
$mem\_Dout \rightarrow T3$	0	1
$alu\_c \rightarrow T3$	1	1

## Register File



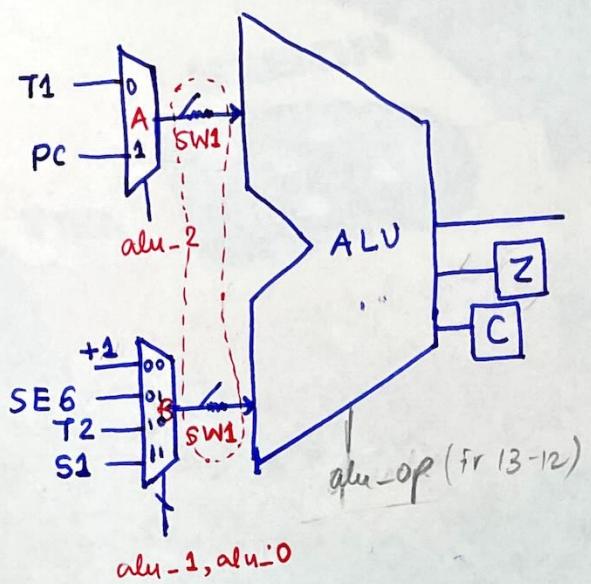
	A	C	D
IR <sub>8-1</sub> - SW2	111 → A : 00	111 → AC : 00	S7 → D : 00
SW2 - 1	IR <sub>11-9</sub> → A : 01	IR <sub>11-9</sub> → AC : 01	T3 → D : 01
	IR <sub>8-6</sub> → A : 10	IR <sub>8-6</sub> → AC : 10	PC → D : 10
	CC <sub>out</sub> → A : 11	CC <sub>out</sub> → AC : 11	TR2 → D : 11

## Control Word (RF<sub>8-0</sub>)

SW-1	SW-2	SW-3	alu-0 RR5	alu-1 RR4	alu-2 RR3	alu-3 RR2	alu-4 RR1	alu-5 RR0
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{ A }      { C }      { D }

## ALU



## A

$t_1 \rightarrow a : 0$   
 $PC \rightarrow a : 1$

## B

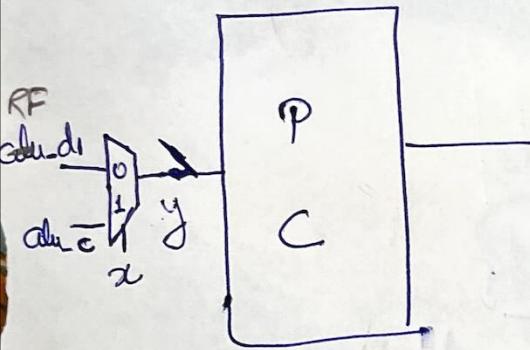
$+1 \rightarrow b : 00$   
 $SEG \rightarrow b : 01$   
 $F2 \rightarrow b : 10$   
 $15 \rightarrow b : 11$

SW1:  $0 \rightarrow \text{open} ; 1 \rightarrow \text{closed}$

Control word:

SW.1	ALU-2	alu-1	alu-0
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# PC



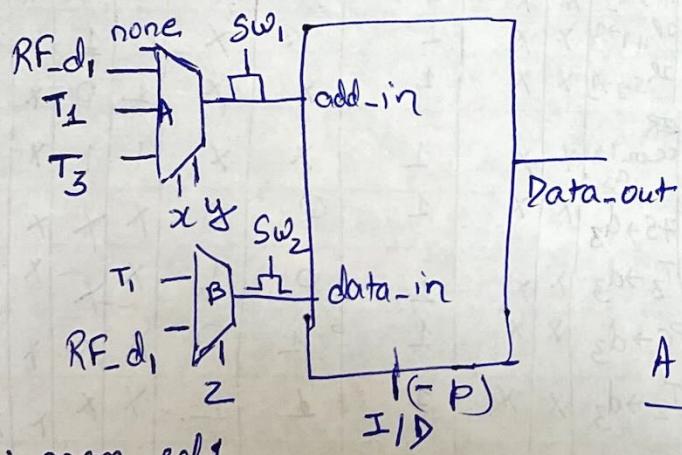
$x$ : PC-Sel

$y$ : PC-en

$x$	$y$
X	0
0	1
1	1

RF none  
 $alu\_di \rightarrow PC$   
 $alu\_c \rightarrow PC$

# Memory



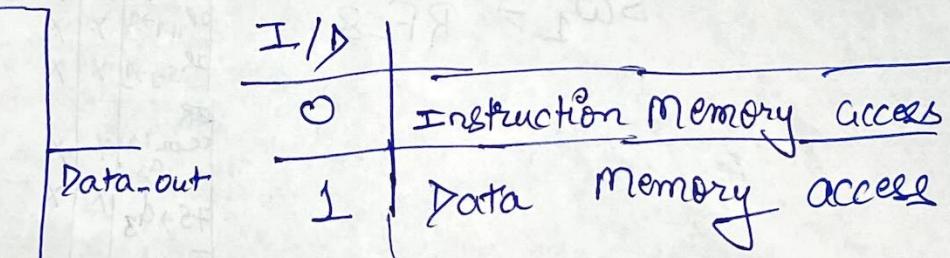
$x$ : mem-sel1

$y$ : mem-sel0

$z$ : mem-sel2

~~w - mem-state~~

$p = I/D$



	$x$	$y$
none	0	0
$RF\_di \rightarrow mem\_A$	0	1
$T_1 \rightarrow mem\_A$	1	0
$T_3 \rightarrow mem\_A$	1	1

# B

	$z$
$T_1 \rightarrow mem\_D$	0
$RF\_di \rightarrow mem\_D$	1

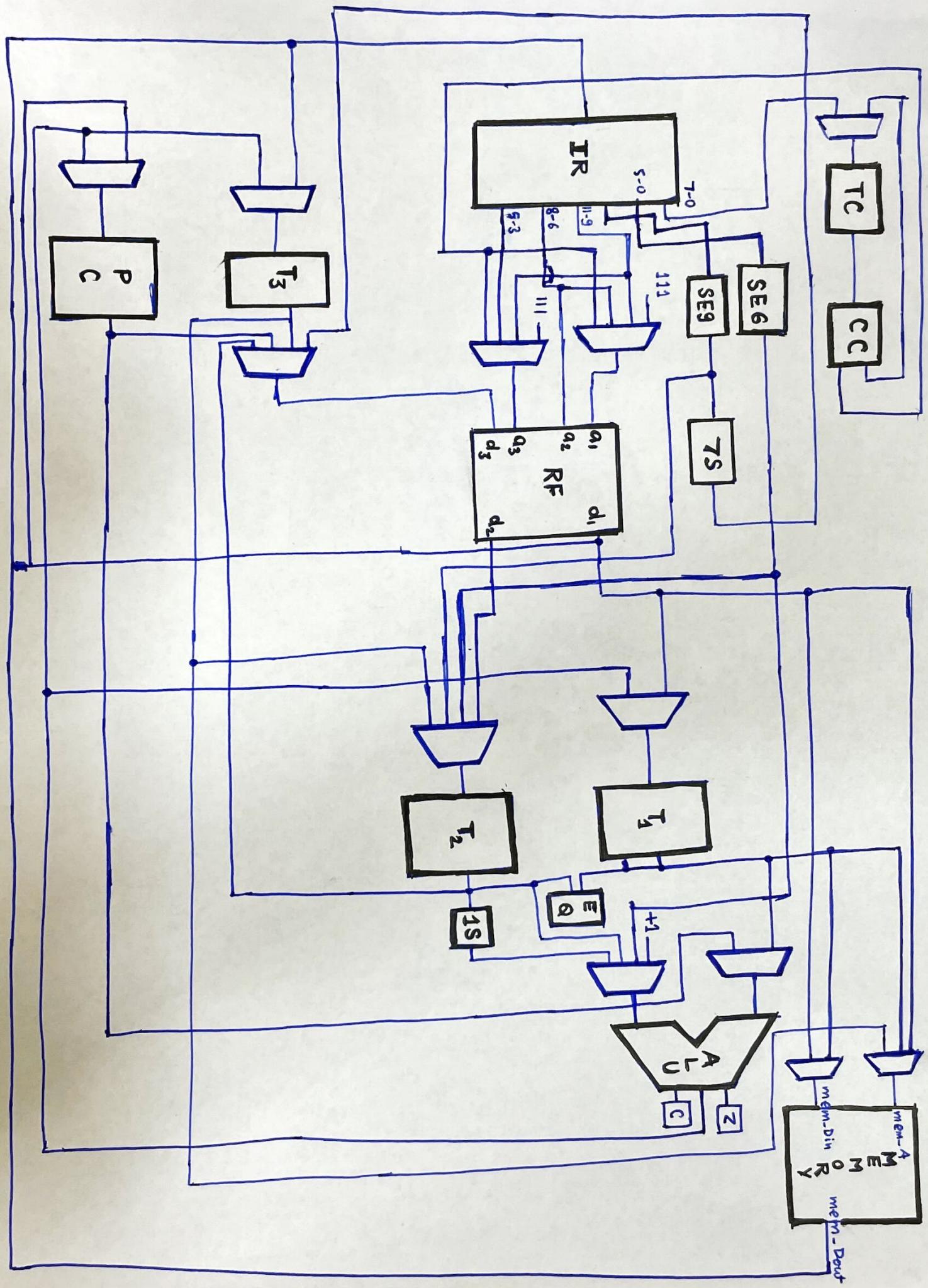
$$SW_1 = x + y \oplus p$$

$$SW_2 = w = I/D$$

$w$
0
1

Write data-in ~~enable~~

Write data-in enable



State	T1		T2			T3		TC
	T1_sel	T1_en	T2_sel1	T2_sel0	T2_en	T3_sel	T3_en	
	34	33	32	31	30	29	28	
S0	0	1	x	x	0	x	0	x
S1	x	0	x	x	0	x	0	x
S2	0	1	0	0	1	x	0	x
S3	x	0	x	x	0	1	1	x
S4	x	0	x	x	0	x	0	x
S5	x	0	x	x	0	x	0	x
S6	x	0	x	x	0	1	1	x
S7	0	1	0	1	1	x	0	x
S8	x	0	x	x	0	x	0	x
S9	0	1	0	1	1	x	0	x
S10	x	0	x	x	0	0	1	x
S11	x	0	x	x	0	x	0	x
S12	0	1	x	x	0	x	0	x
S13	x	0	x	x	0	x	0	x
S14	x	0	x	x	0	x	0	x
S15	x	0	x	x	0	1	1	x
S16	0	1	1	0	1	x	0	x
S17	x	0	x	x	0	x	0	x
S18	x	0	x	x	0	x	0	x
S19	0	1	1	0	1	x	0	x
S20	0	1	1	1	1	x	0	x
S21	1	1	x	x	0	x	0	0
S22	x	0	1	1	1	x	0	x
S23	0	1	x	x	0	x	0	1
S24	1	1	x	x	0	x	0	0

C	PC			MEMORY					
	TC_en	PC_sel	PC_en	MEM_sel2	MEM_sel1	MEM_sel0	MEM_wr	RF_8(SW1)	RF_7(SW2)
	26	25	24	23	22	21	20	19	18
0	x	0	x	0	1	0	1	0	
0	1	1	x	0	0	0	0	0	0
0	x	0	x	0	0	0	1	1	
0	x	0	x	0	0	0	0	0	0
0	x	0	x	0	0	0	0	0	0
0	x	0	x	0	0	0	0	0	0
0	x	0	x	0	0	0	0	0	0
0	x	0	x	0	0	0	0	1	0
0	x	0	x	0	0	0	0	0	0
0	x	0	x	0	0	0	0	0	0
0	x	0	x	0	0	0	0	1	0
0	x	0	x	1	1	0	0	0	0
0	x	0	x	0	0	0	0	0	0
0	x	0	x	0	0	0	0	1	0
0	x	0	0	1	1	1	0	0	0
0	x	0	x	0	0	0	0	0	0
0	x	0	x	0	0	0	0	0	0
0	x	0	x	0	0	0	0	0	0
0	0	1	x	0	0	0	0	0	0
0	x	0	x	0	0	0	1	0	
0	x	0	x	0	1	0	1	0	
1	x	0	x	0	0	0	0	0	0
0	x	0	x	1	0	0	0	0	0
1	x	0	x	0	0	0	1	0	
1	x	0	1	1	0	1	1	0	

RF							1S	SE6
RF_6(SW3)	RF_5	RF_4	RF_3	RF_2	RF_1	RF_0		
17	16	15	14	13	12	11	10	9
0	0	0	x	x	x	x	0	0
0	x	x	x	x	x	x	0	0
0	0	1	x	x	x	x	0	0
0	x	x	x	x	x	x	0	0
1	x	x	1	0	0	1	0	0
1	x	x	0	0	1	0	0	0
0	x	x	x	x	x	x	1	0
0	0	1	x	x	x	x	0	1
1	x	x	0	1	0	0	0	0
0	1	0	x	x	x	x	0	1
0	x	x	x	x	x	x	0	0
1	x	x	0	1	0	1	0	0
0	0	1	x	x	x	x	0	0
0	x	x	x	x	x	x	0	0
0	x	x	x	x	x	x	0	0
0	x	x	x	x	x	x	0	1
1	x	x	0	1	1	0	0	0
1	x	x	0	0	0	1	0	0
1	x	x	0	1	1	0	0	0
0	0	1	x	x	x	x	0	0
1	0	1	0	0	1	0	0	0
1	x	x	1	1	1	1	0	0
0	x	x	x	x	x	x	0	0
1	0	1	0	0	1	0	0	0
0	1	1	x	x	x	x	0	0

SE9	CC	7S	IR	ALU				EQ EQ_IN
	CC_in			ALU_3	ALU_2	ALU_1	ALU_0	
	8	7	6	5	4	3	2	1
0	0	0	1	0	x	x	x	0
0	0	0	0	1	0	0	0	0
0	0	0	0	0	x	x	x	0
0	0	0	0	1	0	1	0	0
0	0	0	0	0	x	x	x	0
0	0	0	0	0	x	x	x	0
0	0	0	0	1	0	1	1	0
0	0	0	0	0	x	x	x	0
1	0	1	0	0	x	x	x	0
0	0	0	0	0	x	x	x	0
0	0	0	0	0	x	x	x	0
0	0	0	0	0	x	x	x	0
0	0	0	0	0	x	x	x	0
0	0	0	0	1	0	1	0	1
0	0	0	0	1	1	0	1	0
1	0	0	0	0	x	x	x	0
0	0	0	0	0	x	x	x	0
0	0	0	0	0	x	x	x	0
1	0	0	0	0	x	x	x	0
0	0	0	0	0	x	x	x	0
0	1	0	0	1	0	0	0	0
0	0	0	0	0	x	x	x	0
0	0	0	0	0	x	x	x	0
0	1	0	0	1	0	0	0	0

01xx0x0x0x0x010010000xxxx0000010xxx0			
x0xx0x0x011x00x0000xxxxxx00000010000			
01001x0x0x00x011001xxxx0000000xxx0			
x0xx011x0x0x00x0000xxxxxx00000010100			
x0xx0x0x0x00x0001xx10010000000xxx0			
x0xx0x0x0x00x0001xx00100000000xxx0			
x0xx011x0x0x00x0000xxxxxx10000010110			
01011x0x0x00x010001xxxx0100000xxx0			
x0xx0x0x0x00x0001xx01000010100xxx0			
01011x0x0x00x010010xxxx0100000xxx0			
x0xx001x0x0x1110000xxxxxx0000000xxx0			
x0xx0x0x0x00x0001xx01010000000xxx0			
01xx0x0x0x00x010001xxxx0000000xxx0			
x0xx0x0x001111000xxxxxx0000000xxx0			
x0xx0x0x0x00x0000xxxxxx000000010101			
x0xx011x0x0x00x0000xxxxxx01000011010			
01101x0x0x00x0001xx01100010000xxx0			
x0xx0x0x0x00x0001xx00010000000xxx0			
x0xx0x001x00x0001xx01100000000xxx0			
01101x0x0x00x010001xxxx0010000xxx0			
01111x0x0x0110101010010000000xxx0			
11xx0x001x0x00x0001xx111100010010000			
x0111x0x0x1010000xxxxxx0000000xxx0			
01xx0x011x0x00x01010100100000000xxx0			
11xx0x001x01101110011xxxx00010010000			

