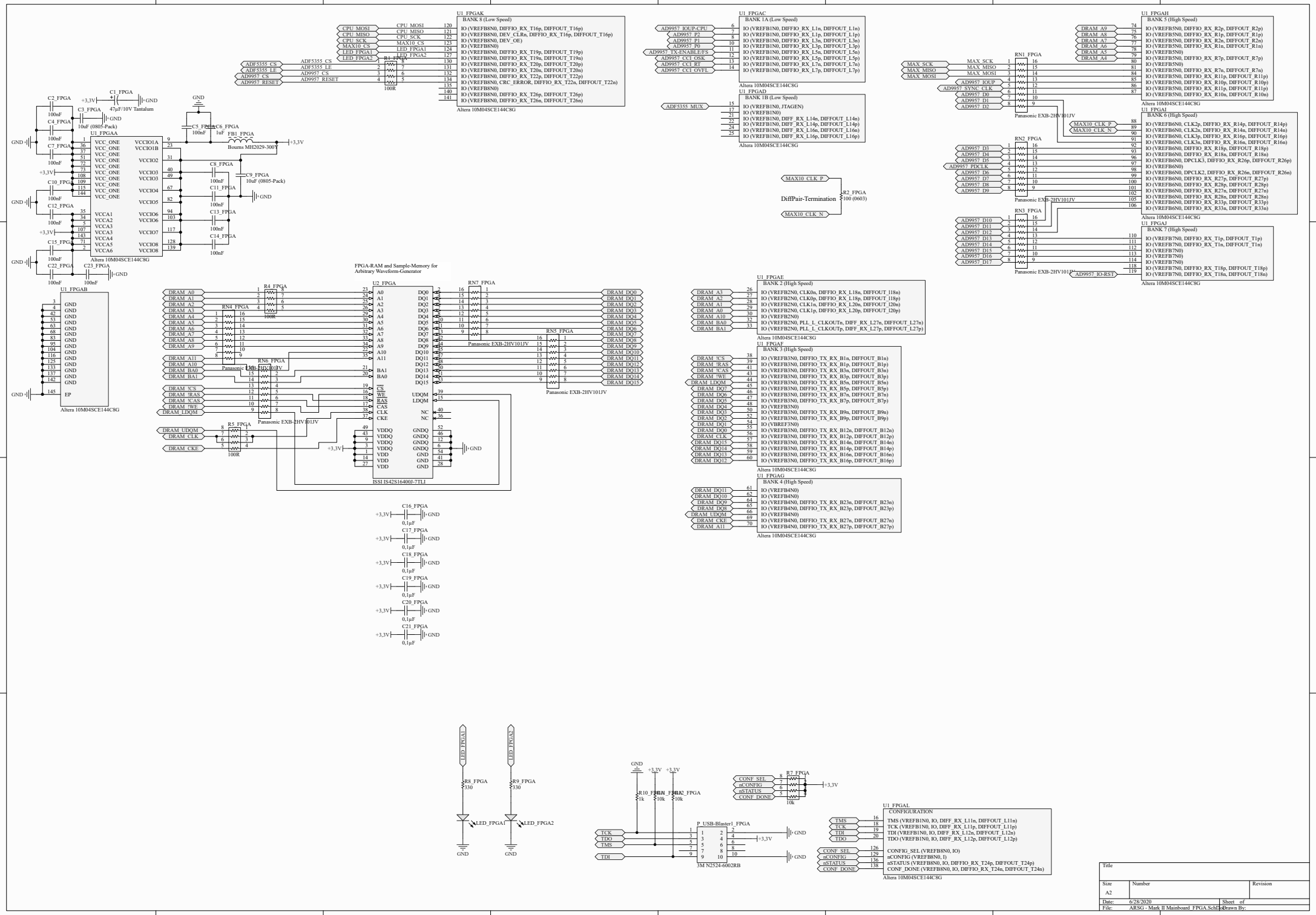
U1_FPGAK
BANK 8 (Low Speed)
IO (VREFB8N0, DIFFIO_RX_T16p, DIFFOUT_T16p)
IO (VREFB8N0, DEV_CLRn, DIFFIO_RX_T16p, DIFFOUT_T16p)
IO (VREFB8N0, DEV_OE)
IO (VREFB8N0)
IO (VREFB8N0, DIFFIO_RX_T19p, DIFFOUT_T19p)
IO (VREFB8N0, DIFFIO_RX_T19n, DIFFOUT_T19n)
IO (VREFB8N0, DIFFIO_RX_T20p, DIFFOUT_T20p)
IO (VREFB8N0, DIFFIO_RX_T20n, DIFFOUT_T20n)
IO (VREFB8N0, DIFFIO_RX_T22p, DIFFOUT_T22p)
IO (VREFB8N0, CRC_ERROR, DIFFIO_RX_T22n, DIFFOUT_T22n)
IO (VREFB8N0)
IO (VREFB8N0, DIFFIO_RX_T26p, DIFFOUT_T26p)
IO (VREFB8N0, DIFFIO_RX_T26n, DIFFOUT_T26n)
Altera 10M04SCE144C8G
U1_FPGAC
BANK 1A (Low Speed)
IO (VREFB1N0, DIFFIO_RX_L1n, DIFFOUT_L1n)
IO (VREFB1N0, DIFFIO_RX_L1p, DIFFOUT_L1p)
IO (VREFB1N0, DIFFIO_RX_L3n, DIFFOUT_L3n)
IO (VREFB1N0, DIFFIO_RX_L3p, DIFFOUT_L3p)
IO (VREFB1N0, DIFFIO_RX_L5n, DIFFOUT_L5n)
IO (VREFB1N0, DIFFIO_RX_L5p, DIFFOUT_L5p)
IO (VREFB1N0, DIFFIO_RX_L7n, DIFFOUT_L7n)
IO (VREFB1N0, DIFFIO_RX_L7p, DIFFOUT_L7p)
Altera 10M04SCE144C8G
U1_FPGAD
BANK 1B (Low Speed)
IO (VREFB1N0, JTAGEN)
IO (VREFB1N0)
IO (VREFB1N0, DIFF_RX_L14n, DIFFOUT_L14n)
IO (VREFB1N0, DIFF_RX_L14p, DIFFOUT_L14p)
IO (VREFB1N0, DIFF_RX_L16n, DIFFOUT_L16n)
IO (VREFB1N0, DIFF_RX_L16p, DIFFOUT_L16p)
Altera 10M04SCE144C8G
U1_FPGAH
BANK 5 (High Speed)
IO (VREFB5N0, DIFFIO_RX_R2p, DIFFOUT_R2p)
IO (VREFB5N0, DIFFIO_RX_R1p, DIFFOUT_R1p)
IO (VREFB5N0, DIFFIO_RX_R2n, DIFFOUT_R2n)
IO (VREFB5N0, DIFFIO_RX_R1n, DIFFOUT_R1n)
IO (VREFB5N0)
IO (VREFB5N0, DIFFIO_RX_R7p, DIFFOUT_R7p)
IO (VREFB5N0)
IO (VREFB5N0, DIFFIO_RX_R7n, DIFFOUT_R7n)
IO (VREFB5N0, DIFFIO_RX_R11p, DIFFOUT_R11p)
IO (VREFB5N0, DIFFIO_RX_R10p, DIFFOUT_R10p)
IO (VREFB5N0, DIFFIO_RX_R11p, DIFFOUT_R11p)
IO (VREFB5N0, DIFFIO_RX_R10n, DIFFOUT_R10n)
Altera 10M04SCE144C8G
U1_FPGAI
BANK 6 (High Speed)
IO (VREFB6N0, CLK2p, DIFFIO_RX_R14p, DIFFOUT_R14p)
IO (VREFB6N0, CLK2n, DIFFIO_RX_R14n, DIFFOUT_R14n)
IO (VREFB6N0, CLK3p, DIFFIO_RX_R16p, DIFFOUT_R16p)
IO (VREFB6N0, CLK3n, DIFFIO_RX_R16n, DIFFOUT_R16n)
IO (VREFB6N0, DIFFIO_RX_R18p, DIFFOUT_R18p)
IO (VREFB6N0, DIFFIO_RX_R18n, DIFFOUT_R18n)
IO (VREFB6N0, DPCLK3, DIFFIO_RX_R26p, DIFFOUT_R26p)
IO (VREFB6N0)
IO (VREFB6N0, DPCLK2, DIFFIO_RX_R26n, DIFFOUT_R26n)
IO (VREFB6N0, DIFFIO_RX_R27p, DIFFOUT_R27p)
IO (VREFB6N0, DIFFIO_RX_R28p, DIFFOUT_R28p)
IO (VREFB6N0, DIFFIO_RX_R27n, DIFFOUT_R27n)
IO (VREFB6N0, DIFFIO_RX_R28n, DIFFOUT_R28n)
IO (VREFB6N0, DIFFIO_RX_R33p, DIFFOUT_R33p)
IO (VREFB6N0, DIFFIO_RX_R33n, DIFFOUT_R33n)
Altera 10M04SCE144C8G
U1_FPGAJ
BANK 7 (High Speed)
IO (VREFB7N0, DIFFIO_RX_T1p, DIFFOUT_T1p)
IO (VREFB7N0, DIFFIO_RX_T1n, DIFFOUT_T1n)
IO (VREFB7N0)
IO (VREFB7N0)
IO (VREFB7N0)
IO (VREFB7N0, DIFFIO_RX_T18p, DIFFOUT_T18p)
IO (VREFB7N0, DIFFIO_RX_T18n, DIFFOUT_T18n)
Altera 10M04SCE144C8G
U1_FPGAE
BANK 2 (High Speed)
IO (VREFB2N0, CLK0n, DIFFIO_RX_L18n, DIFFOUT_I18n)
IO (VREFB2N0, CLK0p, DIFFIO_RX_L18p, DIFFOUT_I18p)
IO (VREFB2N0, CLK1n, DIFFIO_RX_L20n, DIFFOUT_I20n)
IO (VREFB2N0, CLK1p, DIFFIO_RX_L20p, DIFFOUT_I20p)
IO (VREFB2N0)
IO (VREFB2N0, PLL_L_CLKOUTn, DIFF_RX_L27n, DIFFOUT_L27n)
IO (VREFB2N0, PLL_L_CLKOUTp, DIFF_RX_L27p, DIFFOUT_L27p)
Altera 10M04SCE144C8G
U1_FPGAF
BANK 3 (High Speed)
IO (VREFB3N0, DIFFIO_TX_RX_B1n, DIFFOUT_B1n)
IO (VREFB3N0, DIFFIO_TX_RX_B1p, DIFFOUT_B1p)
IO (VREFB3N0, DIFFIO_TX_RX_B3n, DIFFOUT_B3n)
IO (VREFB3N0, DIFFIO_TX_RX_B3p, DIFFOUT_B3p)
IO (VREFB3N0, DIFFIO_TX_RX_B5n, DIFFOUT_B5n)
IO (VREFB3N0, DIFFIO_TX_RX_B5p, DIFFOUT_B5p)
IO (VREFB3N0, DIFFIO_TX_RX_B7n, DIFFOUT_B7n)
IO (VREFB3N0, DIFFIO_TX_RX_B7p, DIFFOUT_B7p)
IO (VREFB3N0)
IO (VREFB3N0, DIFFIO_TX_RX_B9n, DIFFOUT_B9n)
IO (VREFB3N0, DIFFIO_TX_RX_B9p, DIFFOUT_B9p)
IO (VBREF3N0)
IO (VREFB3N0, DIFFIO_TX_RX_B12n, DIFFOUT_B12n)
IO (VREFB3N0, DIFFIO_TX_RX_B12p, DIFFOUT_B12p)
IO (VREFB3N0, DIFFIO_TX_RX_B14n, DIFFOUT_B14n)
IO (VREFB3N0, DIFFIO_TX_RX_B14p, DIFFOUT_B14p)
IO (VREFB3N0, DIFFIO_TX_RX_B16n, DIFFOUT_B16n)
IO (VREFB3N0, DIFFIO_TX_RX_B16p, DIFFOUT_B16p)
Altera 10M04SCE144C8G
U1_FPGAG
BANK 4 (High Speed)
IO (VREFB4N0)
IO (VREFB4N0)
IO (VREFB4N0, DIFFIO_TX_RX_B23n, DIFFOUT_B23n)
IO (VREFB4N0, DIFFIO_TX_RX_B23p, DIFFOUT_B23p)
IO (VREFB4N0)
IO (VREFB4N0, DIFFIO_TX_RX_B27n, DIFFOUT_B27n)
IO (VREFB4N0, DIFFIO_TX_RX_B27p, DIFFOUT_B27p)
Altera 10M04SCE144C8G
U1_FPGAA
U1_FPGAB
Altera 10M04SCE144C8G
U2_FPGA
ISSI IS42S16400J-7TLI
FPGA-RAM and Sample-Memory for Arbitrary Waveform-Generator
Panasonic EXB-2HV101JV
R1_FPGA 100R
R2_FPGA 100 (0603)
DiffPair-Termination
C1_FPGA 47µF/10V Tantalum
C3_FPGA 10uF (0805-Pack)
C9_FPGA 10uF (0805-Pack)
FB1_FPGA Bourns MH2029-300Y
C16_FPGA 0,1µF
C17_FPGA 0,1µF
C18_FPGA 0,1µF
C19_FPGA 0,1µF
C20_FPGA 0,1µF
C21_FPGA 0,1µF
R8_FPGA 330
R9_FPGA 330
LED_FPGA1
LED_FPGA2
R10_FPGA 1k
R11_FPGA 10k
R12_FPGA 10k
R7_FPGA 10k
P_USB-Blaster1_FPGA
3M N2524-6002RB
U1_FPGAL
CONFIGURATION
TMS (VREFB1N0, IO, DIFF_RX_L11n, DIFFOUT_L11n)
TCK (VREFB1N0, IO, DIFF_RX_L11p, DIFFOUT_L11p)
TDI (VREFB1N0, IO, DIFF_RX_L12n, DIFFOUT_L12n)
TDO (VREFB1N0, IO, DIFF_RX_L12p, DIFFOUT_L12p)
CONFIG_SEL (VREFB8N0, IO)
nCONFIG (VREFB8N0, I)
nSTATUS (VREFB8N0, IO, DIFFIO_RX_T24p, DIFFOUT_T24p)
CONF_DONE (VREFB8N0, IO, DIFFIO_RX_T24n, DIFFOUT_T24n)
Altera 10M04SCE144C8G
Title
Size A2
Number
Revision
Date: 6/28/2020
Sheet of
File: ARSG - Mark II Mainboard_FPGA.SchDoc
Drawn By: