Isaac Sanchez

Design & Verification Engineer

CONTACT

Phone: +49-1522-596-7267
Email: sanchezf.si@outlook.com
Location: Dresden

LinkedIn
GitHub
Website

PROFILE

Master's graduate in Nanoelectronic Systems with hands-on experience in RTL design and digital verification. Skilled in SystemVerilog, UVM, assertions, and functional coverage, with a solid background in scripting and EDA tools. Experienced in creating and improving verification environments, collaborating across design and verification teams to ensure robust, high-quality designs.

PROFESSIONAL EXPERIENCE

Digital Design and Verification Engineer (WS) | Oct 2023 – Mar 2025

Racyics GmbH

- Enhanced JTAG IP for production deployment, ensuring IEEE standard compliance and improving verification with UVM scoreboards, assertions, and integration tests.
- Verified clock gating and power mode logic in a complex SoC, gaining hands-on experience with UVM-based IP verification and AMBA protocols; additionally supported ROM generation and integration.
- Streamlined verification by improving scripts, tooling, and reusable components, and authored detailed IP/VIP documentation to reduce integration overhead.

Studentische Hilfskraft (SHK) | Mar – Sep 2023

Center for Advancing Electronics Dresden

- Designed a hardware-assisted Federated Learning framework for IoT applications, enabling privacy-preserving distributed training across edge devices.
- Optimized neural networks through quantization, reducing size and compute overhead while maintaining accuracy for efficient edge deployment.

Digital Design and Verification Engineer | Apr – Sep 2022

Center of Semiconductors Technology (CINVESTAV)

- Verified experimental RTL designs with UVM-based test benches, and implemented synthesis and physical design flows using Cadence Genus/Innovus.
- Designed custom logic cells in Virtuoso for a proprietary PDK and created Dockerized training environments with OpenLane to enable reproducible RTL-to-GDSII experiments.

EDUCATION

Technische Universität Dresden | Oct 2022 – Apr 2025

Master of Science in Nanoelectronic Systems

- Thesis: "Generator Concept for Complex SoC Designs"
- Relevant Coursework: HW Modelling & Simulation, HW/SW Co-design, RF Integrated Circuits, Embedded Hardware Systems Design, Physical Design.

CINVESTAV | Sep 2021 – Feb 2022

Diploma Course in Integrated Circuit (IC) Design

- Short-term, postgraduate-level program on IC design fundamentals and EDA tools.
- Relevant Coursework: Digital Design & Verification, Synthesis, Physical Design, DFT.

Southern Oregon University | Sep 2019 – Jun 2020

Abroad Studies – Computer Science

- Relevant Coursework: **Algorithms and Data Structures**, Operating Systems, **C & UNIX**, Machine Learning.

Universidad de Guanajuato | Jan 2017 – Dec 2021

Bachelor of Science in Mechatronics Engineering

- Relevant Coursework: Digital Electronics, Analog Electronics, Object-Oriented Programming, Signals and Systems.

SKILLS

RTL Design and Verification

- Verilog, SystemVerilog, System C, VHDL.
- UVM, SystemVerilog Assertions (SVAs), Functional and code coverage.

Programming Languages

- C/C++, Python, TCL, Rust.

Tools

- Linux, Git, JIRA, Docker, Shell scripting (bash, zsh, tcsh), Make.
- Cadence Xcelium, QuestaSim/ModelSim, Verilator, Xilinx Vivado & Vitis; experience with ASIC and FPGA flows.

Protocols

- AMBA (AXI, APB, AHB), JTAG, UART, SPI, I2C.

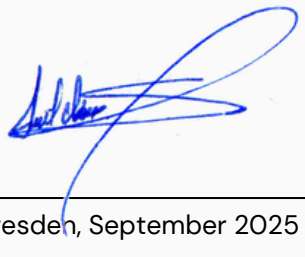
LANGUAGES

- English (**C1**)
- German (**A2**) ~ *Work in Progress!*
- Spanish (**Native**)

HOBBIES & INTERESTS

- 3D Printing & DIY Electronic projects.
- Fiction books, movies & games.
- Cooking & sharing traditional food.

Saul Isaac Sanchez Flores



Dresden, September 2025