

Seat No.

Name

Lab-2:

Circuit Draw using Microsoft Visio Tool

EP1749096

SHEIKH SAAD HUSSAIN

Submitted to:

Sir Hussain Saleem (Assistant Professor / Course Incharge)

Department of Computer Science, UBIT, University of Karachi.

Lab-3 CAODate: March 16 2019Figure 6-15 Ripple carry AdderFA1:

A B Cin

Input: 1 1 0 1/0

Output: - (give output only when carry applied)

FA2

A B Cin

Input: 1 0 1/0

Output: Gives opt only when FA1 gives carry to it.

FA3

A B Cin

Input: 1 0 1/0

Output: Only when Cout by FA1 and Cout from FA2.

The delay is the worst case addition time.

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The Look ahead carry adder:

Derivations

Fig 6-16

6/6(a)

Input: 110

Opt: 1 → Cout

6/6(b)

Input: 111

Opt: 1 → Cout

6/6(c)

Opt: 101

Opt: 1 → Cout

6/6(d)

Opt: 001

Opt: 1 → Cout

M. Hamza

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Carry Propagation / Carry Generation.
 C_p C_g

FA-1

Input: $A_1 B_1 C_{in1}$ } $C_{g1} = A_1 B_1$
 Opt: C_{out1} } $C_{p1} = A_1 + B_1$

FA2

Input: $\overline{A_2} B_2 C_{in2}$ } $C_{g2} = A_2 B_2$
 Opt: C_{out2} } $C_{p2} = A_2 + B_2$

FA3

Ipt : $A_3 B_3 C_{in3}$ } $C_{g3} = A_3 B_3$
 Opt : C_{out3} } $C_{p3} = A_3 + B_3$

FA4

Ipt : $A_4 B_4 C_{in4}$ } $C_{g4} = A_4 B_4$
 Opt : C_{out4} } $C_{p4} = A_4 + B_4$

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Derivations

$$\underline{FA-1} : C_{out1} = C_{g1} + C_p C_{in1}$$

$$\underline{FA-2} : C_{in2} = C_{out1}$$

$$\begin{aligned} C_{out2} &= C_{g2} + C_{p2} C_{in2} = C_{g2} + C_{p2} C_{out1} \\ &= C_{g2} + C_{p2} C_{g1} + C_{p2} C_{p1} C_{in1} \end{aligned}$$

$$\underline{FA-3} :$$

$$C_{in3} = C_{out2}$$

$$\begin{aligned} C_{out3} &= C_{g3} + C_{p3} (C_{g2} + C_{p2} C_{g1} + C_{p2} C_{p1} C_{in1}) \\ &= C_{g3} + C_{p3} C_{g2} + C_{p3} C_{p2} C_{g1} + C_{p3} C_{p2} C_{p1} C_{in1} \end{aligned}$$

$$\underline{FA-4} : C_{in4} = C_{out3}$$

$$\begin{aligned} C_{out4} &= C_{g4} + C_{p4} C_{g3} + C_{p4} C_{p3} C_{g2} + C_{p4} C_{p3} C_{p2} C_{g1} \\ &\quad + C_{p4} C_{p3} C_{p2} C_{p1} C_{in1} \end{aligned}$$

M. Hamza Products