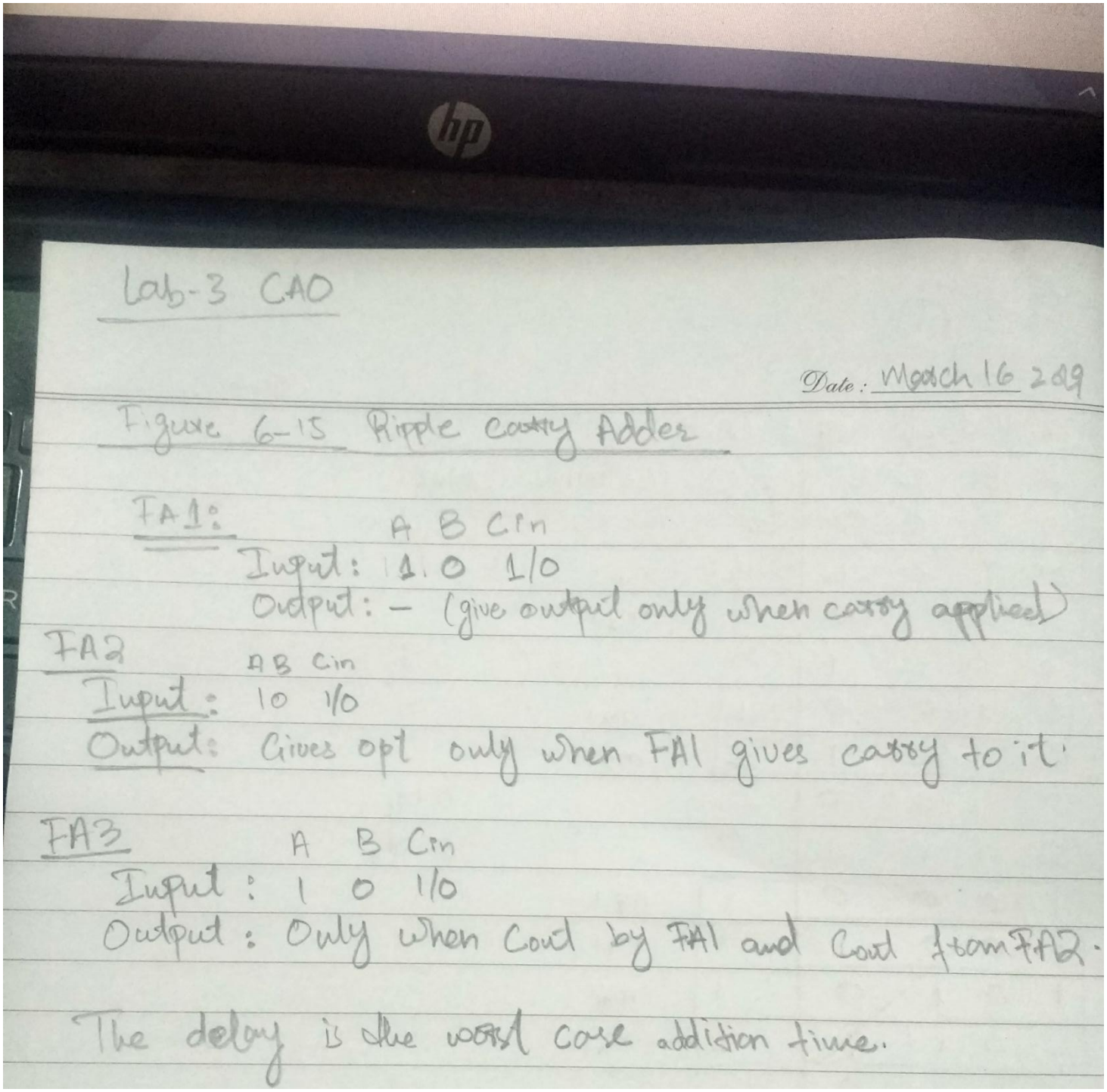
Seat No.	Name	Lab-3: Logic Design of Arithmetic Circuits
EP1749096	SHEIKH SAAD HUSSAIN	Submitted to: Sir Hussain Saleem (Assistant Professor / Course Incharge) Department of Computer Science, UBIT, University of Karachi.



Lab-3 CAO

Date: March 16 209

Figure 6-15 Ripple carry Adder

FA1: A B Cin

Input: 1 0 1/0

Output: – (give output only when carry applied)

FA2 A B Cin

Input: 1 0 1/0

Output: Gives opt only when FA1 gives carry to it.

FA3 A B Cin

Input: 1 0 1/0

Output: Only when Cout by FA1 and Cout from FA2.

The delay is the worst case addition time.

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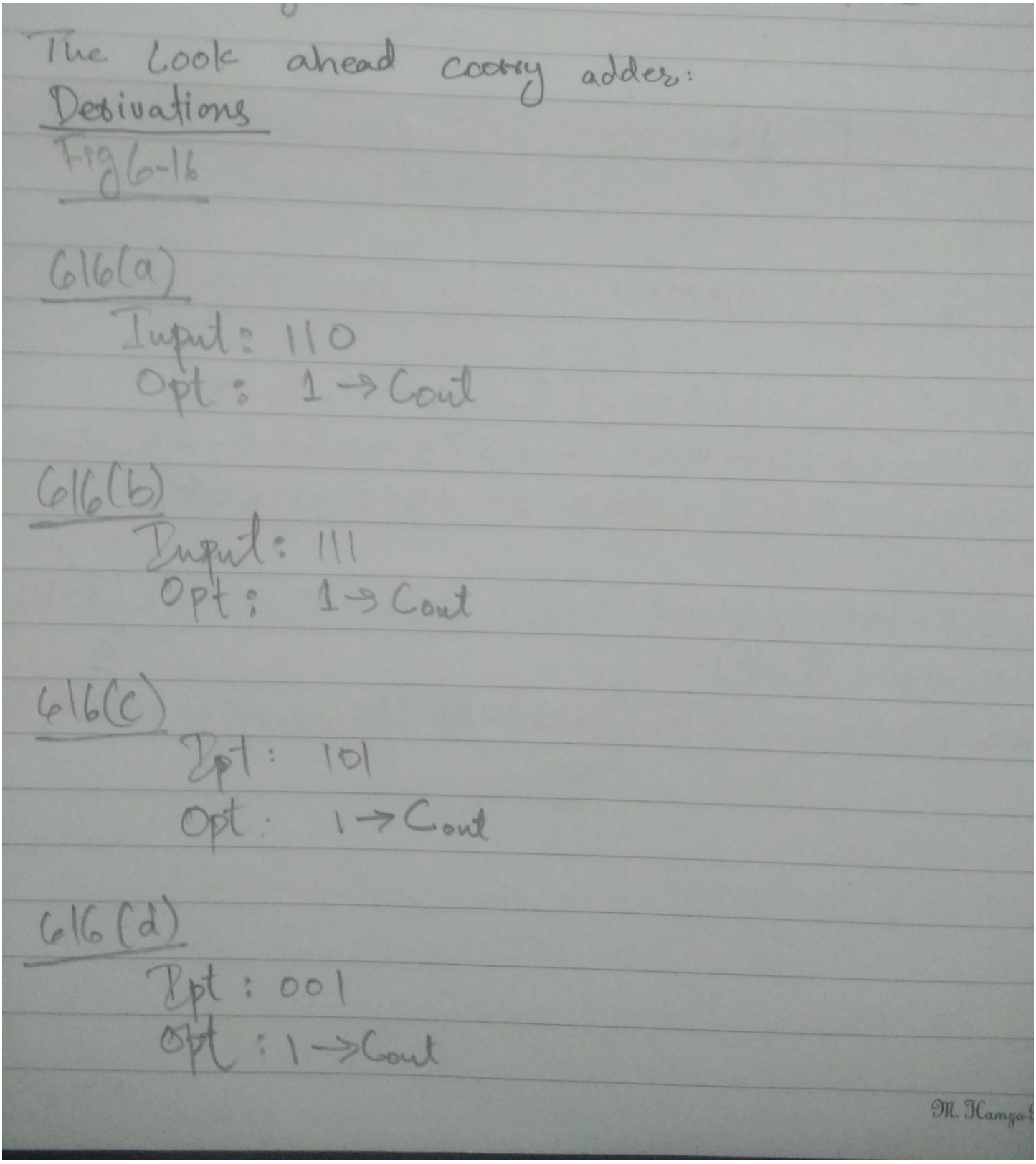

The Look ahead carry adder:

Derivations

Fig 6-16

6.16(a)

Input: 110

Opt: 1 → Cout

6.16(b)

Input: 111

Opt: 1 → Cout

6.16(c)

Ipt: 101

Opt: 1 → Cout

6.16(d)

Ipt: 001

Opt: 1 → Cout

M. Hamza

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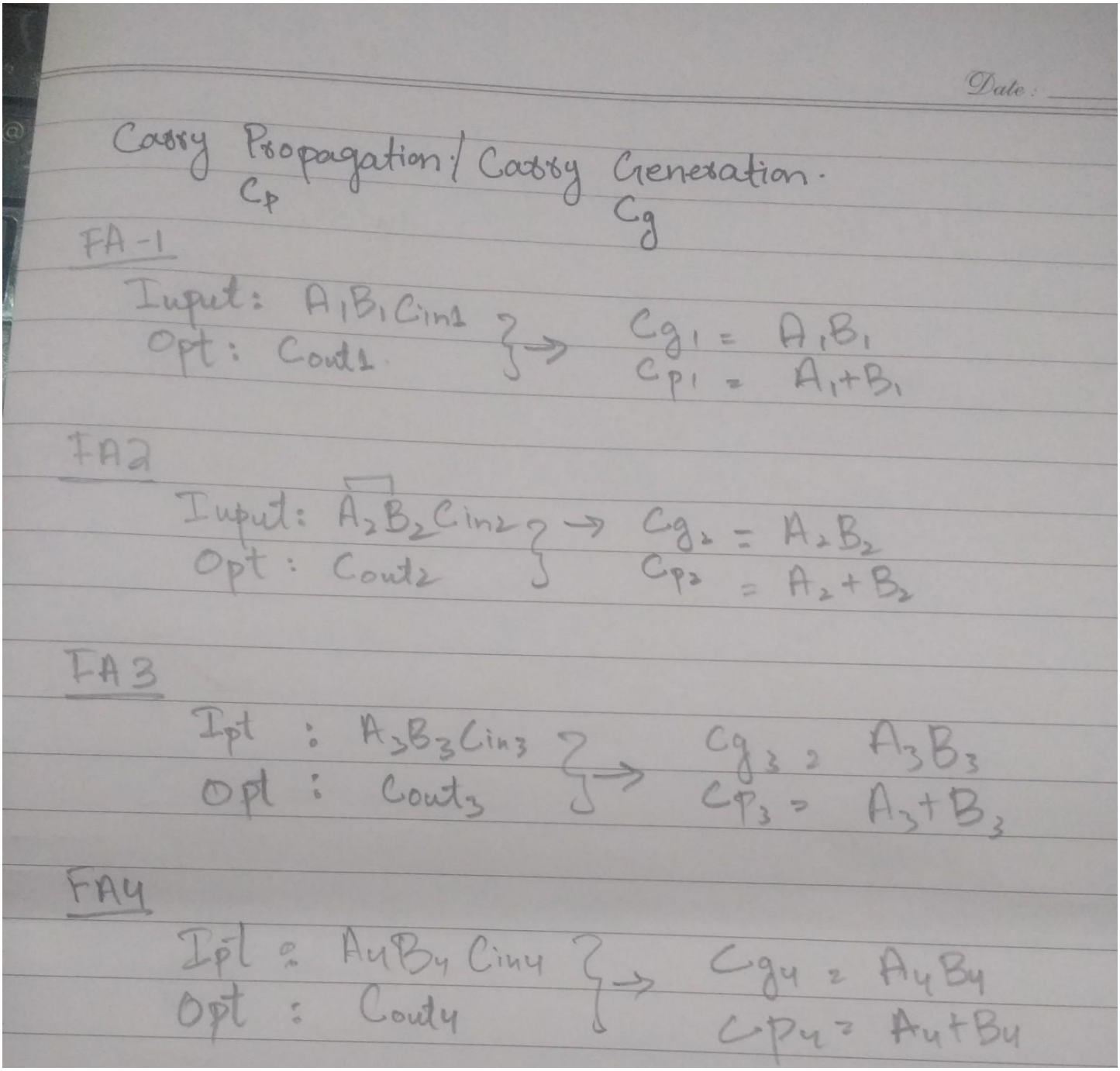

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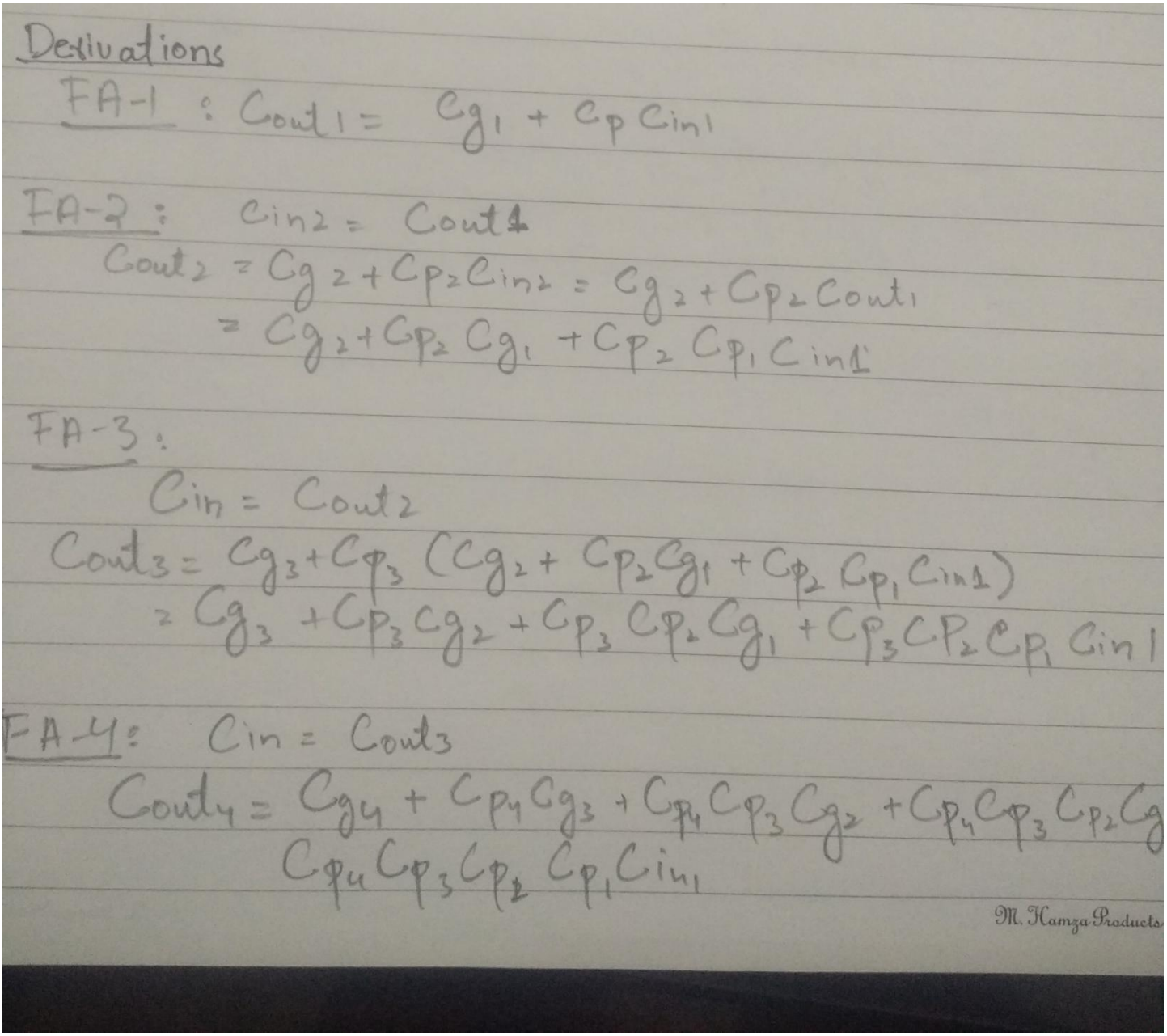

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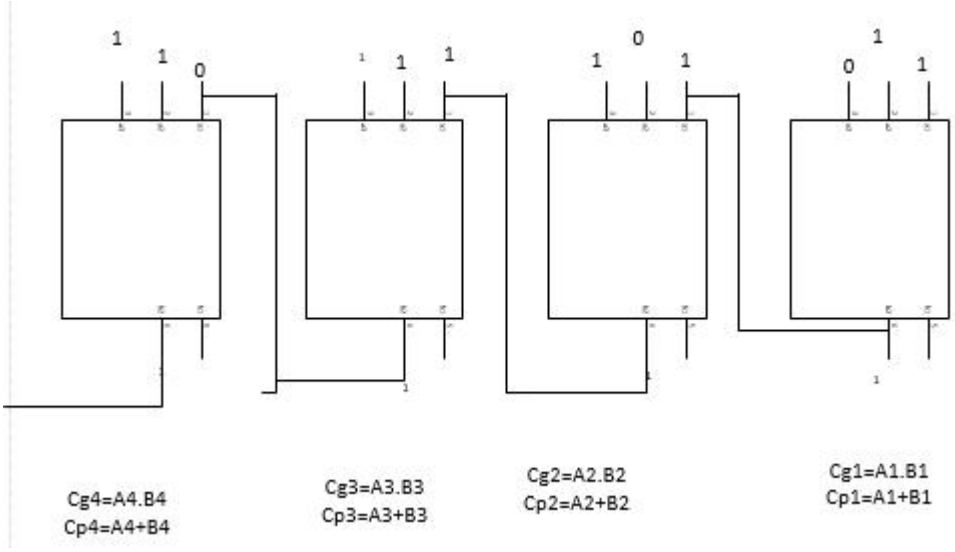
Derivation diagram



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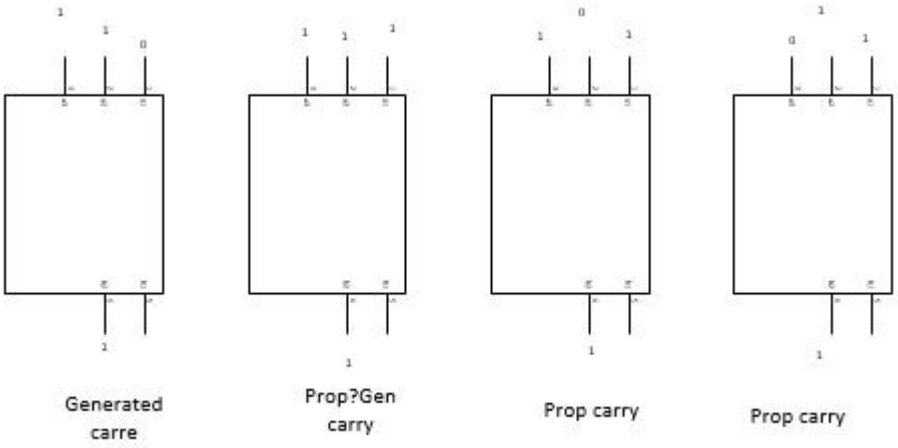
Look-Ahead Carry Adder



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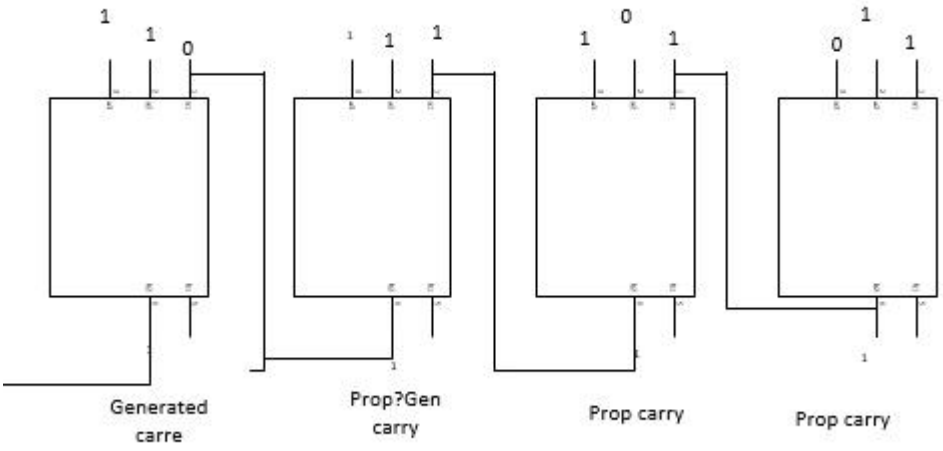
Ripple Carry Adder



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QUESTION:2

Lab-3 : Arithematic Circuits. Date :

3-Bits Parallel Adder : Page one

Expressions / Derivations:

Inputs A_0B_0, A_1B_1, A_2B_2

HA-1 :

Outputs : $\Sigma = A_0 \oplus B_0$ → 1s

$C_{out} = A_0B_0$

FA-1 :

Ipt : A_1, B_1, C_{in} (C_{in} from C_{out}).

Opt : $\Sigma = (A_1 \oplus B_1) \oplus C_{in}$ → 2s

$C_{out} = A_1B_1 + (A_1 \oplus B_1) C_{in}$.

FA-2 :

Ipt : A_2, B_2, C_{in}

Opt : $\Sigma = (A_2 \oplus B_2) \oplus C_{in}$ → 4s

$C_0 = A_2B_2 + (A_2 \oplus B_2) C_{in}$ → 8s

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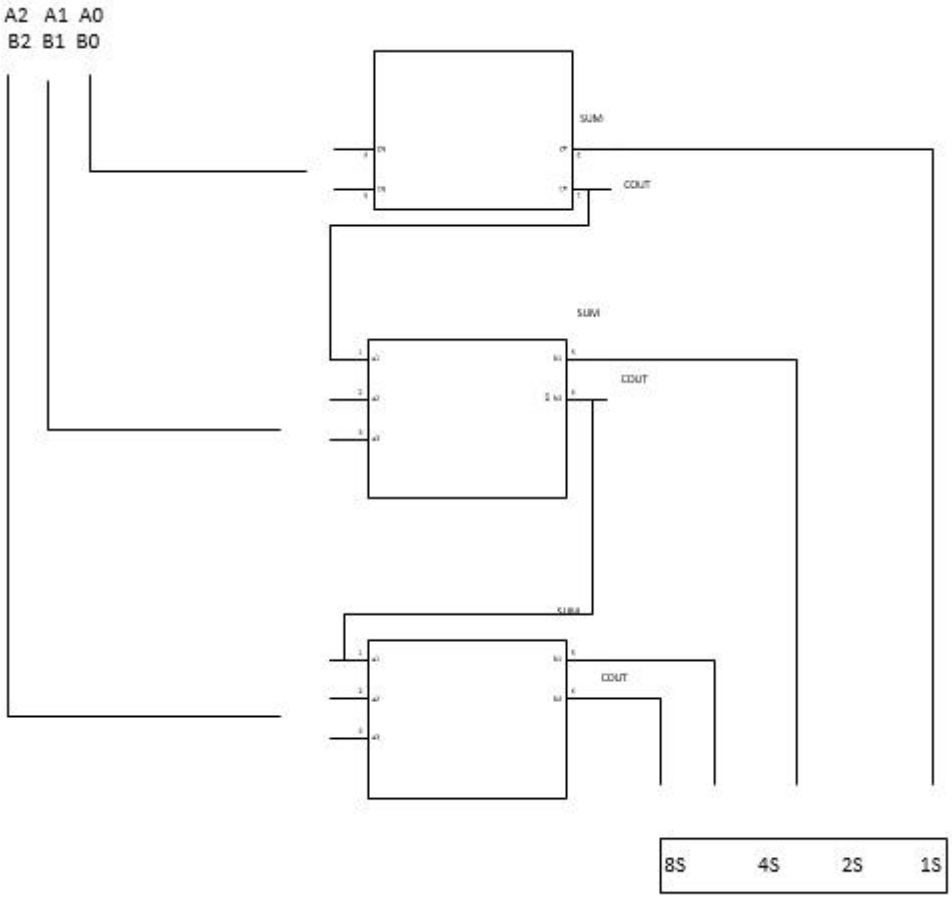
3 bit parallel adder



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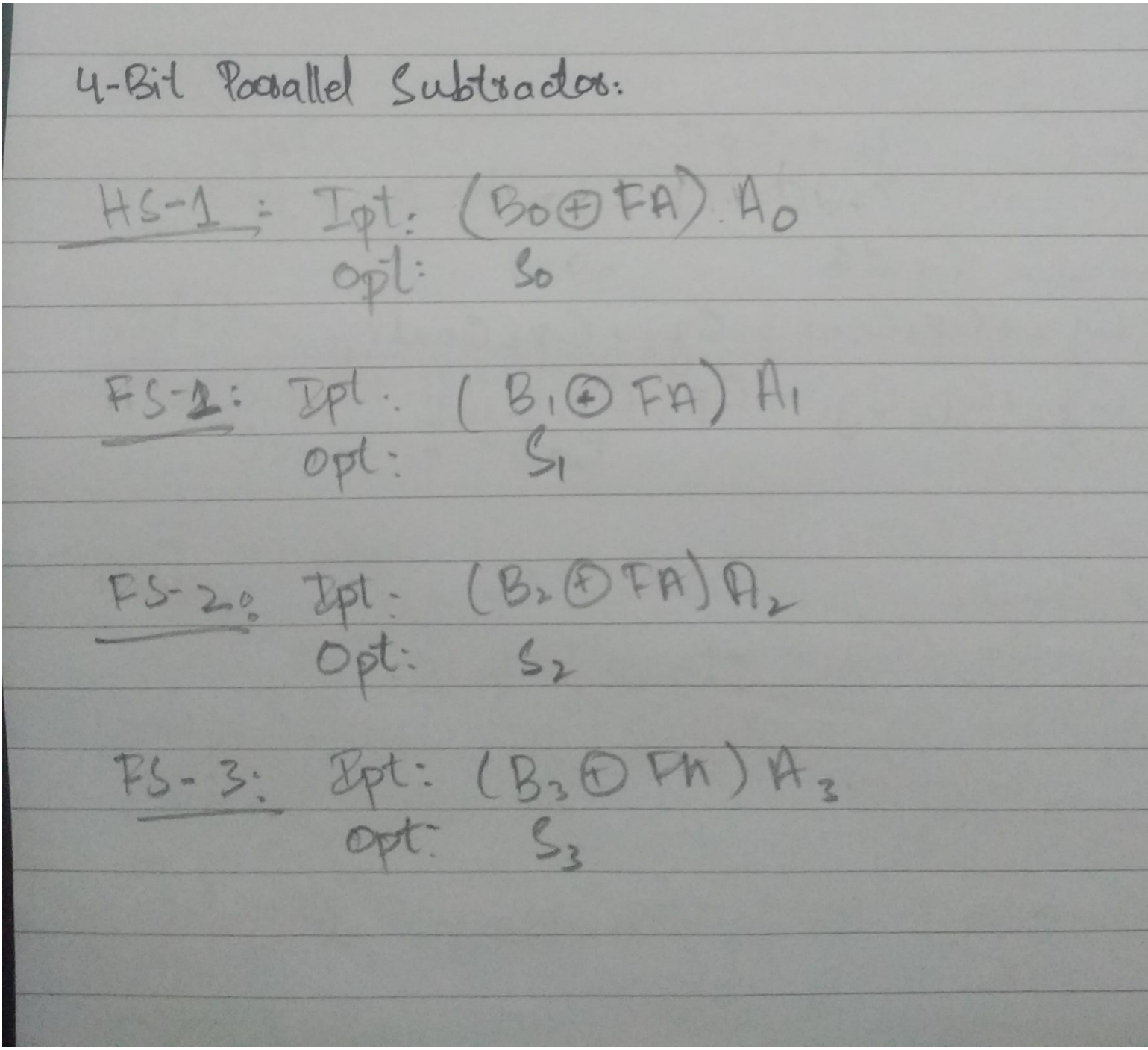

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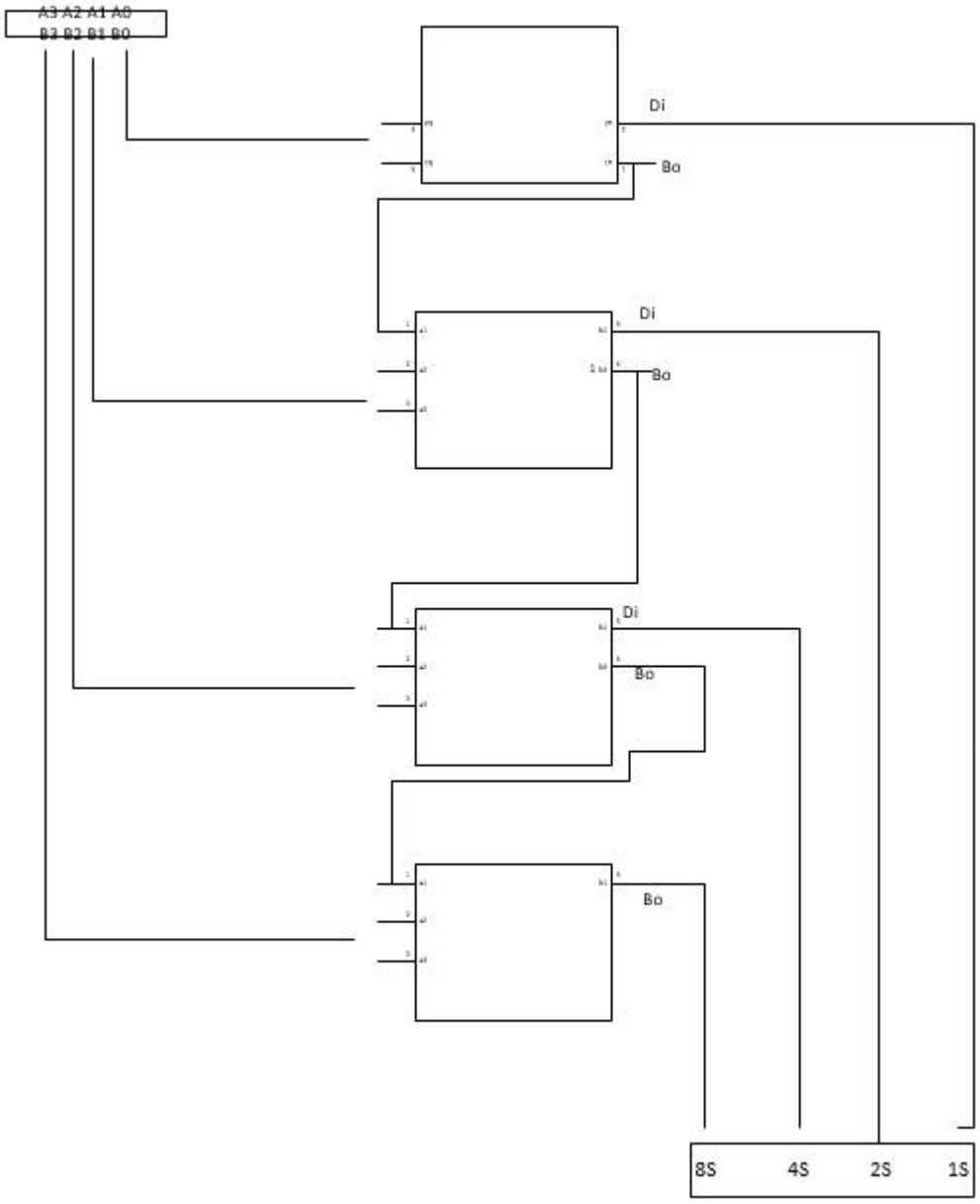
4 Bit parallel subtractor



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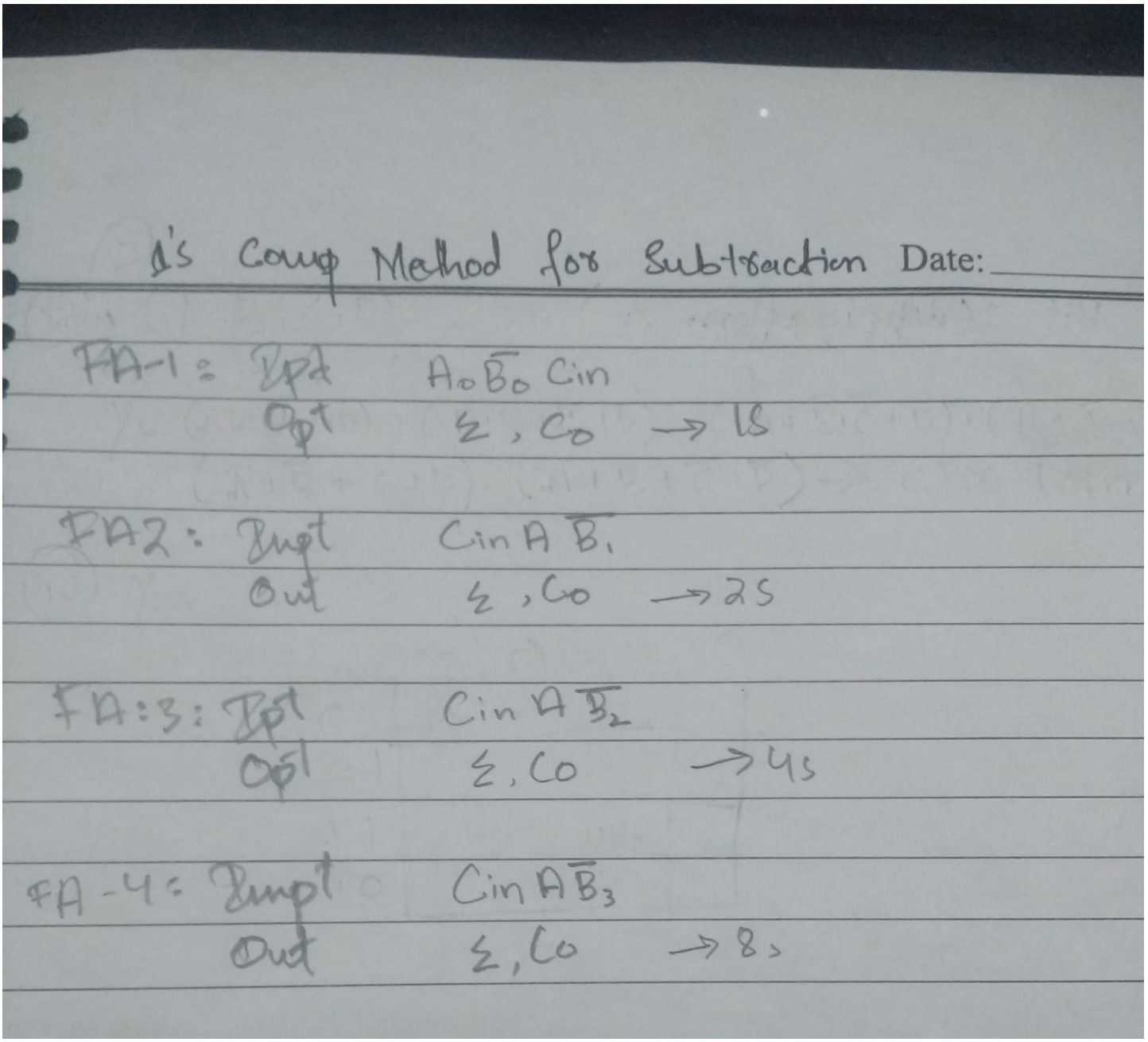

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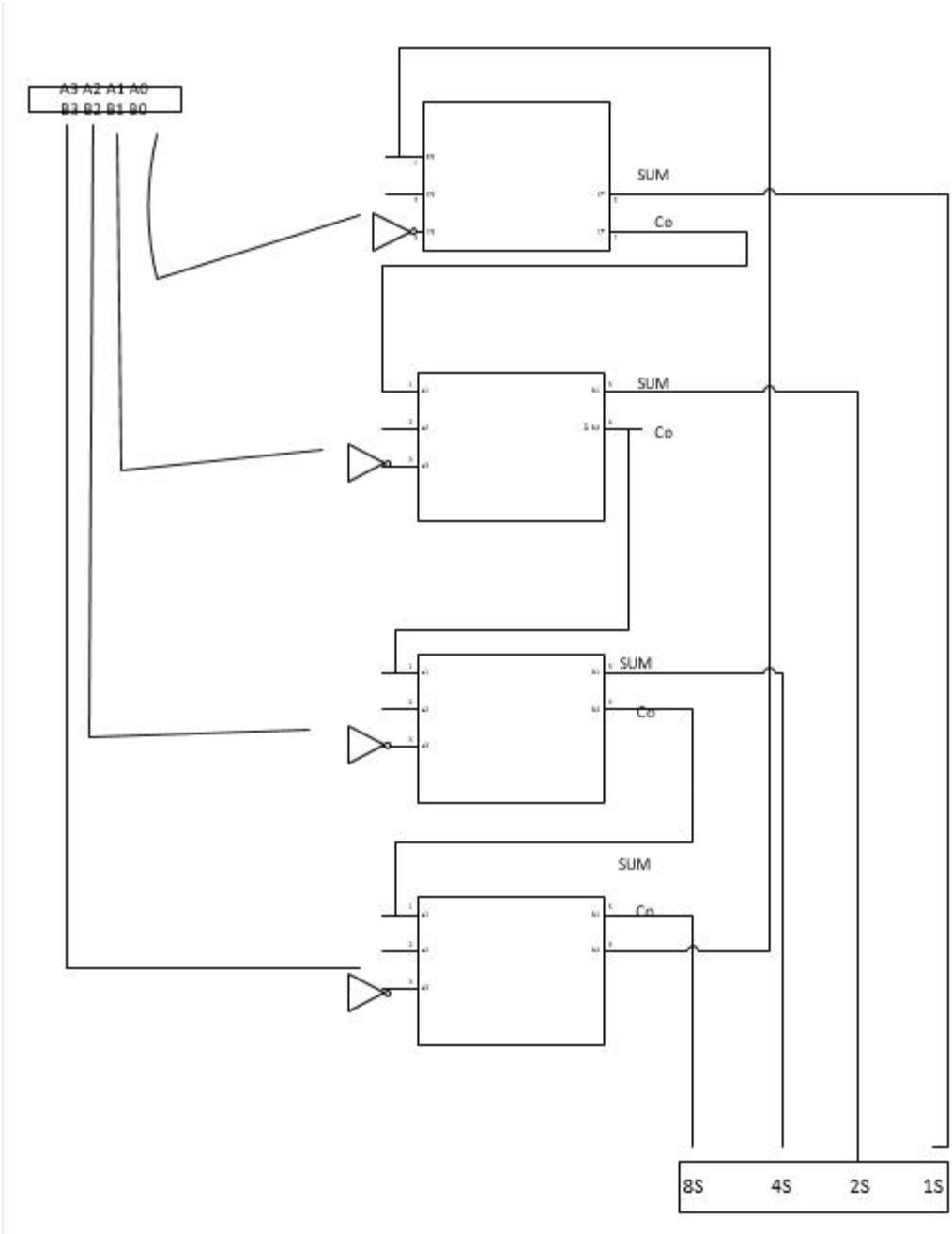
1s complement method for subtraction



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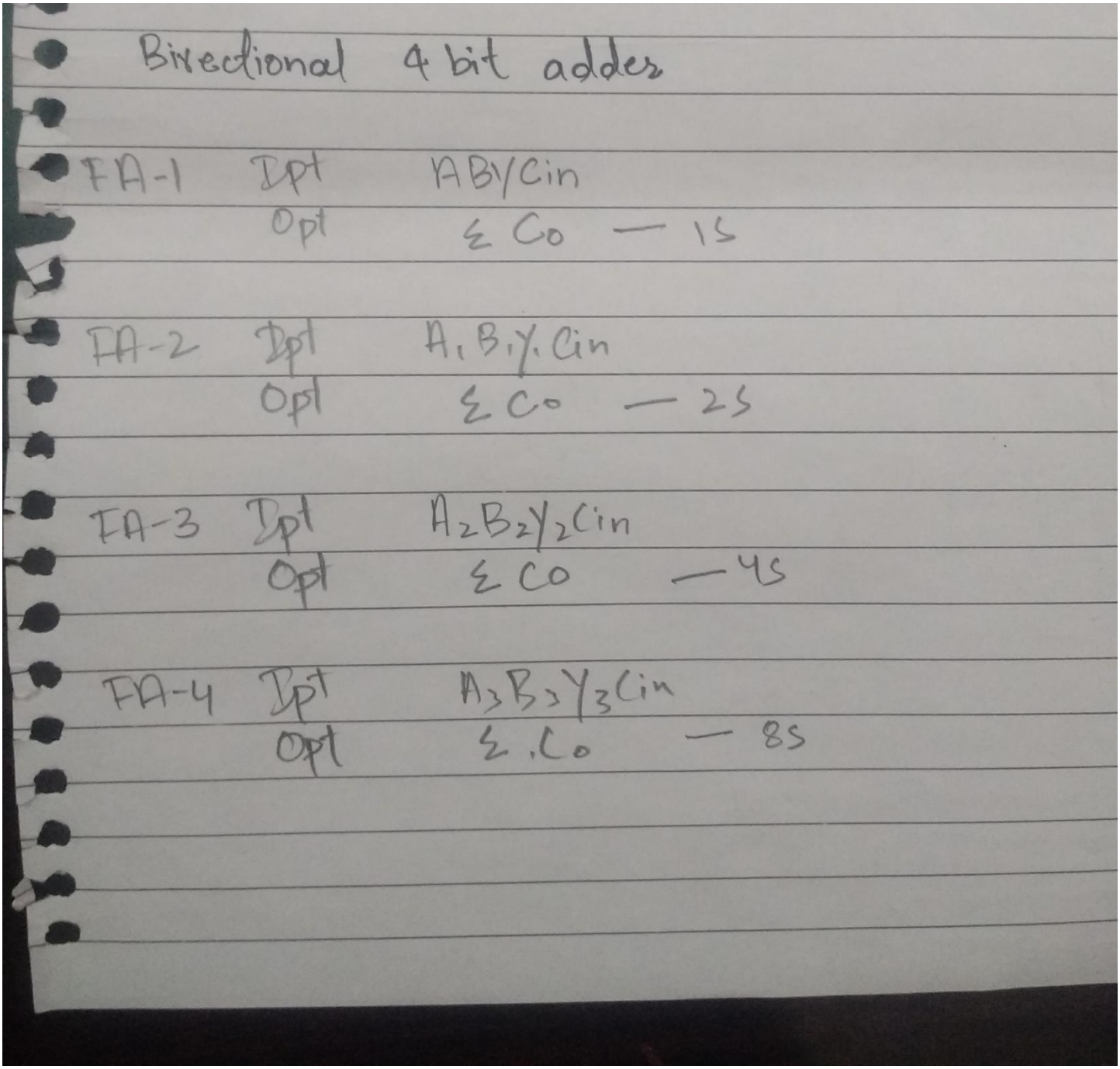

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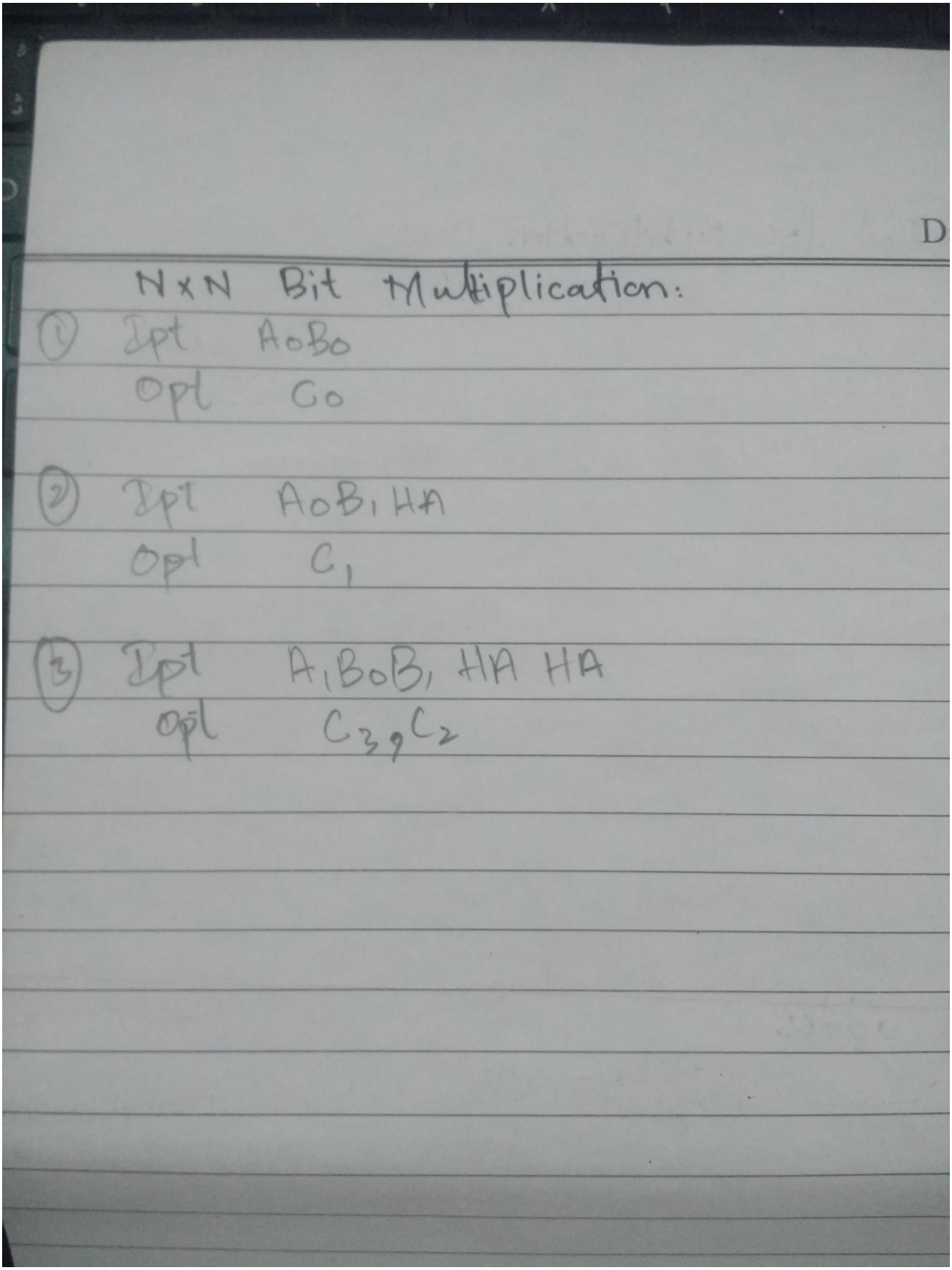

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NxN Multiplication