

Seat No.

Name

Lab-3:

Logic Design of Arithmetic Circuits

EP1749096

SHEIKH SAAD HUSSAIN

Submitted to:

Sir Hussain Saleem (Assistant Professor / Course Incharge)

Department of Computer Science, UBIT, University of Karachi.

Lab-3 CAODate: March 16 2019Figure 6-15 Ripple carry AdderFA1:

A B Cin

Input: 1 1 0 1/0

Output: - (give output only when carry applied)

FA2

A B Cin

Input: 1 0 1/0

Output: Gives opt only when FA1 gives carry to it.

FA3

A B Cin

Input: 1 0 1/0

Output: Only when Cout by FA1 and Cout from FA2.

The delay is the worst case addition time.

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The Look ahead carry adder:

Derivations

Fig 6-16

6/6(a)

Input: 110

Opt: 1 → Cout

6/6(b)

Input: 111

Opt: 1 → Cout

6/6(c)

Opt: 101

Opt: 1 → Cout

6/6(d)

Opt: 001

Opt: 1 → Cout

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Carry Propagation / Carry Generation.
 C_p C_g

FA-1

Input: $A_1 B_1 C_{in1}$ } $C_{g1} = A_1 B_1$
 Opt: C_{out1} } $C_{p1} = A_1 + B_1$

FA2

Input: $\overline{A_2} B_2 C_{in2}$ } $C_{g2} = A_2 B_2$
 Opt: C_{out2} } $C_{p2} = A_2 + B_2$

FA3

Ipt : $A_3 B_3 C_{in3}$ } $C_{g3} = A_3 B_3$
 Opt : C_{out3} } $C_{p3} = A_3 + B_3$

FA4

Ipt : $A_4 B_4 C_{in4}$ } $C_{g4} = A_4 B_4$
 Opt : C_{out4} } $C_{p4} = A_4 + B_4$

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Derivations

$$\underline{FA-1}: C_{out1} = C_{g1} + C_p C_{in1}$$

$$\underline{FA-2}: C_{in2} = C_{out1}$$

$$\begin{aligned} C_{out2} &= C_{g2} + C_{p2} C_{in2} = C_{g2} + C_{p2} C_{out1} \\ &= C_{g2} + C_{p2} C_{g1} + C_{p2} C_{p1} C_{in1} \end{aligned}$$

$$\underline{FA-3}: C_{in3} = C_{out2}$$

$$\begin{aligned} C_{out3} &= C_{g3} + C_{p3} (C_{g2} + C_{p2} C_{g1} + C_{p2} C_{p1} C_{in1}) \\ &= C_{g3} + C_{p3} C_{g2} + C_{p3} C_{p2} C_{g1} + C_{p3} C_{p2} C_{p1} C_{in1} \end{aligned}$$

$$\underline{FA-4}: C_{in4} = C_{out3}$$

$$\begin{aligned} C_{out4} &= C_{g4} + C_{p4} C_{g3} + C_{p4} C_{p3} C_{g2} + C_{p4} C_{p3} C_{p2} C_{g1} \\ &\quad + C_{p4} C_{p3} C_{p2} C_{p1} C_{in1} \end{aligned}$$

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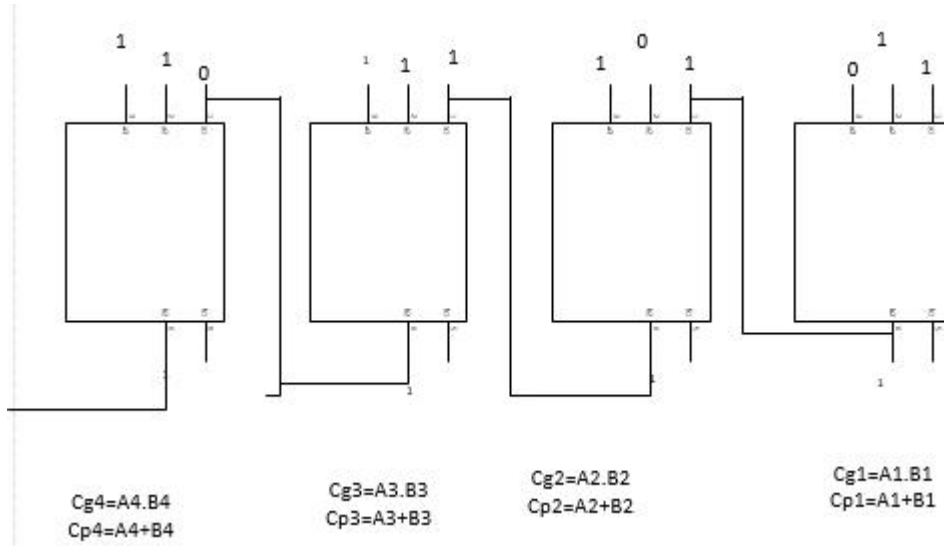
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Derivation diagram



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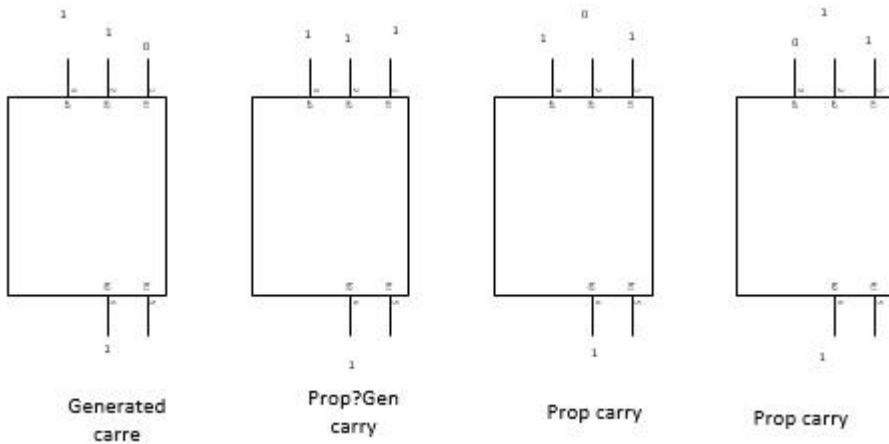
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Look-Ahead Carry Adder



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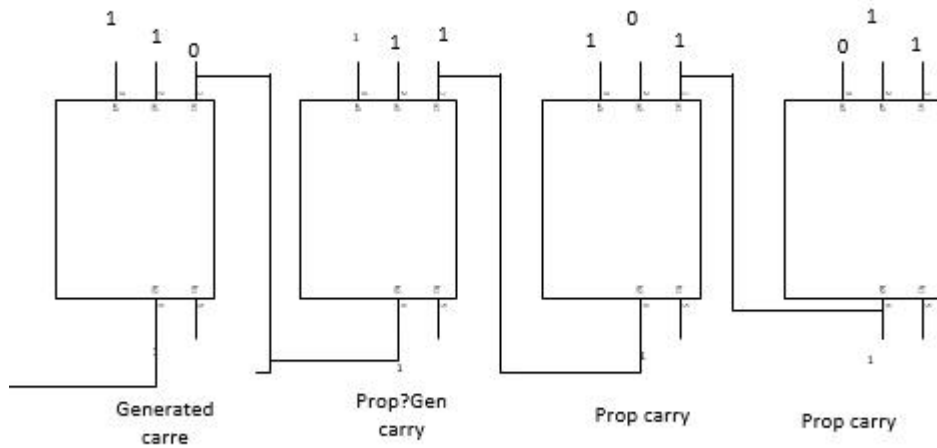
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Ripple Carry Adder



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QUESTION:2

Lab-3 : Arithmetic Circuits.

Date : _____

3-Bits Parallel Adder : Page one

Expressions / Derivations:

Inputs $A_0, B_0, A_1, B_1, A_2, B_2$ HA-1:

Outputs: $\Sigma = A_0 \oplus B_0 \rightarrow 1s$
 $Count = A_0 B_0$

FA-1:Ipt: A_1, B_1, Cin (Cin from Count).Opt: $\Sigma = (A_1 \oplus B_1) \oplus Cin \rightarrow 2s$
 $Count = A_1 B_1 + (A_1 \oplus B_1) Cin$
FA-2:Ipt: A_2, B_2, Cin Opt: $\Sigma = (A_2 \oplus B_2) \oplus Cin \rightarrow 4s$
 $C_0 = A_2 B_2 + (A_2 \oplus B_2) Cin \rightarrow 8s$

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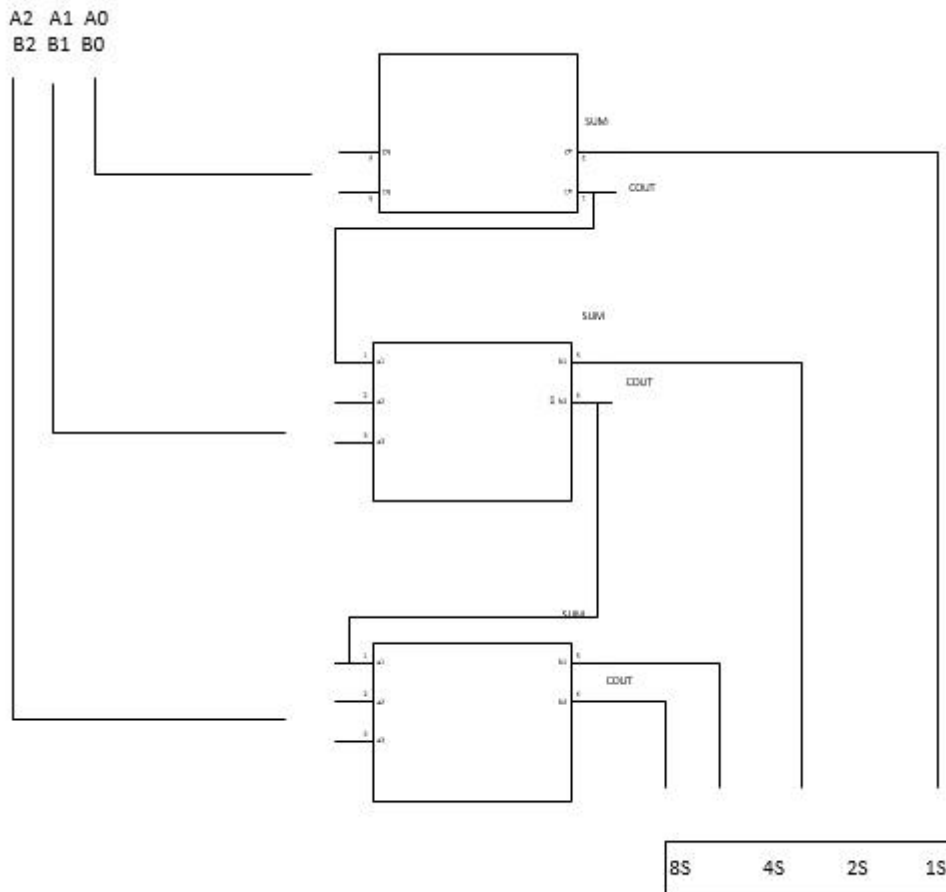
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3 bit parallel adder



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4-Bit Parallel Subtractor:

$$\underline{HS-1}: \text{Ipt: } (B_0 \oplus FA) A_0 \\ \text{Opt: } S_0$$

$$\underline{FS-1}: \text{Ipt: } (B_1 \oplus FA) A_1 \\ \text{Opt: } S_1$$

$$\underline{FS-2}: \text{Ipt: } (B_2 \oplus FA) A_2 \\ \text{Opt: } S_2$$

$$\underline{FS-3}: \text{Ipt: } (B_3 \oplus FA) A_3 \\ \text{Opt: } S_3$$

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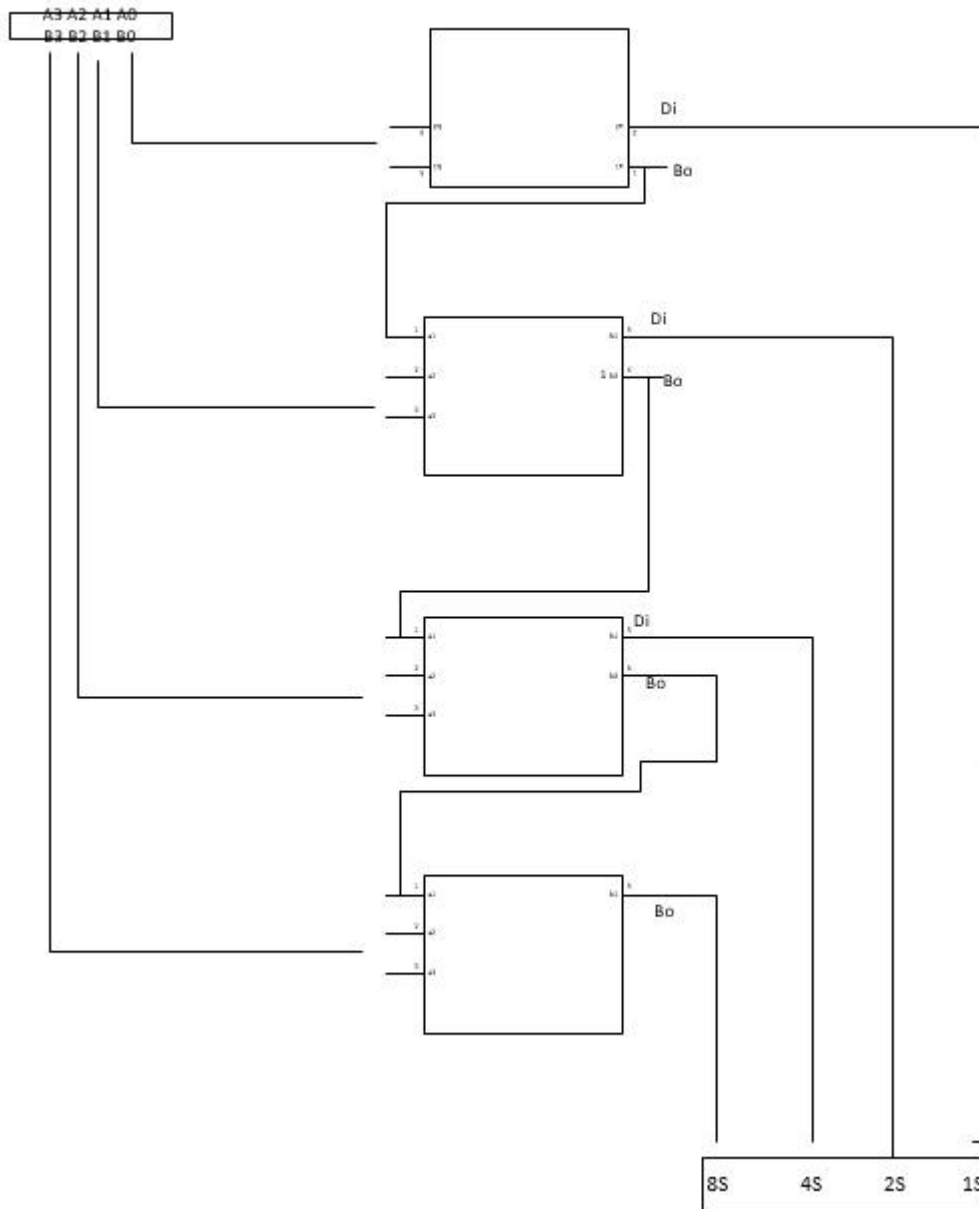
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4 Bit parallel subtractor



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1's Comp Method for Subtraction Date: _____

FA-1: 2pt
Op1 $A_0 \bar{B}_0 \text{ Cin}$
 $\Sigma, Co \rightarrow 1s$

FA-2: 2pt
Out $Cin A \bar{B}_1$
 $\Sigma, Co \rightarrow 2s$

FA-3: 2pt
Op1 $Cin A \bar{B}_2$
 $\Sigma, Co \rightarrow 4s$

FA-4: 2pt
Out $Cin A \bar{B}_3$
 $\Sigma, Co \rightarrow 8s$

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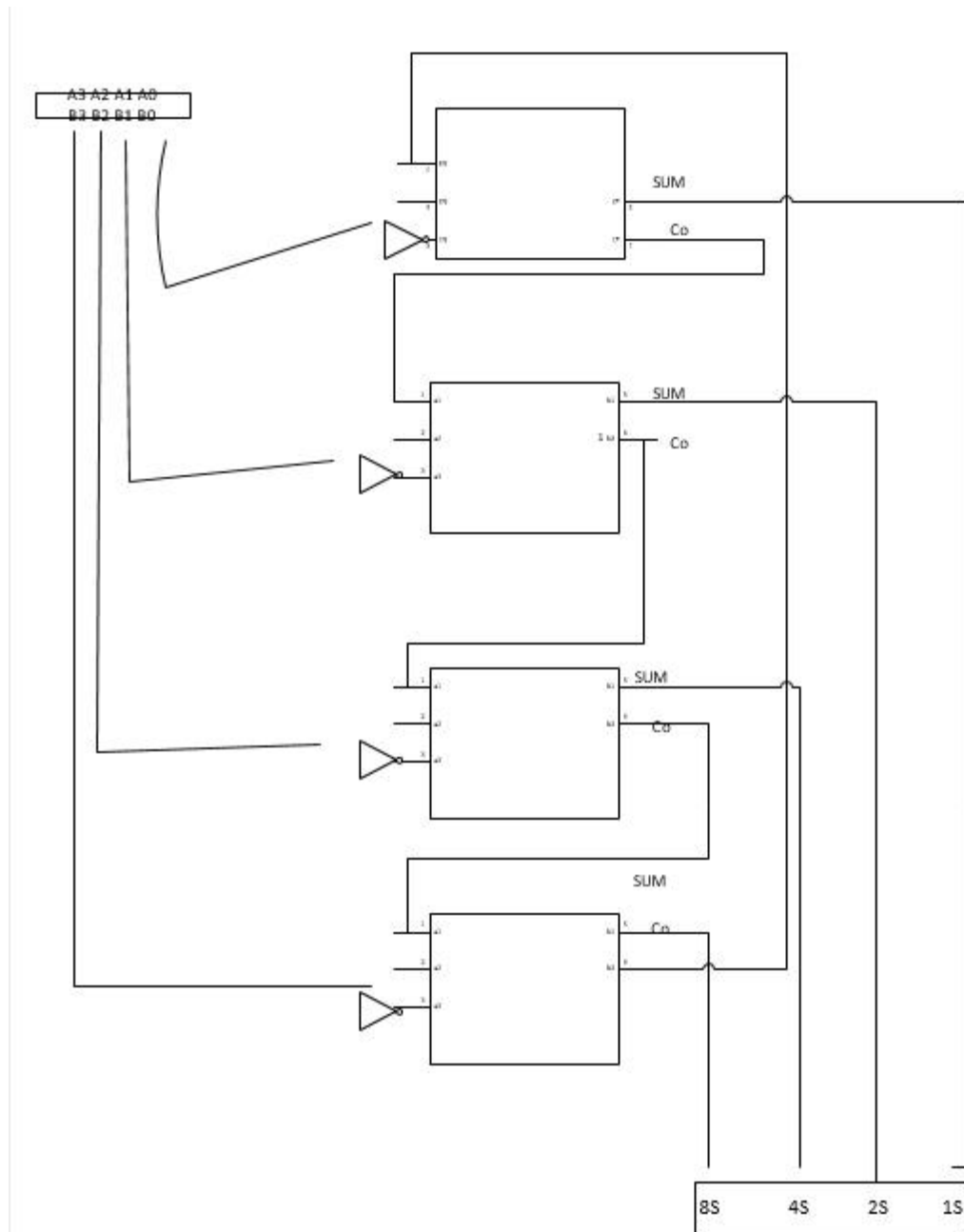
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1s complement method for subtraction



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Birectional 4 bit adder

FA-1 Dpt AB/C_{in}
 Opt ΣC_o — 15

FA-2 Dpt $A_1 B_1 / C_{in}$
 Opt ΣC_o — 25

FA-3 Dpt $A_2 B_2 / C_{in}$
 Opt ΣC_o — 45

FA-4 Dpt $A_3 B_3 / C_{in}$
 Opt ΣC_o — 85

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N x N Bit Multiplication:

① 2pt A₀B₀
0pt C₀

② 2pt A₀B₁ HA
0pt C₁

③ 2pt A₁B₀B₁ HA HA
0pt C₃, C₂

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NxN Multiplication

