CURRICULUM VITAE

ASHRAF MANIYAR
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Google Scholar Id: https://scholar.google.co.in/citations?user=P-ouprAAAAAJ&hl=en

CAREER OBJECTIVE

I aim to achieve a challenging and professional position in which I can make a significant contribution to the organization through my dedication and by using all my skills.

TECHNICAL SKILLS

- Well-versed with MS Office (MS Word, MS Excel, MS Power point)
- Internet
- MATLAB
- TCAD
- XILINX
- Cadence Virtuoso
- ATLAS
- Machine Learning
- Physics
- Chemistry
- User Research
- Numerical Method

WORK EXPERIENCE

- **Serving as a role of Chair , IEEE EDS student branch chapter IIT Patna from 2024.**
- **HINDUSTAN AERONAUTICS LIMITED, KORWA (U.P.) (AUG 2017–AUG 2018)**
  - **Testing of Auto computer and Roll computer units of Jaguar Aircraft.**
  - **Assembling of Divider, Power supply and Output Modules.**
  - **Testing of Divider Module and Power supply Module.**
- I have worked as a teaching assistant in MTech and am currently in PhD and have worked on projects and my dissertation thesis.
- **Subjects handled: Engineering Physics, Basic Semiconductor devices, Linear Integrated Circuit Design, Digital electronics, Integrated Circuit Design, Basic Electronics, Circuit Theory.**

ACADEMIC QUALIFICATION

Degree / Certification	Qualification	Board / University	Year of Passing	Marks (%)/CGPA
Ph.D.	**Ph.D.** **(**Electrical Engineering**)**	IIT Patna	**2025(May)**	**7.75**
Post-Graduation	**M.Tech** (VLSI Design)	NIT Kurukshetra	**2020**	**8.42**

Graduation	**B.Tech** (Electronics and Communication Engineering)	NIT Nagaland	**2016**	**80.00**
12th	**Senior Secondary**	**RBSE** (PILANIA ACADEMY, TARANAGAR)	**2011**	**61.69**
10th	**Secondary School**	**RBSE** (PILANIA ACADEMY, TARANAGAR)	**2009**	**90.17**

M.Tech Dissertation: Visible Region Absorption in TMDs/Phosphorene Heterostructures for Use in Solar Energy Conversion Applications

B.Tech Project: - Cascaded Multilevel Inverter Structure with Reduce no. of Switches.

ACADEMIC ACHIEVEMENTS, AWARDS, AND FELLOWSHIPS

- **2nd Rank in B.Tech,** Department of Electronics and Communication Engineering, NIT Nagaland
- **5th Rank** in M.Tech., Department of VLSI Design, NIT Kurukshetra
- GATE-2016, 2018 (Electronics and Communication Engineering) qualified
- PG Scholarship (GATE) provided by UGC for pursuing M.Tech

Journal Papers

1. A. Maniyar, P. S. T. N. Srinivas, K. -S. Chang-Liao, and P. K. Tiwari, "Impact of Process-Induced Inclined Side-Walls on Gate-Induced Drain Leakage (GIDL) Current of Nanowire GAA MOSFETs" in *IEEE Trans. Electron Devices*, pp. 1-6, 02 August 2022, doi.org/10.1109/TED.2022.3194109.
2. A. Maniyar, P. S. T. N. Srinivas, K. -S. Chang-Liao, and P. K. Tiwari "Impact of Process-Induced Inclined Sidewalls on Gate Leakage Current of Nanowire GAA MOSFETs," in *IEEE Trans. Electron Devices*, 2024.
3. A. Maniyar, and Sudhanshu Choudhary. "Visible region absorption in TMDs/phosphorene heterostructures for use in solar energy conversion applications." *RSC Advances* 10 (2020): 31730 - 31739.
4. Impact of Process-Induced Inclined Side-Walls on Thermal Noise of Nanowire GAA MOSFETs in *Physica Scripta*. (Provisionally Accepted)
5. P. Sinha, A. Maniyar, Pushp raj, and P. K. Tiwari " A Quasi 3-D Analytical Model of Gate Induced Drain Leakage (GIDL) Current of Nanowire GAA MOSFETs" in Journal of Electronic Materials. (Minor Revision).
6. S. Das, A. Maniyar, Pushp raj, and P. K. Tiwari "Si/SiGe Superlattice-Based Double Gate Feedback Field-Effect Transistor and its application in 1T-DRAM" in Microelectronics Journal. (Major Revision)

Conference Papers

1. A. Maniyar, P. S. T. N. Srinivas, and P. K. Tiwari "Impact of Substrate Doping on Gate-Induced Drain Leakage Current in FD SOI MOSFETs" *2022 International Conference on Electrical Engineering (ICEE)*, Bangalore, India, 2022.
2. A. Maniyar, P. S. T. N. Srinivas, and P. K. Tiwari "Impact of Process-Induced Inclined Sidewalls on Small Signal Parameters of Silicon Nanowire GAAMOSFET"*TENCON 2023 - 2023 IEEE Region 10*

Conference, Chiang Mai, Thailand, 2023.

STRENGTH

- Eager to learn new things
- Self-motivated & committed
- Good communication & interpersonal skills
- Strong administrative qualities
- Goal oriented
- Highly organized &dedicated
- Hard working
- Highly trustworthy, discreet & ethical
- Positive thinker
- Strong analytical & problem-solving skills

INTERESTS

Internet surfing, Playing Cricket, and Study books

PERSONAL DETAILS

Full Name : Ashraf Maniyar
Father's Name : Nizamuddin
Permanent Address : POST-TARANAGAR, DIST-Churu (845415)
Date of Birth : 14th July 1995
Marital Status : Married
Sex : Male
Languages known : English, Hindi and Urdu

DECLARATION

I hereby declare that all the information given above is true to the best of my knowledge. I will do hard work and be sincere and thankful to you if I get a chance to work in your esteemed organization. I assure you that I will abide by all the rules and regulations of your organization. Expecting a very favorable reply from you at the earliest.

Place: IIT Patna

Date: 17-02-2025 **(ASHRAF MANIYAR)**

References:

Dr. Pramod Kumar Tiwari
Associate Professor
Department of Electrical Engineering,
Indian Institute of Technology Patna,
Bihar, India 801106.
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Dr. Saurabh Kumar Pandey
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