ELEC-3500 Lab #6

Verilog labs 6 and 8

Date: _____ Section: B1 Fri/B2 Wed/B3 Thu/B4 Tue/B5 Mon

Partner 1 Name: _____ Student #: _____

Partner 1 Name: _____ Student #: _____

	Partner 1	Partner 2
Attendance		
In Lab Demo: Checked By:_____	_____/70 (total)	
	Lab 6 1-1	____/7
	Lab 6 1-2	____/7
	Lab 6 1-3	____/7
	Lab 6 1-4	____/7
	Lab 6 1-5	____/7
	Lab 6 2-1	____/7
	Lab 6 2-3	____/7
	Lab 8 1-1	____/7
	Lab 8 1-2	____/7
	Lab 8 2-1	____/7
Code and Questions: Checked By:_____	_____/20	_____/20
Finished in Lab Checked By:_____	_____/10	_____/10
Total:	_____/100	_____/100